# 行政院國家科學委員會專題研究計畫　期中進度報告

## 子計畫七：積極低功率最佳化下之平面規劃(2/3)

計畫類別：整合型計畫
計畫編號：NSC93-2220-E-009-020-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立交通大學電子工程學系暨電子研究所

計畫主持人：陳宏明
共同主持人：周景揚
計畫參與人員：陳宏明

報告類型：完整報告
報告附件：出席國際會議研究心得報告及發表論文
處理方式：本計畫可公開查詢

中　華　民　國 94 年 5 月 31 日

# 行政院國家科學委員會補助專題研究計畫期中報告

## 低功率系統之設計及自動化
## 子計劃七：積極低功率最佳化下之平面規劃
## Floorplanning with Aggressive Power Optimization

計畫編號：NSC 93－2220－E－009－020－
執行期間：93 年 8 月 1 日至 94 年 7 月 31 日
計畫主持人：陳宏明 助理教授 國立交通大學電子工程學系
共同主持人：周景揚 教授 國立交通大學電子工程學系
Email: hmchen@mail.nctu.edu.tw

一、中文摘要

隨著半導體製程進步，元件尺寸縮小，積體電路可以操作在更高的頻率而達到更好的效能。但操作頻率越高，消耗的功率越大。尺寸縮小還會造成漏電流增加。所以現今的積體電路都有功率消耗太高的煩惱。功率消耗的問題不僅僅是會影響到用電池驅動的產品，也會影響到一般的產品的上市所需時間、成本、和可靠度。一個可行的作法是將供應給 IC 的電壓降低，可是降低電壓的同時，電路的延遲時間會加長。故要壓低 IC 的消耗功率又不影響操作速度是個不容易解決的挑戰。CVS 叢聚型電壓調降)是一種可以達成這個目標的做法。這種以 CVS 為基礎的省電方法已經研究了好幾年。相關的雙供應電壓佈局方式，譬如說一行一行的排法，已經被實際應用，並且證明了是可行的方式。因此這一年我們計劃以結合叢聚型電壓調降及電壓佈局方式，加上快速的電路時序分析，進一步形成電壓島，以在平面規劃與放置階段達到低功率消耗，同時顧及電源供應之繞線效應。

關鍵字：供給電壓、叢聚型電壓調降、雙供應電壓、電壓島

英文摘要Abstract

As the semiconductor technology advances, integrated circuits can operate at higher frequencies and achieve higher performance. However, higher operating frequency spends more power. Scaling-down also causes larger leakage current. So the recent high speed ICs suffer from power consumption problems. These problems not only influence the designs for battery powered applications, but also affect the ordinary designs in terms of time to market, cost, and reliability.

One possible way to reduce the IC power is lowering the supply voltage. However, as the supply voltage is lowered, the circuit delay time increases. Therefore it is a great challenge to reduce IC power consumption while maintain high performance. CVS (Clustering Voltage Scaling) is one of the possible solutions to achieve this target. Methods based on CVS for saving power have been studied for years. Relevant dual-supply-voltage layout schemes, such as row-by-row power scheme, had been applied and proved as practical ways. In this year, we plan to develop the methodology to combine CVS and dual-supply-voltage layout schemes, in addition to efficient static timing analysis, trying to further form voltage islands and lower power dissipation in current designs with care on power routing.

Keywords: Supply voltage, CVS, dual-supply-voltage, voltage islands

## 二、計畫的緣由與研究目的（Background and Objective)

### 1. Background

CVS (Clustering Voltage Scaling)[1], was one of the most widely adopted methodology for dual VDD low power designs. Many researches ([2][3][5-9]) afterwards explored possible improvements based on this idea. Different from voltage island schemes [10], these dual-VDD approaches reduce power by utilizing excessive slack in the circuits within the same functional block. Each functional block was powered by two voltage levels at the same time, and works with the same clocking rate but consumes less power. Nevertheless, additional interface circuits ([11][12]) are require to raise the signal voltage level from VDDL to VDDH. These circuits are usually largely compared with standard logic cells. As a result, they form manifest overhead on core area. Controlling the number of these level shifters is one of the critical points of the optimization process.

Power routability is another torment to dual VDD circuit designer. VDDH and VDDL nets must be separated with special care. To prevent area penalty due to the necessary gap between the N-wells connected to VDDH and VDDL, we should choose back-to-back row-based layout scheme for the standard cell design. In addition, the total cell area ratio between VDDH and

VDDL plays a key role of the optimality issue. Poor balance of this ratio would result in poor quality of the optimization. Unfortunately, such ratio strongly depends on the timing constraints and circuit topology of the design, which varies from design to design.

Dual threshold voltage is another solution for low power design [13-19]. But it suffers from process variation problems. So that dual-threshold-voltage seems not to be a suitable solution for standard cell designs. [1-4] are some of the methodologies apply dual-VDD solution. Such methods, however, introduce either power routing difficulty or much area/wire-length overhead. Furthermore, there are problems of consistency in timing analysis with these methods. We tried to solve these problems.

## 2. Objective

Given an original standard cell design with single power supply, we want to obtain a solution to reduce the power consumption with dual supply voltage. Under the same timing restriction, we will find a dual-VDD version for the given design with lower power and good routabilty.

## 三、文獻探討 (Survey on existing literatures)

### 1. Clustering Voltage Scaling

Reference [2] provided Extend CVS (ECVS) algorithm based on the original Clustered Voltage Scaling (CVS) [1] algorithm, as shown in Figure 1.

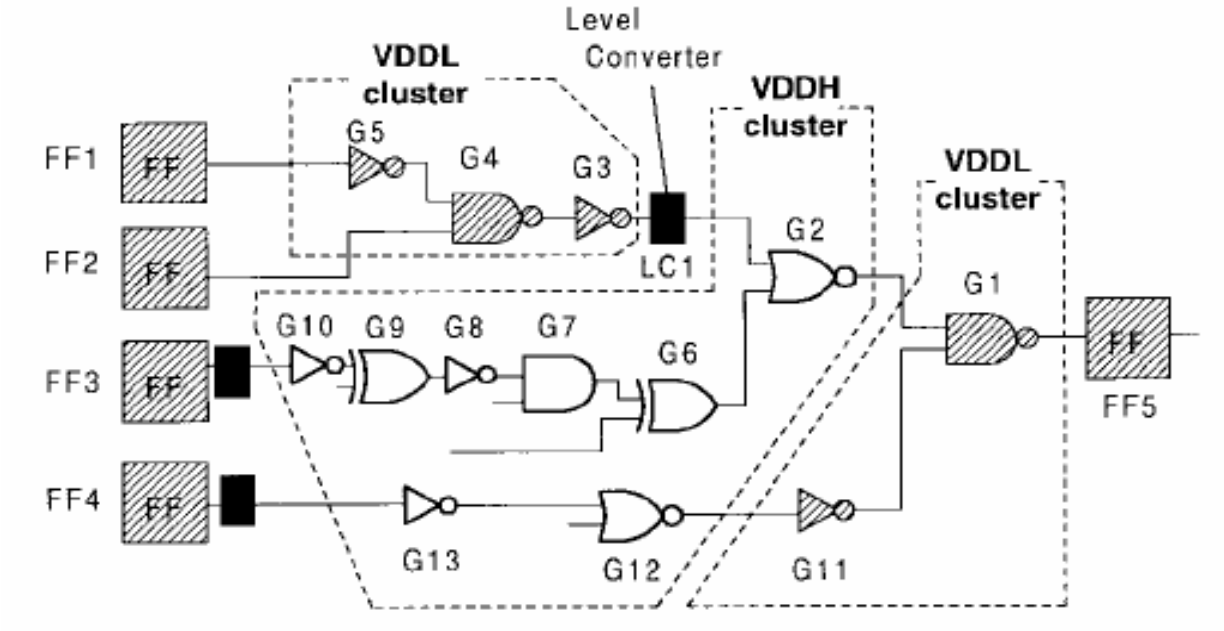



Figure 1. Extended Clustered Voltage Scaling Scheme [2]

First, the VDDL cluster grows from the rear flip-flops backward to the inner region. Until no more cells adjacent to the VDDL cluster can be merged, it stops to grow. Then a second VDDL cluster grows from the front flip-flops forward to the inner region. Similarly, it stops to grow if no more cells can be merged into this cluster.

## 2. Layout Scheme

(a). Existing approach [3] applied “Row-by-Row Power Scheme (RRPS)” to place cells with proper power supply, as shown in Figure 2.

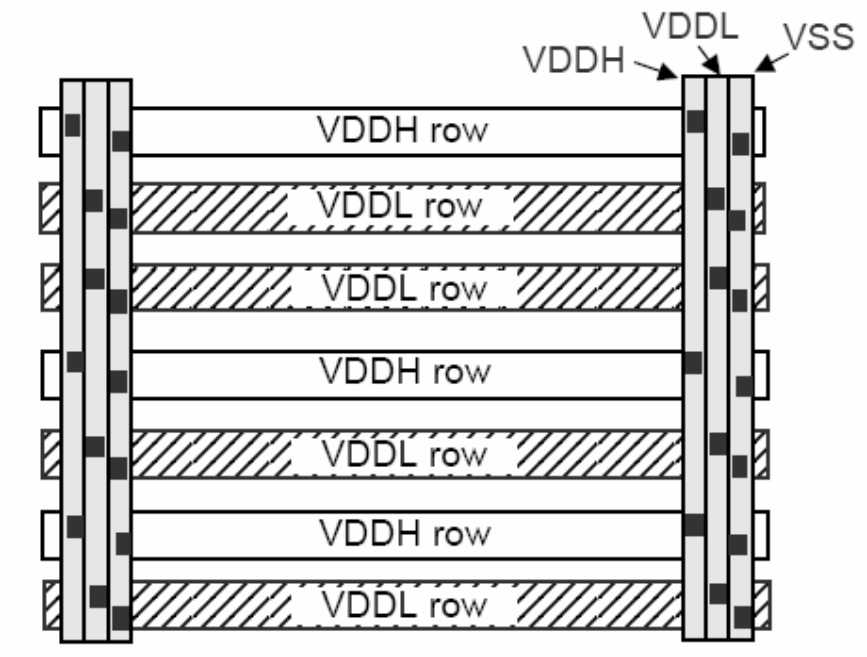



Figure 2. Row-by-Row Power Scheme [3]

The cells are firstly assigned with supply voltage level by ECVS and then placed by a min-cut placer. The voltage level assigned to each row is determined by the larger part of cells placed on it, as shown in Figure 3.

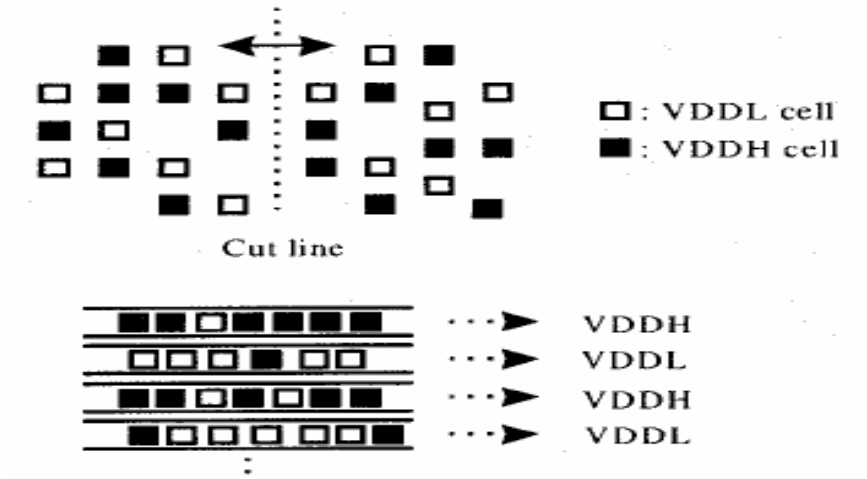
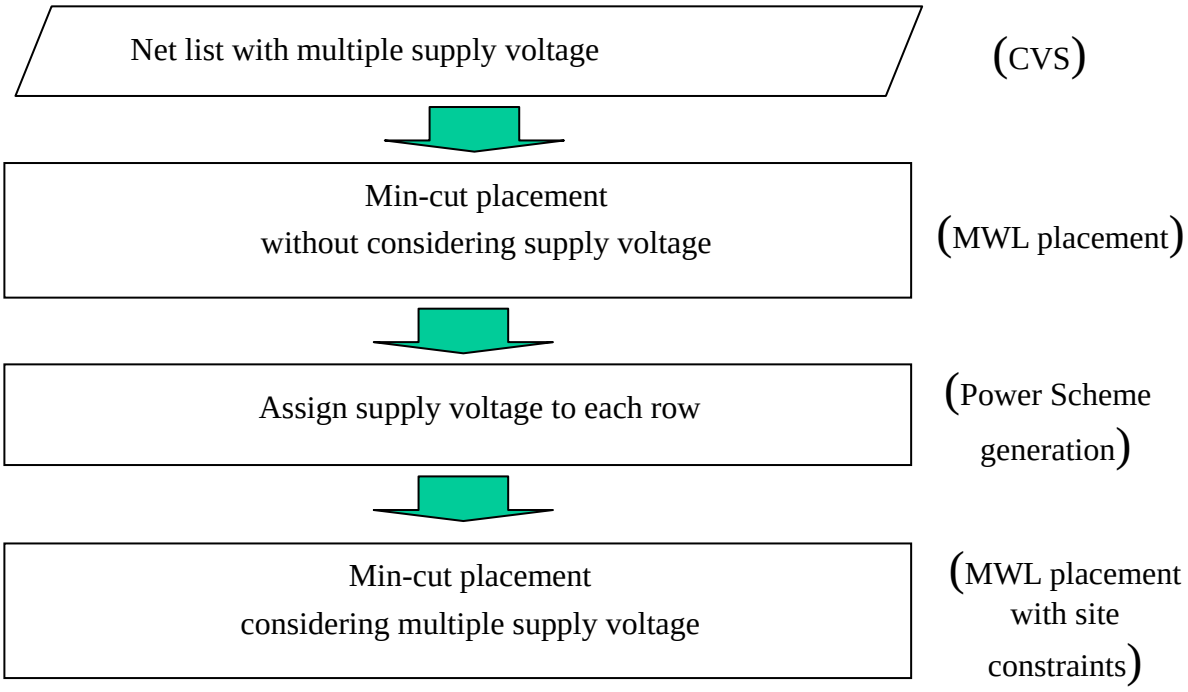



Figure 3. Generation of Row-by-Row Power Scheme [3]

This scheme would sacrifice much total wire-length, especially the ratio of the number of VDDH rows to VDDL rows is far from balance. The algorithm flow is as follows.




(b). [4] provided another layout scheme as shown in Figure 4.

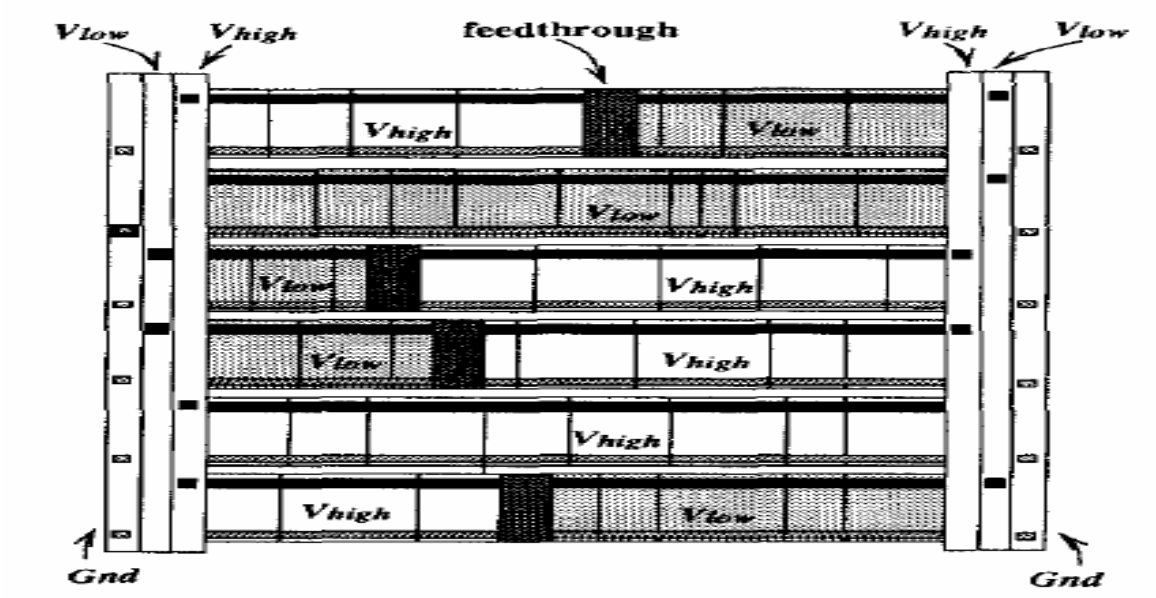



Figure 4. Dual Supply Voltage Layout Scheme [4]

Cells were swapped with Simulated Annealing algorithm to achieve lower wire-length penalty. The wire-length and core size are increased by about 10% relative to traditional SA using single supply voltage. This power scheme, using separated row, is supposed to be better than the above one (RRPS).

Both of the above two power schemes suffer another problem: the fan-out load of each cell

is inconsistent with CVS. Timing violation may occur due to this inconsistence. Some extra process such as gate re-sizing or buffer insertion is necessary. These extra processes, however, may induce cell overlapping and cause problem in algorithm closure.

## 四、研究方法 (Proposed method)

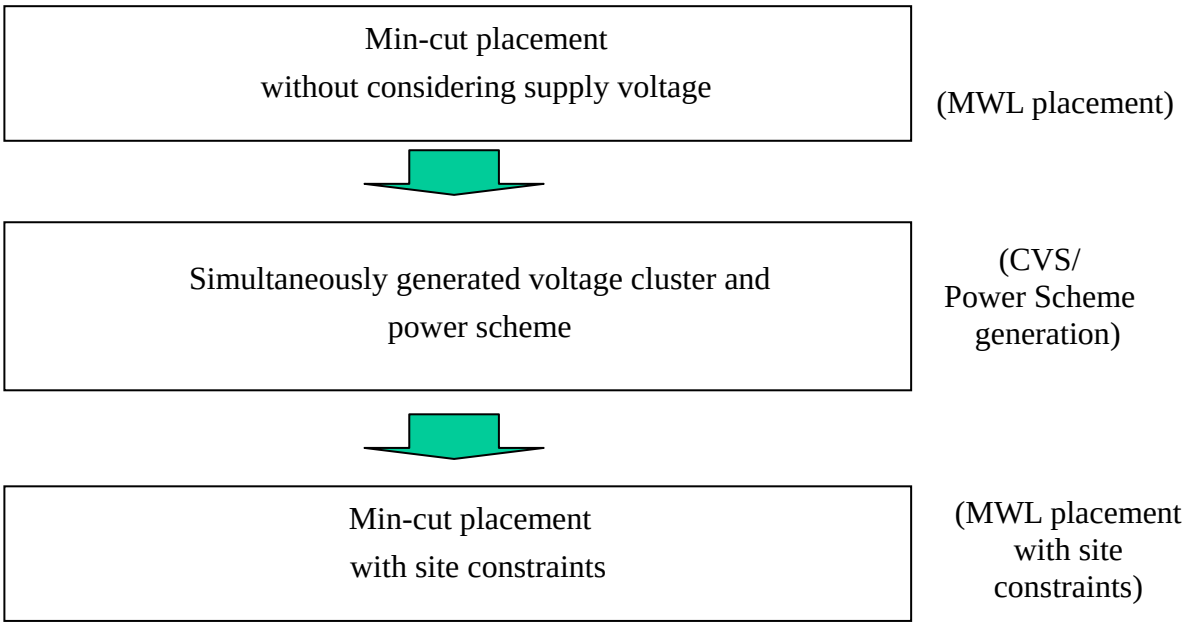
**Main algorithm:**

Step1: To achieve shorter overall wire-length, we first place the cells with traditional minimum wire-length placer before applying CVS.

Step2: Apply CVS after the first placement. The result is consistent with actually wire-loading. At the same time, simultaneously perform power supply scheming so that the power scheme and CVS are consistent with each other.

Step3: Re-place the cell with site constraints determined by the power scheme generated in step2.

The new algorithm flow is:



## 五、結論與討論(Conclusion and Discussion)

We have described a new methodology for dual-VDD low power design and it is an enhanced version from last year's result. Our method can reduce the power dissipation with good power routability and proper wire-length. The amount of power-saving depends on the netlist topology and the given timing constraints, ranging from 5% to 40%.

## 六、研究方向 (Future work)

Switching activity is an important factor in analyzing power dissipation. Many researches explore new methods to save power consumption through scheduling for low power or shutting down the circuit parts into sleep mode. Once we can apply the switching activity factor into optimization analysis, the optimality is more ensured. We can also plan for better power schemes considering current density on power rails or chip power density. Moreover, the information about switching activity can also help for analyzing glitches, which is an important source of dynamic power consumption. Our future work lies at integrating the switching activity factor into power optimization to reduce the dynamic power consumption by reducing glitches.

## 七、參考文獻(References)

[1] Usami, K. and Horowitz, M. "Clustered voltage scaling technique for low-power design," International Symposium on Low Power Design, 1995, pp. 3-8

[2] Kimiyoshi Usami, Mutsunori Igarashi, Fumihiro Minami, Takashi Ishikawa, Masahiro Kanazawa, Makoto Ichida, and Kazutaka Nogami, "Automated Low-Power Technique Exploiting Multiple Supply Voltages Applied to a Media Processor," IEEE JSSC, Volume 33, Issue 3, March 1998, pp.463 – 472

[3] Mutsunori Igarashi, Kimiyoshi Usami, Kazutaka Nogami, Fumihiro Minami, Yukio Kawasaki, Takahiro Aoki, Midori Takano, Chiharu Mizuno, Takashi Ishikawa, Masahiro Kanazawa , Shinji Sonoda, Makoto Ichida and Naoyuki Hatanaka, "A Low-power Design Method Using Multiple Supply Voltages," IEEE ISLPED, pp.36-41, 1997

[4] Chingwei Yeh and Yin-Shuin Kang, "A Simulated Annealing Based Method Supporting Dual

Supply Voltages in Standard Cell Placement," IEEE ISCAS 1999, pp. 310 - 313

[5] Masafumi Takahashi et.al., "A 60mW MPEG4 Video Codec Using Clustered Voltage Scaling with Variable supply-Voltage Scheme," IEEE JSSC, Volume 33, Issue 11, Nov. 1998 Page(s):1772 – 1780

[6] Kimiyoshi Usami, Mutsunori Igarashi, Takashi Ishikawa, Masahiro Kanazawa, Masafumi Takahashi, Mototsugu Hamada, Hideho Arakida, Toshihiro Terazawa and Tadahiro Kuroda, "Design Methodology of Ultra Low-power MPEG4 Codec Core, Exploiting Voltage Scaling Techniques," Design Automation Conference, 1998. Page(s):483 - 488

[7] Yi-Jong Yeh, Sy-Yen Kuo, Jing-Yang Jou, "Converter-Free Multiple-Voltage Scaling Techniques for Low-Power CMOS Digital Design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 20, Issue 1, Jan. 2001 Page(s):172 – 176

[8] J.-Y.Jou, D.-S.Chou, "Sensitisable-path-oriented clustered voltage scaling technique for low power," IEE Computers and Digital Techniques, Proceedings-Volume 145, Issue 4, July 1998 Page(s):301-307

[9] Sarvesh H Kulkarni, Ashish N Srivastava, Dennis Sylvester, "A New Algorithm for Improved VDD Assignment in Low Power Dual VDD systems," Proceedings of International Symposium on Low Power Electronics and Design, 2004 Page(s):200 – 205

[10] David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn, "Managing Power and Performance for System-on-Chip Designs using Voltage islands," IEEE/ACM ICCAD 2002.10-14 Nov. 2002 Page(s):195 – 202

[11] K. Joe Hass David F. Cox, "Level Shifting Interfaces for Low Voltage Logic," 9th NASA Symposium on VLSI Design 2000

[12] Fujio Ishihara1, Farhana Sheikh, Borivoje Nikoli, "Level Conversion for Dual-Supply Systems," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 12, Issue 2, Feb. 2004 Page(s):185 – 195

[13] James T. Kao, Anantha P. Chandrakasan, "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE Journal of Solid-State Circuits, Volume 35, Issue 7,

July 2000 Page(s):1009 - 1018

[14] Koichi Nose, Takayasu Sakurai, “Optimization of VDD and VTH for Low-Power and High-Speed Applications,” IEEE Asia and South Pacific Design Automation Conference 2000 (ASP-DAC'00), Pages: 469 - 474

[15] Anirban Basu, Sheng-Chih Lin, Vineet Wason, Amit Mehrotra,Kaustav Banerjee, “Simultaneous Optimization of Supply and Threshold Voltages for Low-Power and High-Performance Circuits in the Leakage Dominant Era,” Design Automation Conference, 2004. Page(s):884 – 887

[16] Takayasu Sakurai, “Reducing Power Consumption of CMOS VLSI's through Vdd and Vth Control,” IEEE International Symposium on Quality of Electronic Design, 2000

[17] Ricardo Gonzalez, Benjamin M. Gordon, and Mark A. Horowitz, “Supply and Threshold Voltage Scaling for Low Power CMOS,” IEEE JSSC, vol. 32, no. 8, August 1997

[18] Tanay Karnik, Yibin Ye, James Tschanz, Liqiong Wei, Steven Burns, Venkatesh Govindarajulu, Vivek De, Shekhar Borkar, “Total Power Optimization By Simultaneous Dual-Vt Allocation and Device Sizing in High Performance Microprocessors,” Proceedings of Design Automation Conference, 2002.10-14 June 2002 Page(s):486 – 491

[19] W. Hung, Y. Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin and Y. Tsai, “Total Power Optimization through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing with Stack Forcing,” IEEE International Symposium on Low Power Electronics and Design, 2004.Page(s):144 - 149