BST 介電薄膜在 12 吋矽晶圓上快速熱回火製程中熱物理性質及熱應力之研究（I）

Study on the Thermal Properties and Stresses of a 12-inch Silicon Wafer with High-dielectric BST Thin Films in Rapid Thermal Processing/Annealing（I）

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中文摘要

本研究第一年主要提出一種逆向模式之數值演算法以便能計算快速熱製程（RTP）中使得晶圓上溫度均勻所需之晶圓邊緣的熱補償，進而降低過程中所產生的熱應力。考慮矽晶圓熱物理性質隨溫度而變化，並採用含未來溫度演算法的逆解熱傳方法。結果顯示，晶圓上溫度均勻所需的照射熱通量可直覺地、有效地經由此逆向模式評估計算出來。假若快速加熱系統能根據此逆向方法來動態控制晶圓上照射的熱通量，本文顯示晶圓上溫度的不均勻性將大大地降低。

由於快速熱製程的加熱光源系統只對矽晶片選擇性吸熱的特殊性，過程中改變晶圓片之輻射頻譜（例如，沈積或成長於晶片表面或背面之絕緣層或導電層），可能在晶圓上產生不均勻的溫度分佈。本研究第一年之實驗，應用傅氏轉換紅外線頻譜儀(FTIR)對常溫中的矽晶圓以及具 BST 介電薄膜的矽晶圓，做其熱輻射性質的量測。

關鍵詞：快速熱製程，矽晶圓，溫度均勻，輻射性質

Abstract

First year, a numerical inverse-modeling algorithm was developed in the present study which was able to calculate optimal edge-heat compensations on wafers sequentially during rapid thermal processing in order to obtain temperature uniformity across wafers. The temperature-dependent thermal properties of silicon and a future-time algorithm of inverse heat-transfer method are used. Our numerical results show that temperature uniformity can be efficiently achieved using inverse modeling and reveal that the thermal non-uniformity can be reduced considerably if the incident heat fluxes on the wafer can be dynamically controlled according to the results calculated by the inverse methods.

First year, measurements of spectral emissivity of silicon wafers were presented. The p-type and heavily doped silicon wafer with front side polished as well as (Ba,Sr)TiO_3 [BST] thin film on silicon wafer had been carried out using Bomem Michelson series MB-154 FTIR spectrometer at room temperature. The effects of BST thin film and oxide on silicon wafer were to reduce the transmittance significantly.

Keywords: rapid thermal processing (RTP), silicon wafer, temperature uniformity, thermal radiative properties

1. Introduction

As device dimension shrinks to the sub-micrometer range, reduction of thermal budget during microelectronic processing is becoming a crucial issue. Single wafer rapid thermal processing has become an alternative to the conventional furnace-based batch processing in many processes. Temperature uniformity across the wafer during all processing continues to be a main obstacle for full acceptance of RTP into manufacturing [1].

Many approaches including patterned susceptor [2] and model-based control [3-5] have been proposed for achieving temperature uniformity. Certain of these approaches rely largely on trial-and-error, which can be quite expensive and time-consuming. This study primarily deals with the determination of edge-heat compensations from heaters to eliminate radial temperature gradients across wafers [6-9] and presents an efficient way using inverse heat transfer method to determine edge-heat compensation intuitively to ensure temperature uniformity during RTP.

A change in spectral distribution of the radiative properties of the wafer is a source of temperature non-uniformity for RTP systems [10]. The details of the spectral features relevant in the design of RTP systems have been in the articles of Roozeboom [11]. The continuing development of RTP techniques requires a detailed understanding of the thermal radiative properties of semiconductor wafers. The most fundamental is the spectral emissivity. It is necessary to know the total hemispherical emissivity of the wafer to calculate the equilibrium temperature it will reach when irradiated with a given power density.

2. Analysis

2.1 Thermal Model

Consider the axially symmetrical wafer shown in Fig. 1. Let l and $¢$ be the radius and thickness, respectively. T_0 is the initial temperature, and the ambient temperature is T_a. Usually, incoherent lights irradiate the wafer from both sides. The total incident heat fluxes on the top and the bottom surfaces are represented by q_{top} and q_{bottom}, respectively. q_{edge} denotes total lateral edge-heat compensations impinging on the edges. All surfaces incur radiant heat losses. The process is considered to operate in a vacuum so heat transfer due to convection can be ignored. Assume that the temperature is uniform through the wafer thickness. Thus a one-dimensional thermal model may be adopted.

The governing equation for an axially symmetric cylindrical coordinate system with its origin at the center is

$$°c(T)\frac{\partial T}{\partial t}=\frac{1}{r}\frac{\partial}{\partial r}\left[k(T)r\frac{\partial T}{\partial r}\right]+\frac{1}{¢}\left[G_{top}+G_{bottom}\right],\quad 0<r<l \quad (1)$$

with

$$G_{top}=\sim_{top} q_{top}(r,t)-£_{top}\pm_s(T^4-T_a^4),$$

$$G_{bottom}=\sim_{bottom} q_{bottom}(r,t)-£_{bottom}\pm_s(T^4-T_a^4),$$

where $\pm_s$ =5.672 × 10^{-12} $Wcm^{-2}K^{-4}$ is the Stefan-Boltzmann constant, the temperature T is a function of radius r, and time t, and $°$, $k(T)$, $c(T)$, $\sim_{top}$, $£_{top}$, $\sim_{bottom}$, and $£_{bottom}$ are the density, thermal conductivity, specific heat capacity,

absorptivity of the top side, emissivity of the top side, absorptivity of the bottom side, and emissivity of the bottom side, respectively. Because of its large temperature variation during processing, the temperature dependence of the thermal conductivity as well as the specific heat capacity of silicon are considered as follows [1]:

$$k(T) = 802.99\, T^{-1.12} \quad (\mathrm{W\ cm^{-1}\ K^{-1}}) \qquad 300\text{-}1683\ \mathrm{K} \quad (2a)$$

$$c(T) = 0.641 + 2.473 \times 10^{-4}\, T \quad (\mathrm{J\ g^{-1}\ K^{-1}}) \qquad >300\ \mathrm{K} \quad (2b)$$

while the density is assumed to be constant and equal to 2.33 g $\mathrm{cm^{-3}}$. Since the disk is considered to be homogeneous, the dependence of $k(T)$ on spatial position is addressed only implicitly by the spatial dependence of the temperature. Because $k(T)$ is weakly dependent on temperature (see Fig. 2), spatial temperature variations across the disk at specific times are expected to be small enough ($\leq$ 200K) so that spatial variations in thermal conductivity may be ignored [6]. Eq. (1) is thus reduced to

$$\rho c(T)\frac{\partial T}{\partial t} = k(T)\left[\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r}\right] + \frac{1}{\phi}\left[G_{top} + G_{bottom}\right]. \quad 0 < r < l \quad (3)$$

The initial and boundary conditions for the system mentioned above are

$$T(r,t) = T_0 \qquad \text{at} \quad t = 0 \quad (4)$$

$$\frac{\partial T}{\partial r} = 0 \qquad \text{at} \quad r = 0 \quad (5)$$

$$-k(T)\frac{\partial T}{\partial r} = \varepsilon_{edge}\, q_{edge}(t) + \varepsilon_{edge}\sigma_s\left(T^4 - T_a^4\right), \quad \text{at} \quad r = l \quad (6)$$

where ε_{edge} and ε_{edge} are the absorptivity and emissivity of the wafer edge, respectively. We may assume without loss of generality that the incident heat flux on both sides during processing are equal, i.e. $q_{top}(r,t) = q_{bottom}(r,t) = q(r,t)$, and that the absorptivities of all surfaces are the same as the emissivities of those surfaces. For simplicity, the emissivities of all surfaces are assumed to be the same and temperature-dependent only in as much as [12]:

$$\varepsilon_{top} = \varepsilon_{top} = \varepsilon_{bottom} = \varepsilon_{bottom} = \varepsilon_{edge} = \varepsilon_{edge} = \varepsilon(T)$$
$$= 0.2662 + 1.8591\, T^{-0.1996} e^{-\frac{1.0359\times 10^{-5}}{T^{0.5328}}} \quad . \quad (7)$$

Thus, Eqs. (3) and (6) may be written as, respectively,

$$\rho c(T)\frac{\partial T}{\partial t} = k(T)\left(\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r}\right) + \frac{2}{\phi}\varepsilon(T)\left[q(r,t) - \sigma_s(T^4 - T_a^4)\right]$$
$$0 < r < l \quad (8)$$

and

$$-k(T)\frac{\partial T}{\partial r} = \varepsilon(T)\left[q_{edge}(t) + \sigma_s\left(T^4 - T_a^4\right)\right]. \qquad \text{at} \quad r = l \quad (9)$$

A central-difference representation of the space derivative and an implicit backward-difference representation of the time derivative are adopted. We can approximate the governing equation and the initial condition as well as the boundary conditions using $T(r,t) = \theta((i-1)\Delta R, n\Delta\tau) = \theta_i^n$, with a p equi-distant grid (the spatial coordinate increment $\Delta R = l/p$) and the temporal coordinate increment $\Delta\tau$. After the nonlinear radiant fourth-power terms in Eqs. (8) and (9) have been simulated using a linear scheme and the SOR-by-lines method has been adopted, the unknowns in the subgroups to be modified simultaneously are set up such that the matrix of coefficients will be tridiagonal in form permitting use of the Thomas algorithm as follows:

$$b_i^n \theta_{i-1}^n + d_i^n \theta_i^n + a_i^n \theta_{i+1}^n = c_i^n . \quad (10)$$

The superscripts refer to the temporal grid and the subscripts refer to the spatial grid.

2.2 Inverse Heat Transfer Method

Without loss of generality, the total absorbed powers are assumed to be controlled such that the center of the wafer follows the center temperature trajectory calculated from the direct thermal model given above using uniform heat flux without any edge-heat compensation.

The finite-difference method in the thermal model above at $\tau = \tau^m = m\Delta\tau$ was used to construct the following matrix equation [13]:

$$\left[F^m\right]\left\{\theta^m\right\} = \left\{\theta^{m-1}\right\} + \left\{S^m\right\} + \left[V^m\right]\left\{\psi^m\right\}, \quad (11)$$

where $\left[F^m\right]$ ontains the coefficients a_i^m, b_i^m, and d_i^m described in the thermal model above. The $\left\{S^m\right\}$ vector includes all known variables of the problem and the $\left[V^m\right]$ matrix contains the coefficients for the edge-heat compensation vector $\left\{\psi^m\right\}$.

The temperature distribution $\left\{\theta^m\right\}$ can then be derived from Eq. (11) as follows:

$$\left\{\theta^m\right\} = \left[F^m\right]^{-1}\left\{\left\{\theta^{m-1}\right\} + \left\{S^m\right\}\right\} + \left[F^m\right]^{-1}\left[V^m\right]\left\{\psi^m\right\}$$
$$= \left[M^m\right]\left\{\left\{\theta^{m-1}\right\} + \left\{S^m\right\}\right\} + \left[N^m\right]\left\{\psi^m\right\} \quad , \quad (12)$$
$$= \left[M^m\right]\left\{\left\{\theta^{m-1}\right\} + \left\{S^m\right\}\right\} + \left[N^m\right]\left\{u_{p+1}\right\}\psi_{p+1}^m$$

where $\left[M^m\right] = \left[F^m\right]^{-1}$ and $\left[N^m\right] = \left[F^m\right]^{-1}\left[V^m\right]$. The vector $\left\{\theta^{m-1}\right\}$ contains the $p+1$ values of the initial distribution or the temperature distribution at the preceding time step. $\left\{u_{p+1}\right\}$ is a unit column vector with a unit at the $(p+1)th$ component. ψ_{p+1}^m denotes the unknown edge-heat compensation required to achieve temperature uniformity during processing. By same means, for the next time step $m+1$ and at successive r future times [14], $\tau = \tau^{m+r-1}$ we can also arrived. It was temporarily assumed that the edge-heat compensation was constant over r future time steps. The temperatures θ_i^{m+k} at each i-spatial grid ($i = 1, 2, \Lambda, p, p+1$) for each analysis interval $k = 0, 1, 2, \Lambda, r-1$ could then be derived [15]. Thus, we were able to construct the following matrix equation

$$\{g\}_{r(p+1)\times 1} = \{\Phi\}_{r(p+1)\times 1}\psi_{p+1}^m . \quad (13)$$

After the known temperature distributions were substituted into vector g, the unknown edge-heat compensation ψ_{p+1}^m could be found using the linear least-squares-error method. The inverse result was

$$\psi_{p+1}^m = (\Phi^T\Phi)^{-1}\Phi^T g . \quad (14)$$

3. Experiments

A Bomem Michelson series MB-154 FTIR spectrometer was used to collect the emission. In measuring the reflectance and transmittance of a wafer, an integrating sphere is used in the sample compartment of the FTIR system to collect all the reflecting or scattering light. For measuring transmittance, the wafer is put on the sample holder, and then locked between the incident light source and the integrating sphere. But for reflectance, the wafer is put beyond the integrating sphere. Spectra are then recorded from 1.1 to 5.5 μm with a resolution of 4 $\mathrm{cm^{-1}}$ resolution and in averaging of 20 scans.

4. Results and Discussion

4.1 Temperature Uniformity of Silicon Wafers during RTP

The sequential algorithms described above were employed in numerical experiments with 100-, 150-, 200- and 300-mm-diameter silicon wafers, respectively, 0.6-, 0.675-, 0.725- and 0.775 mm thick. A heating simulation from an initial

temperature of T_0 =27°C (300K) transitioning to a steady state of 1097°C (1370K) was demonstrated for an ambient temperature of T_a =27°C (300K) under a uniform incident heat flux from the kaleidoscopic light pipe of $q(r,t)$ =20 W/cm^2. The center temperature and ramp-up rate of the 300-mm-diameter 0.775-mm-thick silicon wafer was calculated using the finite-difference scheme during this temperature transition without any edge-heat compensation, as shown in Fig. 3. Fig. 4 shows temperature differences across the 300-mm-diameter 0.775-mm-thick silicon wafer during this thermal processing. The greatest temperature difference during processing, 25°C occurred. Additional edge-heat compensation(s) may be required to eliminate radial temperature gradients across the wafer. The calculated temperature profile of the center shown in Fig. 3 was adopted as our desired uniform temperature track.

Figs. 5(a) and 5(b) show the vertical and lateral edge-heat-compensation-scaling factor obtained from inverse method for 100-, 150-, 200- and 300-mm-diameter silicon wafer, respectively. In Fig. 5(a), the required vertical edge-heat-compensation ratios are increased from 1.0 initially to 1.60, 1.45, 1.37 and 1.26, respectively at the higher steady state periods for the 100-, 150-, 200- and 300-mm-diameter wafers. While in Fig. 5(b), the required lateral edge-heat-compensation ratios increased from zero initially to 1.0 at higher steady state periods for all four wafers.

Figs. 6(a) and 6(b) show temperature difference calculated using inverse method of a 300-mm-diameter 0.775-mm-thick silicon wafer with vertical and lateral edge-heat compensation to control temperature uniformity. Comparing with Fig. 4, we see that the maximum temperature difference was reduced from 25°C to 0.178°C. Fig. 7 shows the temperature differences obtained by inverse method during thermal processing. The maximum temperature differences were 0.279, 0.583, 0.989 and 0.178°C for 100-, 150-, 200- and 300-mm-diameter silicon wafers, respectively.

4.2 Spectral Emissivity Measurement of Silicon Wafers

Fig. 8 show the measured results for reflectance, transmittance and emittance of 5 inches (0.78mm thickness) p-type, heavily doped silicon wafer with front side polished at room temperature in wavenumbers between 10000 and 2000 cm^{-1}. It is found that reflectance and transmittance are always 40% and 50%, respectively, smaller than 8000 cm^{-1} in both wafers. So, the emittance exists only between 10000 and 8500 cm^{-1} at room temperature. According to Sato's works [16], in the visible region, the emissivity is fairly high, since the direct and indirect of band-to-band transitions occur at this spectral region. And, at low temperatures, the wafer is transparent for the wavelengths longer than 1.2 μm (wavenumbers smaller than 8300 cm^{-1}), hence the emissivity is very low in near infrared. Comparing to our measurement results, it reveals that the present results are principally in good agreement with the Sato's work. It also has the evidence in comparison to the measured works of a lighted n-type doped silicon wafer (polished both sides) at 30°C by Ravindra et al. (ref. in Fig. 3, [17]). Those measured reflectance, transmittance and emittance are close to our present measurement results.

High-dielectric-constant (Ba,Sr)TiO_3 (BST) has emerged as the preferred high permittivity thin film material for future generations of high-density Gb-scale DRAM products. The application of rapid thermal annealing (RTA) might increase the crystallinity of the BST films, which resulted in improved dielectric properties of the film [69]. Fig. 9 shows the measured results for reflectance, transmittance and emittance of 2241Å-thick ($Ba_{0.7}Sr_{0.3}$)TiO_3 (1433Å-thick SiO_2), thin film on silicon wafer with front side polished at room temperature in wavenumbers between 10000 and 1000 cm^{-1}. Comparing Fig. 9 with Fig. 8, the measured results reveal that the effects of BST thin film and oxide on silicon wafer are to reduce the transmittance significantly. It was similar to the measured works of 5124Å-thick SiO_2 on silicon wafer at 58°C by Ravindra et al. (ref. in Fig. 7, [17]). Those measured reflectance, transmittance and emittance for silicon wafer with thin films are close to our present measurement results.

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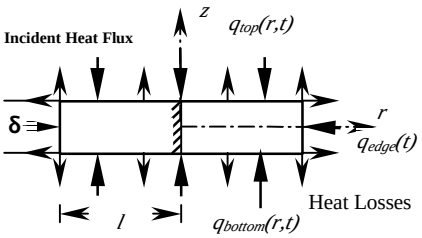

Fig. 1: Schematic representation of energy flux in a wafer under incident heat flux and radiant heat losses emitted from all surfaces

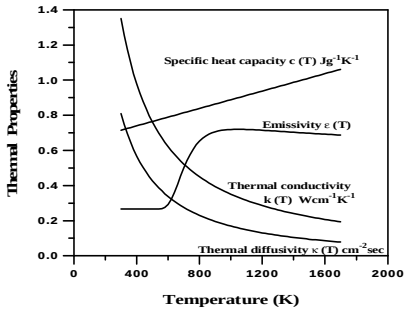

Fig. 2: Temperature-dependent thermal properties of silicon

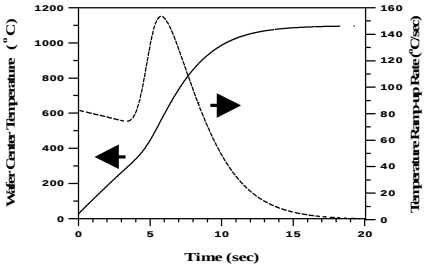

Fig. 3 Center temperature and ramp-up rate during processing

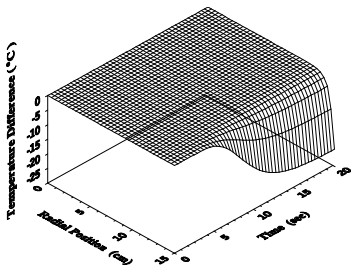

Fig. 4 Temperature differences during processing under uniform heat fluxes without any edge-heat compensations

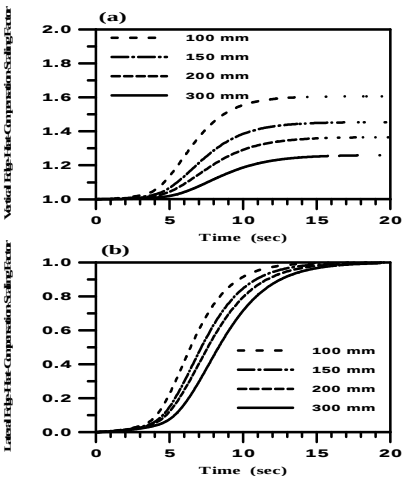

Fig. 5 (a) Vertical (b) Lateral edge-heat-compensation-scaling factor required for temperature uniformity calculated by inverse methods

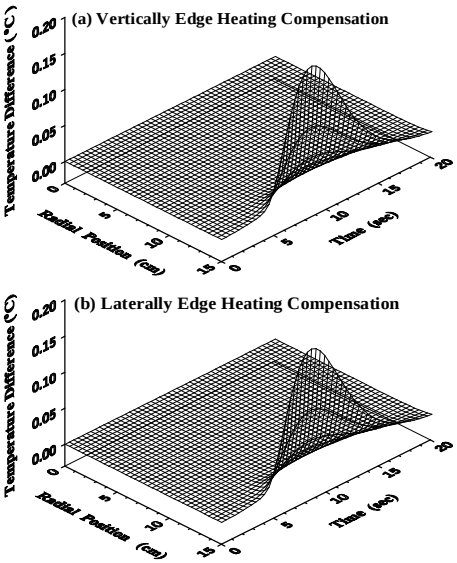

Fig. 6 Temperature differences during processing with (a) vertical (b) lateral edge-heat compensations calculated by inverse methods

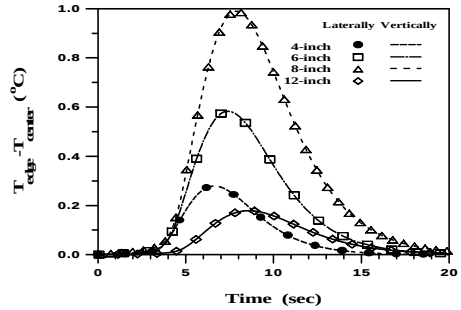

Fig. 7 Temperature differences between centers and edges during processing of 100-, 150-, 200- and 300-mm-diameter wafers with vertical and lateral edge-heat compensations calculated by inverse methods

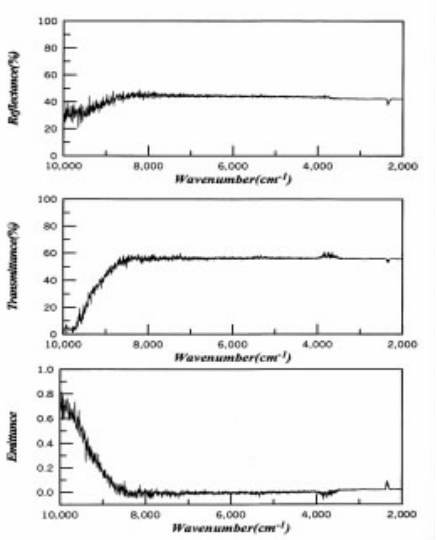

Fig. 8 Measured results for reflectance, transmittance and emittance of 5 inches (0.78mm thickness) p-type, heavily doped silicon wafer with front side polished at room temperature.

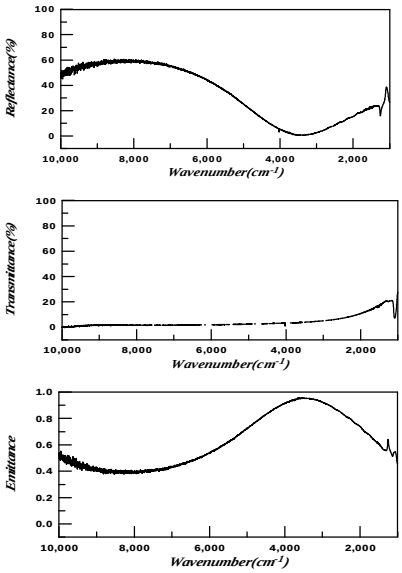

Fig. 9 Measured results for reflectance, transmittance and emittance of 2241Å-thick $(Ba_{0.7}Sr_{0.3})TiO_3$ (1433Å-thick SiO_2) silicon wafer with front side polished at room temperature.