行政院國家科學委員會專題研究計畫　成果報告

子計畫一：矽射頻元件模型與技術(3/3)

計畫類別： 整合型計畫
計畫編號： NSC93-2215-E-009-009-
執行期間： 93 年 08 月 01 日至 94 年 07 月 31 日
執行單位： 國立交通大學電子工程學系暨電子研究所

計畫主持人： 荊鳳德

報告類型： 完整報告

處理方式： 本計畫可公開查詢

中　華　民　國 94 年 8 月 2 日

行政院國家科學委員會補助專題研究計畫■成果報

告　□期中進度報告

（計畫名稱）

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計畫參與人員：

成果報告類型(依經費核定清單規定繳交)：□精簡報告 ■完整報告

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中　華　民　國　九十四　年　七　月　十一　日

一、 中文摘要

本計畫主要研究 16 根閘極數之 0.18 μm 矽射頻元件在矽基板薄化至 30 μm 黏構至塑膠基板上之雜訊、增益效應。而發現最低之雜訊取得其值為 1.1 dB 和增益值為 12 dB，由於其薄化之矽基板，使矽射頻元件有獨特的應力效應產生，進而，增加 25% 元件的汲極電流及降低元件中雜訊至 0.92 dB，此外，此極佳的張力效果不僅只應用在 0.18um 之矽射頻元件，未來也可適用於 0.13um 之矽射頻元件於塑膠基板中。

關鍵詞: 射頻雜訊，增益，金氧半電晶體，塑膠。

二、 英文摘要

A low minimum noise figure (NFmin) of 1.1 dB and high associated gain of 12 dB at 10 GHz were measured for 16 gate fingers 0.18 μm RF MOSFETs after thinning down Si substrate to 30 μm and subsequent mounting on plastic. Owing to the high flexibility of 30 μm Si substrate on plastic, the device performance can be further increased by applying a tensile stress with higher 25% enhancement in saturation drain current and lower NFmin to only 0.92 dB at 10 GHz. These excellent results of mechanical tensile strained 0.18 μm RF MOSFETs on plastic are comparable with 0.13 μm node (Lg=80nm) devices.

關鍵詞: RF Noise, associated gain, MOSFET, plastic.

三、 報告內容：

甲、 前言：

Si RF MOSFETs [1]-[8] are now widely used for wireless communication due to the continuously improved RF noise and high frequency gain with down-scaling technology. However, the major challenge of Si RF IC is the poor RF loss from low resistivity (10 Ω-cm) Si substrate [9]-[11] that substantially degrades passive component performance. One of the solutions is to integrate the Si RF ICs on high-insulating plastic [12], where much better performance of RF passive devices can be realized on low cost plastic substrate. To further utilize the flexible property of plastic substrate, in this paper we have applied a tensile strain to improve the RF performance of Si MOSFETs. After thinning down Si substrate to 30 μm and subsequent mounting on plastic, the standard 0.18μm Si MOSFET shows a low 1.1 dB minimum noise figure (NF_{min}) and a high 12 dB associate gain at 10 GHz. After applying a ~0.7% longitudinal tensile strain mechanically, the same device on plastic shows improved RF performance of a very low 0.92 dB NF_{min} and a high 14 dB associated gain at 10 GHz. Such large RF performance improvement is a consequence of thinner substrate and is due to the 25% higher saturation drive current under tensile strain [13]-[14] that is inversely proportional to substrate thickness (t_{sub}) by $1/t_{sub}^2$

relation. These excellent RF performance of 0.18μm Si MOSFET on plastic, by simple mechanical stress, compares well with 0.13μm node device (L_g=80nm) [5]-[6] giving a full technology generation advantage and is the strong merit for low cost thin-Si body flexible electronics on plastic

乙、 研究方法

Multiple gate fingers 0.18 μm MOSFETs with novel microstrip line layout [8] were used to reduce the RF noise arising from the gate resistance and substrate network of the RF probing pad and the CPW line [5]-[7], [10]-[11]. Then the Si substrate was thinned down from 300 μm to 30 μm by using inductive-coupled plasma (ICP) dry etching followed by wet etching process. The die with thinned down substrate was glued onto a light-transparent polyethylene terephthalate (PET) plastic substrate shown in Fig. 1(a) and the enlarge image is in Fig. 1(b). Figure 1(c) shows a control Si substrate with 30 m thickness, where high flexibility and large surface tensile strain were obtained. These devices were characterized by DC I-V, S-parameters and NFmin measurements using an HP4155C, HP8510C network analyzer and ATN-NP5B noise parameter system, respectively.

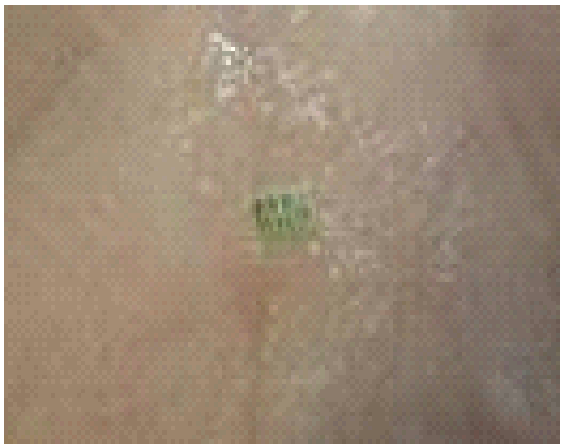

Fig.1 (a)

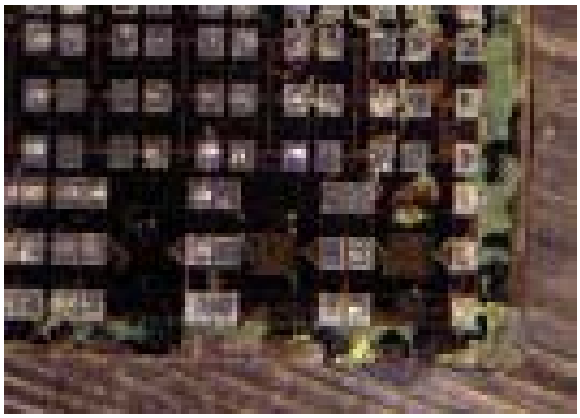

Fig.1 (b)

Fig.1 (c)

丙、 結果與討論（結論與建議）

Figure 2 shows the DC Id-Vd characteristics of 16 gate fingers 0.18 μm RF MOSFETs on VLSI-standard substrate, thinning-down to 30 μm and mounting on plastic, and further applying tensile strain. The process of thinning down the Si substrate and mounting on plastic shows little degradation on device performance as evidenced from the comparable Id-Vd characteristics with the original 0.18 μm MOSFETs. The transistor's saturation drive current can be further improved by 25%, after applying a longitudinal tensile strain of ~0.7%. Such drive current improvement is important to achieve higher operation speed of ICs, which provides an alternative method to apply the strain and enhance the device performance rather than the SiN capped strained Si [4].

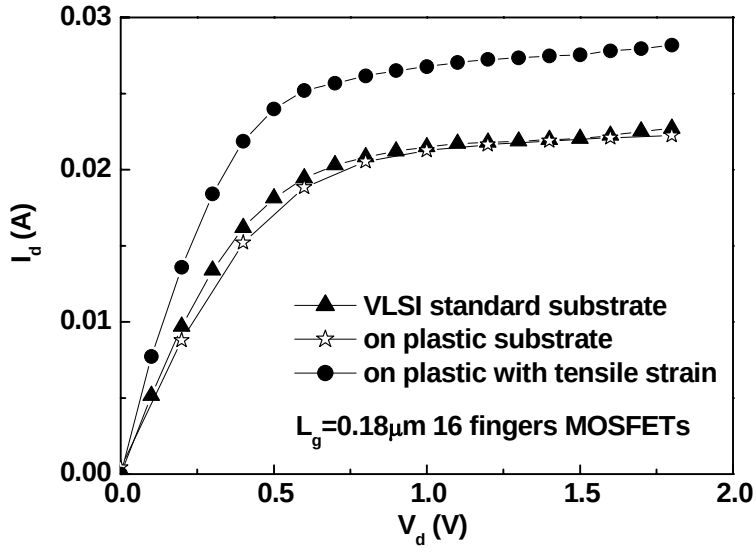

Fig.2

Figure 3 shows the plot of RF current gain ($|H_{21}|^2$) as a function of frequency of 16 gate fingers 0.18 μm MOSFETs. The $|H_{21}|2$ from the measured S-parameters follows the typical -20 dB/decade slope with increasing frequency. The $|H_{21}|^2$ of the 0.18 μm RF MOSFETs on plastic with substrate thinned down shows close value and frequency dependence with the original device with only slight degradation of unity-gain cut-off frequency (f_T) from 48.5 to 48.0 GHz. The tensile strained 0.18 μm RF MOSFETs on plastic also follows the -20 dB/dec slope with increasing frequency with gain enhancement by 1.6 dB at 10 GHz to give a higher f_T of 59 GHz. Such improvements of RF current gain and fT are consistent with the higher saturation drive current in Fig. 2, which is due to the physical effect of strain enhanced mobility.

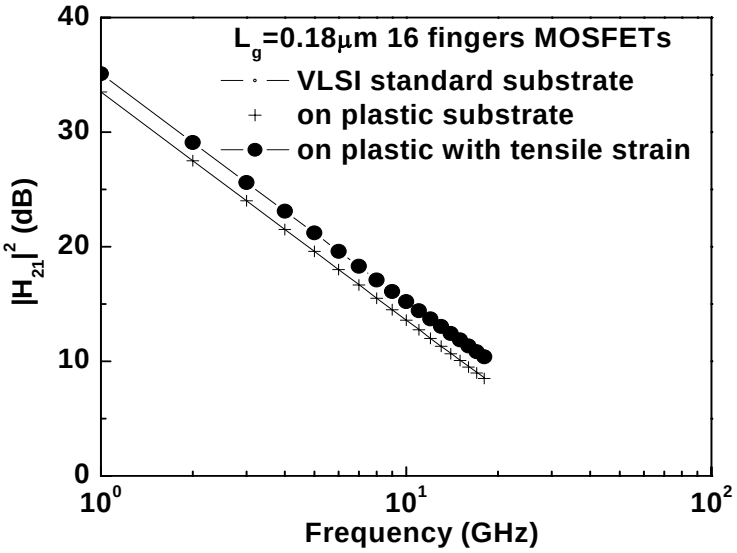

Fig.3

Figure 4(a) shows the NFmin and associated gain. At 10 GHz, the measured NFmin of 0.18 μm devices on VLSI-standard Si substrate and on plastic are 1.0 dB and 1.1 dB and associated gain are 13.5 dB and 12 dB, respectively. The slight degradation may be due to the ICP plasma thinning process. These data suggest that the RF noise and associate gain are more sensitive to substrate engineering through thinning than the DC characteristics. For the mechanical strained 0.18 μm MOSFETs on plastic, very low NFmin of 0.92 dB and high associate gain of 14 dB are obtained at 10 GHz. Such large RF noise improvement is due to the higher f_T [7] by:

$$NF_{min} = 1+2\gamma(1+ g_m R_g/\gamma)^{1/2} f/f_T \quad (1)$$

The γ is the drain current noise correlation factor and an ideal value of 2/3 used here to fit the measured NFmin shown in Fig. 4(a). These excellent results of tensile strained RF MOSFETs on plastic compare well with 0.13 μm node (Lg=80nm) devices [5]-[7] and 90nm node SiN-caped strained nMOS [4], as shown in Fig. 4(b). The low cost and high performance 0.18 μm RF MOSFETs on plastic are the strong merits for flexible electronics and important for RFID and wireless display applications.

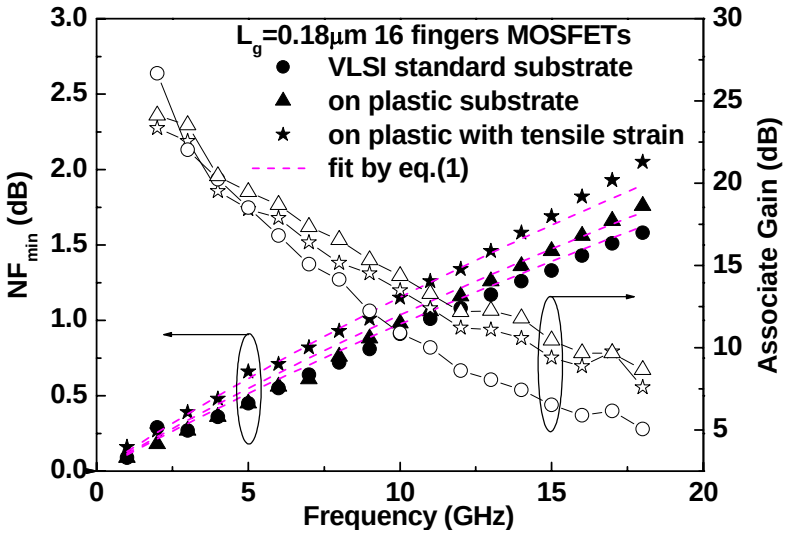

Fig.4 (a)

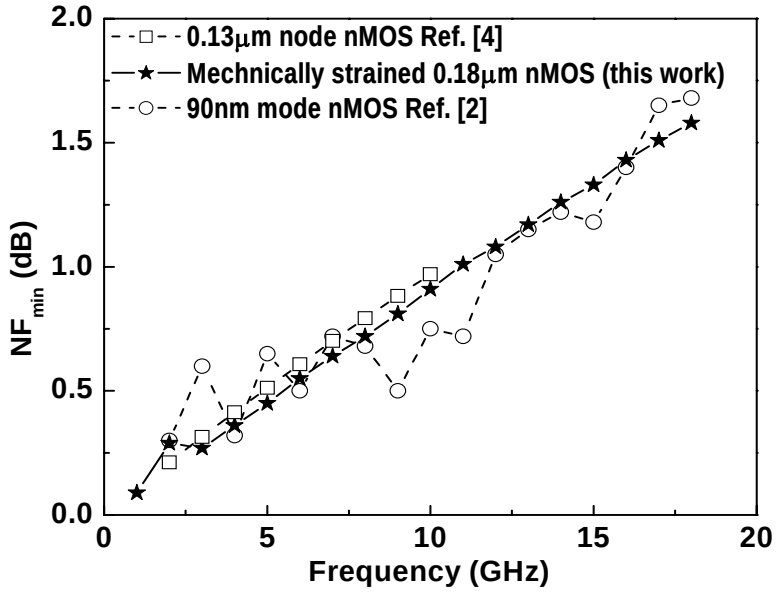

Fig.4 (b)

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五、計畫成果自評

We have successfully demonstrated high RF performance 0.18 μm MOSFETs on flexible plastic with 30 μm Si substrate. Excellent RF performance of very low 0.92 dB NF_{min}, high 14 dB associated gain and high 59 GHz f_T are simultaneously measured under applied tensile strain.