Investigation of Electrostatic Integrity for Ultrathin-Body Germanium-On-Nothing MOSFET

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***Abstract*—This paper examines the electrostatic integrity of ultrathin-body (UTB) germanium-on-nothing (GeON) MOSFET using theoretically calculated subthreshold swing from the analytical solution of Poisson's equation. Our results indicate that UTB GeON MOSFETs with the ratio of channel length (L_g) to channel thickness ($T_{\rm ch}$) around 4 can show comparable subthreshold swing to that of the silicon-on-nothing counterparts. The impact of buried insulator (BI) thickness ($T_{\rm BI}$) and BI permittivity on the electrostatic integrity of the UTB germanium channel devices are also examined.**

***Index Terms*—Electrostatic integrity, germanium, germanium-on-nothing (GeON), Poisson's equation, silicon-on-nothing (SON), ultrathin body (UTB).**

I. Introduction

GERMANIUM as a pFET channel material has been recently proposed [1]–[6] to enable mobility scaling. However, its higher permittivity makes it very susceptible to short channel effects (SCEs). To improve the subthreshold characteristics, ultrathin-body (UTB) germanium-on-insulator (GeOI) MOSFET has been proposed as a promising device architecture [7]–[10] and shows better control of SCEs than the bulk germanium MOSFET. Silicon-on-nothing [SON, buried insulator (BI) permittivity = 1] MOSFETs are also widely discussed as a possible alternative due to its reduced source-to-drain coupling through the BI [11]–[15]. However, the subthreshold characteristics of germanium-on-nothing (GeON) MOSFET have rarely been examined.

In this paper, we assess the electrostatic integrity for nanoscale UTB GeON MOSFETs by using the analytical solution of Poisson's equation. Through our theoretical subthreshold swing model, a comprehensive analysis including the impact of channel thickness ($T_{\rm ch}$) and BI thickness ($T_{\rm BI}$) on the electrostatic integrity of the UTB GeON MOSFET is presented. The impact of BI permittivity on the electrostatic integrity of the UTB MOSFETs with germanium channel is also examined for the first time. This paper is organized as follows. In Section II, we derive an analytical UTB subthreshold swing model to describe the subthreshold characteristics of the UTB GeON MOSFETs. Investigations of the electrostatic integrity for UTB GeON MOSFET are presented in Section III. Section IV concludes the paper.

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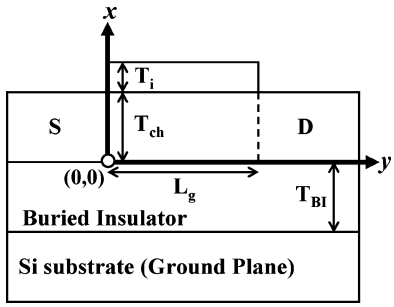

Fig. 1. Schematic sketch of UTB MOSFET with thin BI structure investigated in this study.

II. Analytical Subthreshold Swing Model for GeON MOSFET

Our theoretical subthreshold swing for the UTB GeON MOSFET is derived from the analytical potential solutions in the subthreshold region. Fig. 1 shows a schematic sketch of a UTB with thin BI structure. In the subthreshold regime, the channel is fully depleted with negligible mobile carriers. Therefore, the channel potential distribution $\phi_{\rm ch}(x,y)$ satisfies the Poisson's equation

$$\frac{\partial^2\phi_{\rm ch}(x,y)}{\partial x^2}+\frac{\partial^2\phi_{\rm ch}(x,y)}{\partial y^2}=-\frac{qN_{\rm ch}}{\varepsilon_{\rm ch}} \tag{1}$$

where $N_{\rm ch}$ and $\varepsilon_{\rm ch}$ are the channel doping and permittivity, respectively.

Since there is no charge in the BI region, the BI potential distribution $\phi_{\rm BI}(x,y)$ satisfies the Laplace equation

$$\frac{\partial^2\phi_{\rm BI}(x,y)}{\partial x^2}+\frac{\partial^2\phi_{\rm BI}(x,y)}{\partial y^2}=0 \tag{2}$$

with the required boundary conditions described as

$$\phi_{\rm ch}(T_{\rm ch},y)+T_i\frac{\varepsilon_{\rm ch}}{\varepsilon_i}\left.\frac{\partial\phi_{\rm ch}(x,y)}{\partial x}\right|_{x=T_{\rm ch}}=V_g-V_{\rm fb} \tag{3}$$

$$\phi_{\rm ch}(x,0)=-\phi_{\rm ms}+V_s \tag{4}$$

$$\phi_{\rm ch}(x,L_g)=-\phi_{\rm ms}+V_d \tag{5}$$

$$\phi_{\rm BI}(-T_{\rm BI},y)=V_{\text{back-gate}}-V_{\text{fb,back-gate}}+(E_{i,\rm ch}-E_{i,\rm sub}) \tag{6}$$

$$\phi_{\rm BI}(x,0)=\left[V_{\text{back-gate}}-V_{\text{fb,back-gate}}+(E_{i,\rm ch}-E_{i,\rm sub})\right]+\frac{(-\phi_{\rm ms}+V_s)-\left[V_{\text{back-gate}}-V_{\text{fb,back-gate}}+(E_{i,\rm ch}-E_{i,\rm sub})\right]}{T_{\rm BI}}x \tag{7}$$

$$\phi_{\mathrm{BI}}(x, L_g) = \lfloor V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\mathrm{ch}} - E_{i,\mathrm{sub}}) \rfloor + \frac{(-\phi_{\mathrm{ms}} + V_d) - [V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\mathrm{ch}} - E_{i,\mathrm{sub}})]}{T_{\mathrm{BI}}} x \tag{8}$$

$$\varepsilon_{\mathrm{ch}} \frac{\partial \phi_{\mathrm{ch}}(x,y)}{\partial x}\bigg|_{x=0} = \varepsilon_{\mathrm{BI}} \frac{\partial \phi_{\mathrm{BI}}(x,y)}{\partial x}\bigg|_{x=0} \tag{9}$$

$$\frac{\partial \phi_{\mathrm{ch}}(x,y)}{\partial y}\bigg|_{x=0} = \frac{\partial \phi_{\mathrm{BI}}(x,y)}{\partial y}\bigg|_{x=0} \tag{10}$$

where T_{ch}, T_i, and T_{BI} are the thicknesses of channel, gate insulator, and BI, respectively. L_g is the gate length. ε_i and $\varepsilon_{\mathrm{BI}}$ are the permittivity of gate insulator and BI, respectively. V_g, $V_{\text{back-gate}}$, V_d, and V_s are the voltage biases of gate, back-gate, drain, and source, respectively. V_{fb} and $V_{\text{fb,back-gate}}$ are the flat-band voltages of gate and back-gate, respectively. ϕ_{ms} is the builtin potential of the source/drain to the channel. $E_{i,\mathrm{ch}}$ and $E_{i,\mathrm{sub}}$ are the intrinsic Fermi level of channel and substrate (back-gate), respectively.

The corresponding 2-D boundary value problem can be divided into two subproblems, a 1-D Poisson's equation and a 2-D Laplace equation, respectively. Using the superposition principle, the complete channel potential solution is $\phi_{\mathrm{ch}}(x,y) = \phi_{\mathrm{ch},1}(x) + \phi_{\mathrm{ch},2}(x,y)$, where $\phi_{\mathrm{ch},1}(x)$ and $\phi_{\mathrm{ch},2}(x,y)$ are solutions of 1-D and 2-D subproblems in the channel, respectively. The 1-D solution $\phi_{\mathrm{ch},1}(x)$ can be expressed, (11)–(13), as shown at the bottom of this page.

In solving the 2-D subproblem, the boundary condition of gate dielectric/channel interface (3) is simplified by converting the gate dielectric thickness to $(\varepsilon_{\mathrm{ch}}/\varepsilon_i)$ times and replacing the gate dielectric region with an equivalent channel-material region. The electric field discontinuity across the gate dielectric and channel interface can thus be eliminated. For the channel/BI interface, both the potential distribution in the channel $[\phi_{\mathrm{ch},2}(x,y)]$ and that in the BI $[\phi_{\mathrm{BI},2}(x,y)]$ have to be considered to satisfy the boundary conditions (9) and (10).

The 2-D solution $\phi_{\mathrm{ch},2}(x,y)$ can be obtained using the method of separation of variables

$$\phi_{\mathrm{ch},2}(x,y) = \sum_n \left\{ [c_n \sinh(\gamma_n y) + c'_n \sinh(\gamma_n (L_g - y))] \sin(\gamma_n x) + e_n \sinh\left(\lambda_n \left(T_{\mathrm{ch}} + \left(\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i}\right) T_i - x\right)\right) \sin(\lambda_n y) \right\} \tag{14}$$

where

$$\lambda_n = \frac{n\pi}{L_g} \tag{15}$$

$$\gamma_n = \frac{n\pi}{(T_{\mathrm{ch}} + (\varepsilon_{\mathrm{ch}}/\varepsilon_i)\, T_i)}. \tag{16}$$

The coefficients c_n, c'_n, and e_n in (14) can be expressed as

$$c_n = \frac{1}{\sinh(\lambda_n L_g)} \left[2(-\phi_{\mathrm{ms}} + V_d - B) \frac{1-(-1)^n}{n\pi} + 2A \left(T_{\mathrm{ch}} + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i} T_i\right) \frac{(-1)^n}{n\pi} + 2\left(T_{\mathrm{ch}} + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i} T_i\right)^2 \frac{(-1)^n - 1}{(n\pi)^3} \right] \tag{17}$$

$$c'_n = \frac{1}{\sinh(\lambda_n L_g)} \left[2(-\phi_{\mathrm{ms}} - B) \frac{1-(-1)^n}{n\pi} + 2A \left(T_{\mathrm{ch}} + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i} T_i\right) \frac{(-1)^n}{n\pi} + 2\left(T_{\mathrm{ch}} + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i} T_i\right)^2 \frac{(-1)^n - 1}{(n\pi)^3} \right] \tag{18}$$

$$e_n = \frac{(\mathrm{RHS}_n / \mathrm{LHS}_n)}{\sinh((n\pi/L_g)(T_{\mathrm{ch}} + (\varepsilon_{\mathrm{ch}}/\varepsilon_i)\, T_i))} \tag{19}$$

where

$$\mathrm{LHS}_n = \lambda_n \coth(\lambda_n T_{\mathrm{BI}}) + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{BI}}} \lambda_n \coth(\lambda_n ((\varepsilon_{\mathrm{ch}}/\varepsilon_i)\, T_i + T_{\mathrm{ch}})) \tag{20}$$

$$\begin{aligned} \mathrm{RHS}_n = {} & 2\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{BI}}} A \frac{1-(-1)^n}{n\pi} \\ & + \sum_m \left\{ \left[c_n \frac{\{[(2\varepsilon_{\mathrm{ch}}/\varepsilon_{\mathrm{BI}})(-1)^{n+1}]/n\pi\} \sinh(\lambda_m L_g)}{1 + (\gamma_m/\lambda_n)^2} \right. \right. \\ & \left. + c'_n \frac{[(2\varepsilon_{\mathrm{ch}}/\varepsilon_{\mathrm{BI}})/n\pi] \sinh(\lambda_m L_g)}{1 + (\gamma_m/\lambda_n)^2} \right] \lambda_m \\ & - d_n \frac{m\pi}{T_{\mathrm{BI}}} \frac{(-1)^{m+n+1}}{n\pi} \frac{2\sinh((m\pi/T_{\mathrm{BI}})L_g)}{1 + (\gamma_m/\lambda_n)^2} \\ & \left. - d'_n \frac{m\pi}{T_{\mathrm{BI}}} \frac{(-1)^m}{n\pi} \frac{2\sinh((m\pi/T_{\mathrm{BI}})L_g)}{1 + (\gamma_m/\lambda_n)^2} \right\} \end{aligned} \tag{21}$$

$$\phi_{\mathrm{ch},1}(x) = -\frac{qN_{\mathrm{ch}}}{2\varepsilon_{\mathrm{ch}}} x^2 + Ax + B \tag{11}$$

$$A = \frac{(V_g - V_{\mathrm{fb}}) - [V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\mathrm{ch}} - E_{i,\mathrm{sub}})] + \frac{qN_{\mathrm{ch}}}{2\varepsilon_{\mathrm{ch}}} \left(T_{\mathrm{ch}}^2 + 2\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i} T_i T_{\mathrm{ch}}\right)}{T_{\mathrm{ch}} + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_i} T_i + \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{BI}}} T_{\mathrm{BI}}} \tag{12}$$

$$B = \frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{BI}}} T_{\mathrm{BI}} A + [V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\mathrm{ch}} - E_{i,\mathrm{sub}})] \tag{13}$$

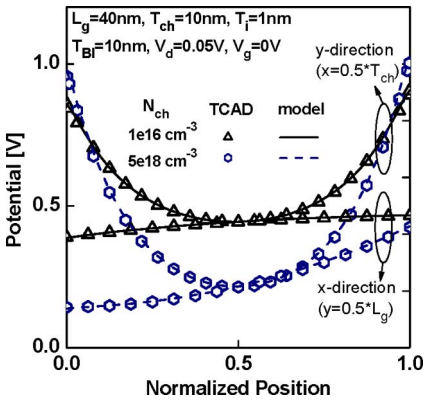

Fig. 2. Analytical potential distribution compared with TCAD simulation.

$$d_n = \frac{2}{\sinh(\gamma_n L_g)}\left\{[V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\text{ch}} - E_{i,\text{sub}})]\frac{1-(-1)^n}{n\pi} + [(-\phi_{\text{ms}} + V_d - B)]\frac{(-1)^{n+1}}{n\pi}\right\} \tag{22}$$

$$d'_n = \frac{2}{\sinh(\gamma_n L_g)}\left\{[V_{\text{back-gate}} - V_{\text{fb,back-gate}} + (E_{i,\text{ch}} - E_{i,\text{sub}})]\frac{1-(-1)^n}{n\pi} + [(-\phi_{ms} - B)]\frac{(-1)^{n+1}}{n\pi}\right\}. \tag{23}$$

Our analytical potential solution has been verified with technology computer-aided design (TCAD) simulation [16]. Fig. 2 shows that our model is fairly accurate for various channel doping (N_{ch}). Based on the potential solution, the subthreshold swing can be derived by (24), as shown at the bottom of this page.

Fig. 3 shows the subthreshold swing verifications with TCAD simulations for UTB SON and GeON devices with various gate lengths and drain biases. As can be seen, the UTB subthreshold swing model shows good agreement with TCAD simulation for both UTB SON and GeON devices.

III. Electrostatic Integrity of UTB GeON MOSFET

In this paper, important device parameters used for investigating the electrostatic integrity of lightly doped ($N_{\text{ch}} = 1 \times 10^{16}$ cm^{-3}) pFET UTB GeON MOSFET such as L_g and EOT are determined based on the ITRS roadmap [17].

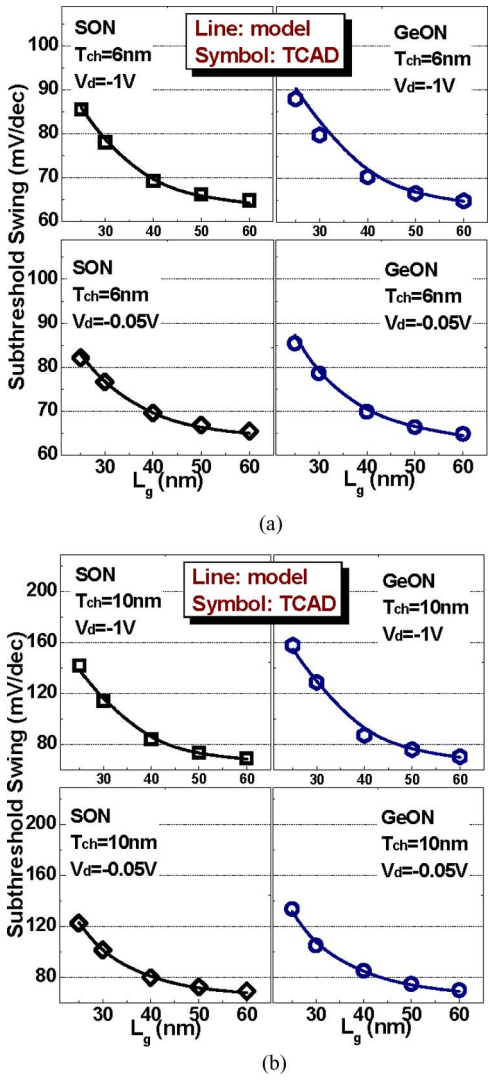

Fig. 3. Subthreshold swing verifications with TCAD simulations for SON and GeON devices with various gate lengths. EOT = 1 nm, $T_{\text{BI}} = 10$ nm. (a) $T_{\text{ch}} = 6$ nm. (b) $T_{\text{ch}} = 10$ nm.

Fig. 4 compares the subthreshold swing of the UTB GeON and SON devices for various T_{ch} with $L_g = 25$ nm. When $T_{\text{ch}} = 10$ nm, GeON device shows larger subthreshold swing than that of the SON device. This can be explained by Fig. 5, which shows the hole conduction path of the UTB GeON device is closer to the back-gate interface (T_{ch}/BI interface) than the UTB SON device. In other words, the UTB GeON device has worse electrostatic integrity than the UTB SON counterpart. However, it should be noted that as T_{ch} is scaled to 6–7 nm (see Fig. 4), the subthreshold swing of the GeON device becomes comparable to that of the SON device. Compared to Fig. 6 that the UTB GeOI (BI permittivity = 3.9) MOFET needs T_{ch} as

$$S = \left[\frac{\int_0^{L_g}\left[\int_0^{T_{\text{ch}}} e^{q\phi_{\text{ch}}/kT}(d\phi_{\text{ch}}/dV_g)dx/(\int_0^{T_{\text{ch}}} e^{q\phi_{\text{ch}}/kT}dx)^2\right]dy}{\int_0^{L_g}\left[dy/\int_0^{T_{\text{ch}}} e^{q\phi_{\text{ch}}/kT}dx\right]}\right]^{-1}\frac{kT}{q}\ln(10) \tag{24}$$

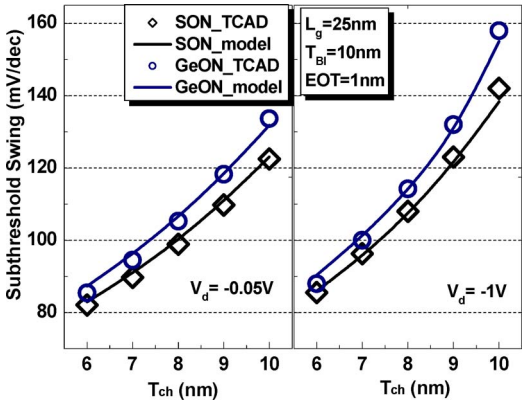

Fig. 4. Impact of $T_{\rm ch}$ on the subthreshold swing of UTB GeON and SON devices for $V_d = -0.05$ and -1 V with $L_g = 25$ nm. The UTB GeON and SON devices show comparable subthreshold swing as $T_{\rm ch}$ is scaled to 6–7 nm.

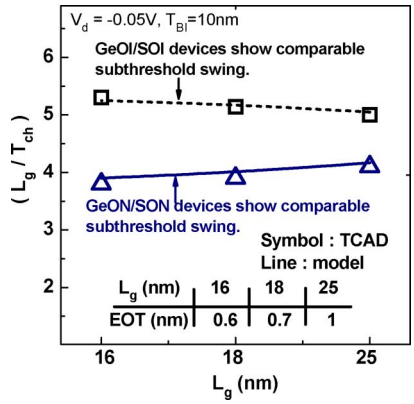

Fig. 7. GeON devices with $L_g/T_{\rm ch}$ around 4 show comparable subthreshold swing to that of SON devices.

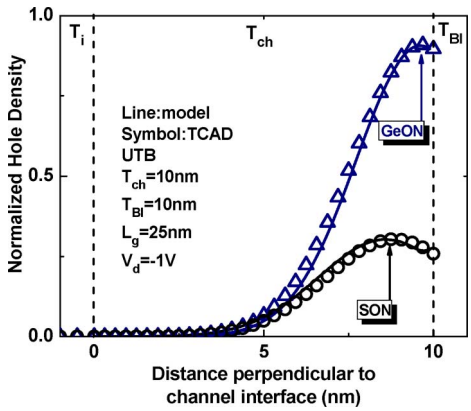

Fig. 5. Normalized hole density distribution (at mid-distance between source and drain) for the UTB SON and GeON devices in the subthreshold region. The arrow tip indicates the hole conduction path.

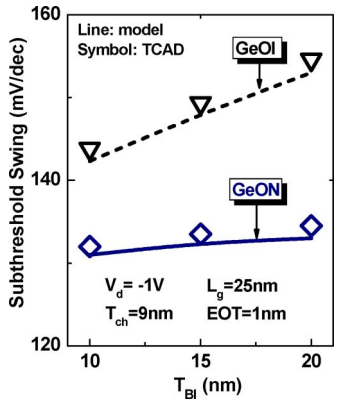

Fig. 8. Subthreshold swing as a function of buried oxide thickness for the UTB GeON and GeOI devices.

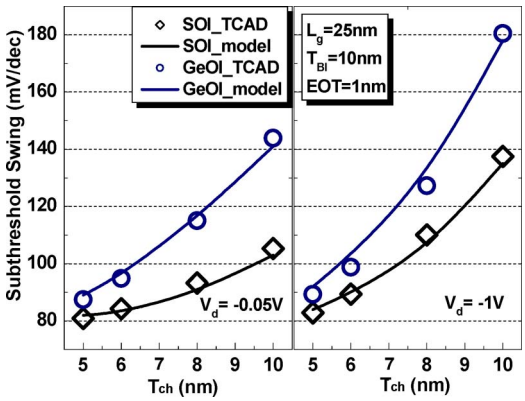

Fig. 6. Impact of $T_{\rm ch}$ on the subthreshold swing of UTB GeOI and SOI devices for $V_d = -0.05$ and -1 V with $L_g = 25$ nm. The UTB GeOI and SOI devices show comparable subthreshold swing as $T_{\rm ch}$ is scaled to 5 nm.

thin as 5 nm [18] to show comparable subthreshold swing to that of the corresponding silicon-on-insulator (SOI) device, the UTB GeON MOSFETs exhibit better electrostatic integrity than the GeOI counterparts.

More generations of UTB devices have been investigated based on the ITRS roadmap [17]. Fig. 7 shows that the GeON devices with the ratio of L_g to $T_{\rm ch}$ around 4 can show comparable subthreshold swing to that of the SON devices. However, the GeOI devices with the ratio of L_g to $T_{\rm ch}$ around 5 exhibit comparable subthreshold swing to that of the SOI counterparts.

Fig. 8 compares the impact of BI thickness $T_{\rm BI}$ on the subthreshold swing of the UTB GeON and GeOI devices. As can be seen, $T_{\rm BI}$ reduction is more effective for the UTB GeOI devices to improve its electrostatic integrity than the UTB GeON devices. This is because, the UTB GeOI devices with higher BI permittivity suffer larger fringing field from drain to source through BI.

Fig. 9 shows the impact of the BI permittivity on the subthreshold swing of UTB devices with germanium and silicon channel. It can be seen that UTB MOSFETs with lower BI permittivity show lower subthreshold swing because of the reduced fringing field. Moreover, the BI permittivity reduction is more effective for germanium-channel UTB device to achieve better electrostatic integrity than the silicon-channel UTB one. The UTB germanium channel device with lower BI permittivity also shows lower variation in subthreshold swing, as shown in Fig. 10. In other words, the UTB GeON device exhibits lower subthreshold swing sensitivity to L_g and $T_{\rm ch}$ and thus better variation immunity than the GeOI counterpart.

TABLE I
COMPARISON OF VARIOUS UTB ARCHITECTURES

GeON	GeON MOSFETs show smaller subthreshold swing than GeOI MOSFETs.
	GeON MOSFETs show lower subthreshold swing sensitivity to T_{BI}, L_g, and T_{ch} as compared with the GeOI MOSFETs.
	GeON MOSFETs with the device design of L_g/T_{ch} around 4 can show comparable subthreshold swing to that of the SON MOSFETs.
SON	SON MOSFETs show smaller subthreshold swing than UTB SOI MOSFETs.
	Generally, SON MOSFETs show lower subthreshold swing than the GeON MOSFETs.
GeOI	GeOI MOSFETs with the device design of L_g/T_{ch} around 5 can show comparable subthreshold swing to that of the SOI MOSFETs.
	GeOI MOSFETs show larger subthreshold swing than GeON MOSFETs.
SOI	SOI MOSFETs show larger subthreshold swing than SON MOSFETs.
	Generally, SOI MOSFETs show lower subthreshold swing than the GeOI MOSFETs.

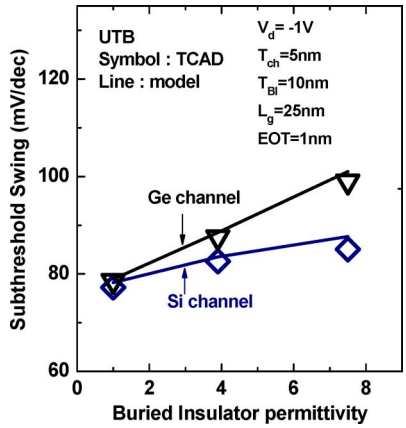

Fig. 9. Subthreshold swing as a function of BI permittivity for germanium channel and silicon channel UTB MOSFETs.

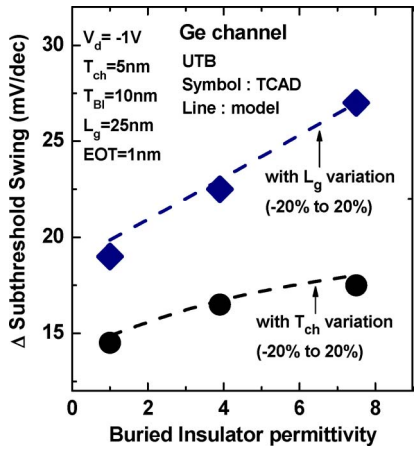

Fig. 10. ΔSubthreshold swing as a function of BI permittivity for germanium channel device with L_g and $T_{\rm ch}$ variation. ΔSubthreshold swing is defined as the subthreshold swing difference with $L_g/T_{\rm ch}$ variation from -20% to 20%.

IV. CONCLUSION

We have investigated the electrostatic integrity for the UTB GeON devices using analytical solution of Poisson's equation verified with TCAD simulation. The impacts of $T_{\rm ch}$ and $T_{\rm BI}$ on the electrostatic integrity of the UTB GeON MOSFET have been examined. Our results indicate that the UTB GeON MOSFETs with the device design of $L_g/T_{\rm ch}$ around 4 can show comparable subthreshold swing to that of the SON devices. The BI permittivity reduction is more effective for germanium-channel UTB devices to achieve better electrostatic integrity than the silicon-channel UTB counterparts. The subthreshold swing of the UTB GeON MOSFET with lower BI permittivity shows lower sensitivity to $T_{\rm BI}$, L_g, and $T_{\rm ch}$ as compared to the UTB GeOI MOSFET with higher BI permittivity. Table I summarizes the advantages of various UTB architectures in terms of subthreshold swing. UTB GeON MOSFETs with higher channel mobility and well-controlled electrostatic integrity are suggested to be used for aggressive generation beyond 22 or 16 nm. This study may provide insights for UTB device designs.

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