行政院國家科學委員會專題研究計畫　成果報告

矽奈米場效電晶體及氧化層奈米線：理論,實驗,及應用潛力(3/3)

計畫類別：個別型計畫
計畫編號：NSC93-2215-E-009-002-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立交通大學電子工程研究所

計畫主持人：陳明哲

計畫參與人員：呂明霈,李建志,顏士貴,曾貴鴻,蔡鐘賢

報告類型：完整報告

處理方式：本計畫可公開查詢

中　華　民　國 94 年 10 月 31 日

行政院國家科學委員會補助專題研究計畫成果報告

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計畫類別：■個別型計畫　　□整合型計畫

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成果報告類型(依經費核定清單規定繳交)：□ 精簡報告　■完整報告

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執行單位：國立交通大學電子工程學系

中　華　民　國　94　年　10　月　31　日

行政院國家科學委員會專題研究計畫成果報告

矽奈米場效電晶體及氧化層奈米線: 理論,實驗及應用潛力(3/3)

Si NanoFET and Oxide Nanowire: Theory, Experiment, and Potential Applications (3/3)

執行期限: 93/08/01 ~ 94/07/31
計畫編號: NSC 93-2215-E-009-002-

主持人：陳明哲教授　　國立交通大學電子工程學系

一、中文摘要

本計劃為期三年，探索奈米場效電晶體及氧化層奈米線之嶄新領域，在奈米場效電晶體部份，以最先進製程製作奈米場效電晶體元件，光罩閘極長度範圍 250 nm～20 nm，氧化層厚度 5 nm～<1 nm。 進行電性量測及低溫實驗。利用自行發展的量子力學模擬器與實驗比較以萃取重要物理參數。改進傳統通道反向散射理論之缺失，更新的版本能正確反映線性區完整特性，臨界電壓定義清楚無誤，以及低溫特性等。更新的通道反向散射理論將含有已萃取的二維電子氣或二維電洞氣密度等，並表達為通道長度，氧化層厚度，閘電壓及汲極電壓之函數。也進行應用潛力之研究：(1) 萃取載子速度分布以具體闡明載子速度超越；(2) 預測閘極長度縮小至極限時彈道傳輸限制並與文獻比較；(3) 預測長通道 (250 nm) 遷移率變化引至推動電流變化百分比 (可與矽鍺通道製程之測試數據比較)；(4) 表現與溫度無關之奈米場效元件；(5) 開發 Spice 電路模擬器專用的更新通道反向散射奈米場效電晶體模式；(6) 晶片電路實現包括低溫電路；以及 (7) 其它應用潛力之發掘。

在氧化層奈米線部分，將發展自動化奈米線產生控制程式，一旦氧化層奈米線形成，即進行電性量測 (低電壓的範圍)。也量測時域之電報雜訊，頻域之低頻雜訊特性，以及低溫下的實驗量測。利用量子點接觸理論模式與實驗比較，萃取相對應的參數。並發展出量子點接觸之電報雜訊版本，低頻雜訊版本以及低溫版本，也與實驗一一比較並萃取參數。亦進行應用潛力之研究：(1) 開發更為快速的奈米線產生設備或產生電路；(2) 因與矽的製程完全相容，將包含其他傳統的矽元件以產生功能電路如負電阻，階梯狀特性等；(3) 利用所量測到的低溫參數設計奈米線低溫電路；(4) 在小面積下或在低溫下應能表現出類似單電子電晶體之特性；以及 (5) 其他應用潛力之發掘。

關鍵詞：矽，奈米，場效電晶體，氧化層，奈米線，散射，低溫，彈道傳輸，電報雜訊，低頻雜訊，量子點接觸，單電子電晶體。

英文摘要

This is a three-years project to explore new areas of nanoFET and oxide nanowire. In the nanoFET side，state-of-the-art process technologies are used for manufacturing nanoFETs with mask gate length ranging from 250 nm down to 20 nm and gate oxide thicknesses from 5 nm to less than 1 nm，then followed by I-V/C-V measurement as well as low temperature experiment. Our developed quantum mechanical I-V/C-V simulators are used to compare experimental data from which relevant physical parameters are extracted. Improved channel backscattering theory including two-dimensional electron or hole gas is expressed as a function of temperature，channel length，oxide thickness，gate voltage，and drain voltage. Also carried out are promising potentials：(1) extract carrier velocity profile in order to highlight velocity overshoot；(2) predict ballistic limit as channel length is reduced down to extremity along with literature comparison；(3) predict device drive current change due to mobility change (compare data from strained-Silicon or Si-Ge channel process)；(4) implementation of

nanoFETs having less temperature dependencies；(5) update SPICE models to account for improved channel backscattering in nanoFETs；(6) realization of integrated circuits including low temperature circuits；and (7) exploration of other applications.

In the oxide nanowire side，we will develop an automatic electrical control program for nanowire generation in gate oxide films. Once a nanowire is created therein，low-voltage I-V's are measured. Also performed are random telegraph signal in time domain，low frequency noise in frequency domain，and low temperature experiment. Quantum point contact model is used to compare data in order to extract physical parameters. We will develop out random telegraph signal version，low frequency noise version，and low temperature version of channel back scattering theory，as well as experimental comparison and parameter extraction. We also examine potential applications：(1) develop fast equipment or circuits for nanowire generation；(2) owing to 100% compatibility with current silicon processes，combine other conventional silicon devices to constitute functional circuits with novel features like negative resistance and step-like current；(3) apply low temperature data and parameters to design and realize low temperature circuits；(4) under small area or low temperature conditions，expect nanoFETs to show behaviors of single electron transistors ; and (5) explore other applications.

Key Words：Silicon，nano，FET，oxide，MOS，nanowire，scatter，low temperature，random telegraph signal，low frequency noise，quantum point contact，single electron transistors

二、緣由與目的

1. 近年來隨著 Si MOSFET 元件的持續不斷縮小，其有效通道(channel)長度(等於 mask gate length 光罩閘極長度減去 Source/Drain overlap 長度)已經達到奈米級的尺寸，可與平均自由路徑(mean-free-path)相當甚至更小，在此情況下，傳統的載子遷移率(mobility)已無意義，因其在如此超短通道內遭遇極為微少的碰撞(collision)，故必得以量子力學即波(wave)的觀點去闡釋並處理相關問題。普渡大學的 Datta 教授與 Lundstrom 教授所提出的通道背向散射理論(Channel Backscattering Theory)特別突出，尤能處理像載子速度超越(Carrier Velocity Overshoot)，彈道傳輸限制(Ballistic Transport Limit)等爭議性極高的問題，吸引全球目光。MIT 的 Antoniadis 教授利用通道背向散射理論在載子速度這議題上有傑出的表現，IBM 的 Yuan Taur 博士（現加大教授）在蒙地卡羅模擬及實驗上證明可與通道背向散射理論銜接。

至於通道背向散射理論應用潛力，本研究群堅信：

1. 目前電路模擬器 SPICE 所用之 Device Models 係基於載子之 Drift 及 Diffusion(也即 mobility)行為而來，不適用於奈米 FET 元件。因之能以波動處理通道傳輸特性之背向散射理論應可為奈米 FETs 元件特性模式之用以取代 SPICE 中元件 Drift-Diffusion 版本。
2. 波動或透納(Tunneling)行為基本上為量子傳輸應有與溫度無關的特性，因之奈米 FETs 元件表現出與溫度無關的特性應可期待。

通道背向散射理論亦牽涉到 Subbands 上二維電子氣(2DEG)或二維電洞氣(2DHG)的 Quantum Confinement 效應。本研究群這幾年已自行發展出量子力學(Quantum Mechanics) I-V/C-V 模擬器(已算入 2DEG 及 2DHG)，亦對波的入射及反射行為鑽研至深。而基於奈米 FET 元件日趨重要，相關的傳導機制必須釐清且應用潛力有待發掘及推廣，本實驗室基於在此領域有良好研究基礎，特別提出此一研究計畫。

本計畫亦探討閘極介電層 percolation 路徑(截面積約 1nm^2，長度約為介電層厚度)的奈米線 nanowire-like 行為，最近 Spain Sune 教授 group 提出 Quantum point contact 理論模式成功闡釋此 nanowire 行為。Percolation 路徑自身亦表現出 on-off switching 或 RTS(Random Telegraph Signal；電報雜訊)現象，甚至閘極介電層內有二條 percolation 路徑或 nanowires，彼此之間產生詭異的 on-off switching 現象，Sune 教授亦認為 percolation 路徑的 nanowire 行為可為未來元件候選人之一，且有一大優勢:與現有 Silicon CMOS 製程完全相容，問題是該如何實現。本研究群這幾年在閘極氧化層 percolation 路徑的理論模式實驗已作出好的研究，我們並且觀察到 nanowire 在頻域的 Lorentzian noise(相當於時域的 RTS 現象)，並很清楚如何從電性上產生 percolation nanowire 且不致因隨後的大電流進入而產生的熱能造成鉅大的結構破壞。我們亦要研究 percolation nanowire 在低溫下的巨觀及微觀行為特性，希冀能觀察到前人未見者並提供更多的設計參數。Percolation nanowire 的應用潛力也將具體地提出及製程實現。

三、研究方法與成果

1. (通道背向散射)

We have successfully experimentally separated the channel backscattering coefficients into two distinct components: Mean-free-path and KT layer width, as shown in the published articles (*2004 IEEE TED and 2005 Silicon Nanoelectronics Workshop*, for example).

2. (奈米系統的雜訊與擾動)

Coulomb energy is essential to the charging of a nanometer-scale trap in the oxide of a metal-oxide-semiconductor (*MOS*) system. Traditionally the Coulomb energy calculation was performed on the basis of an interface-like trap. In this paper, we present for the first time experimental evidence from a 1.7-nm oxide: substantial enhancements in Coulomb energy due to the existence of a deeper trap in the oxide. Other corroborating evidence is achieved using a multiphonon theory, which can adequately elucidate the measured capture and emission kinetics. The corresponding configuration coordinate diagrams are established. Then we elaborate on the clarification of the Coulomb energy and differentiate it from that in memories containing nanocrystals or quantum dots in the oxide. Eventually, some critical issues encountered are addressed as well.

3. (奈米線)

We fabricate and measure a single-walled carbon nanotube transistor having a liquid-gate electrode. The ratio value of I_{on}/I_{off} is as high as 10^4, indicating the presence of a semiconducting channel. A passivation layer over the source/drain electrode greatly suppresses the liquid-gate leakage by about three orders of magnitude. The channel currents are noticeably distinct between two liquid samples: distilled water and aqueous solution (1×10^{-4} M NaCl). This biological sensing ability is attributed to the different electrical double-layer capacitances with respect to the bulk part of the channel. The corresponding theoretical calculation is carried out in detail.

四、結論與討論

1. 在奈米系統的雜訊與擾動領域當中我們確實已作出世界級的貢獻:

(a) 一篇送至 *Physical Review – B* 的論文獲致兩位國際評審的高度推薦 (well written, high quality, new data, novel linkage to quantum dots in a MOS system, and interesting and useful analysis)

(b) 一篇 *Applied Physical Letters* (M. J. Chen and M. P. Lu, *APL*, vol. 81, p. 3488, 2002) 論文先後被 德國漢堡大學 Schroeder 教授 及 希臘雅典大學 Varotsos 教授 於他們的 *APL* and *PRL* 論文引用:

Europhys. Lett. **65**, 753 (2004).
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2. 我們已將奈米線研究延伸至奈米碳管電晶體測試鍵, 完成一篇 *Applied Physical Letters* 探討生物樣本電性量測及量子力學理論計算, 特別是後者確實 interesting and useful 且為 *APL* 國際評審高度認定, *APL* 編輯最近的回應是: Considerable for publication.

3. 最後在通道背向散射領域, 我們確實完成了大量的實驗工作, 也有一些論文發表並被引用 (部分見下). 然而每當我們自以為接近成功的一步, 我們就愈發覺現有的通道背向散射理論架構有所不足, 是以計畫雖然結束我們仍繼續肇清通道背向散射理論架構, 作法是運用 Monte Carlo 技巧, 到目前為止已見若干突破, 假以時日 (約需數月) 我們定能在此嶄新領域取得國際性地位.

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5. M. P. Lu and M. J. Chen, "Oxide trap enhanced Coulomb energy in a metal-oxide-semiconductor system," *Physical Review - B*, 2005 (under review for months, now approaching with positive results).

Figures:

(cited by a 2004 IEDM paper)

Electro-Thermal Comparison and Performance Optimization of Thin-Body SOI and GOI MOSFETs

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Taking the above into account, we obtain an expression for the temperature dependence of the saturation current for devices near the limit of scaling:

$$\frac{\Delta I_d}{I_{do}} = \left[\frac{1}{T_o}\left(\frac{1}{2} + \frac{2\alpha - 1}{2 + \lambda_o/l_o}\right) - \frac{\eta}{V_{gs} - V_{to}}\right]\Delta T, \quad (8)$$

which is a generalization of the expression in [14]. All

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(cited by a 2005 VLSI Tech. paper)

The Impact of Uniaxial Strain Engineering on Channel Backscattering in Nanoscale MOSFETs

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cally obtained with preferable strain engineering, channel backscattering reduction should receive no less attention for ultimate performance in nanoscale MOSFETs.

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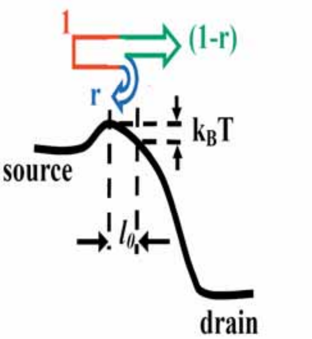


Fig. 1 Schematic diagram of carrier channel backscattering in nanoscale MOSFETs. Carriers injected from the source may be backscattered in k_BT layer.

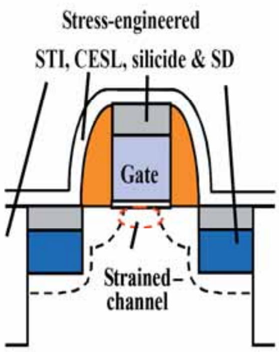


Fig. 2 Schematic structure of process strained silicon (PSS) MOSFETs.

Table I Summary of (a) factors of drive current equation, and (b) temperature-dependent model for λ_0 / l_0 extraction used in this work.

(a) I_{dsat} Approximation from Full-range Expression [7]	$I_{dsat} = WC_{eff}\upsilon_{inj}(\frac{1-r_{sat}}{1+r_{sat}})(V_g - V_T)$
Injection Velocity υ_{inj}	$\upsilon_{inj} = \sqrt{\frac{2k_BT}{\pi m^*}}$, m* : effective mass
Backscattering factors	$r_{sat} = \frac{l_0}{l_0 + \lambda_0}$ l_0 : k_BT layer $= \frac{k_BT}{q\varepsilon(0^+)}$ $\varepsilon(0^+)$: electric field @ top of barrier λ_0 : MFP of carrier backscattering $= \frac{2D_n}{\upsilon_{inj}} = \frac{2k_BT}{\upsilon_{inj}q}\mu_n^0$ μ_n^0 : near equilibrium mobility @ top of barrier
(b) Temperature-Dependent Model for λ_0 / l_0 Extraction [6]	
	$\frac{\partial I_{dsat}}{\partial T} = \alpha I_{dsat} \Rightarrow \alpha = \frac{(0.5 - \frac{4}{2+\lambda_0/l_0})}{T} - \frac{\eta}{V_g - V_T}$
α, η, V_T	$\alpha = \frac{I_{dsat}(T_1) - I_{dsat}(T_2)}{T_1 - T_2}$ $\eta = \frac{V_T(T_1) - V_T(T_2)}{T_1 - T_2}$ $V_T = V_{T,lin}$($G_{m,max}$ method@ $\lvert V_d \rvert$= 10mV) $-\Delta V_T$(Const. I_d @ $\lvert V_d \rvert$= 10mV, 1V)

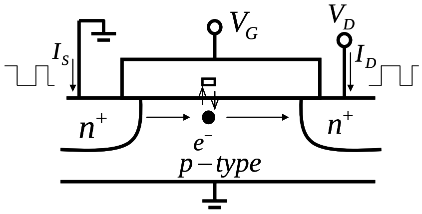


Fig. 1 Schematic cross section of the device showing the capture-emission process.

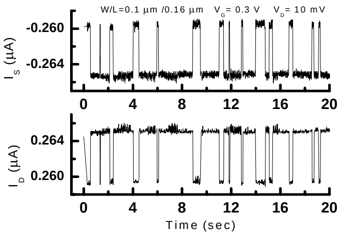


Fig. 2 The measured fluctuations simultaneously occurring in both source and drain currents.

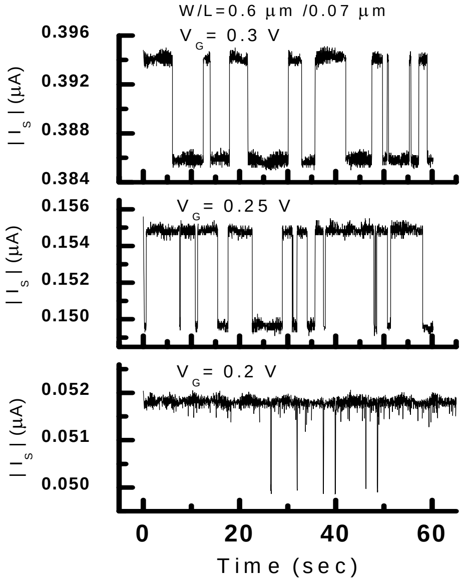


Fig. 3 The measured RTS recorded as a function of gate voltage.

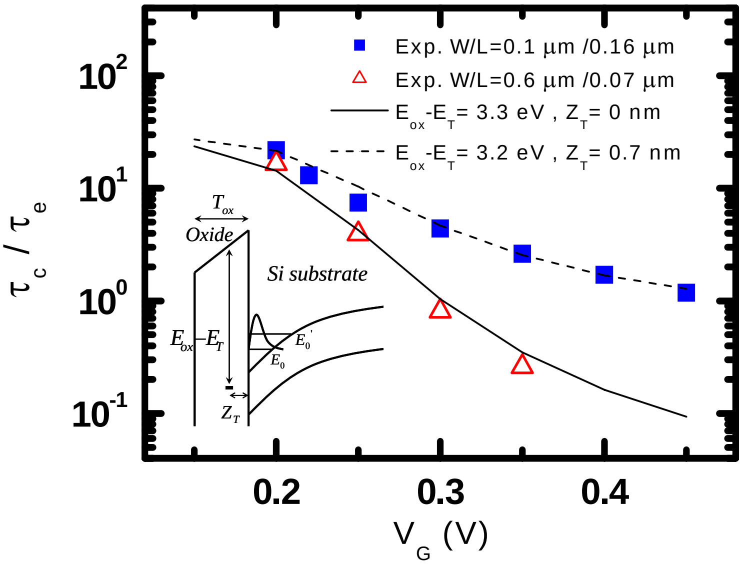


Fig. 4 The measured (symbols) and calculated (lines) ratio of the mean capture time (τ_c) divided by the mean emission time (τ_e) against gate voltage for two devices. The inset shows underlying band diagram indicating the trap position.

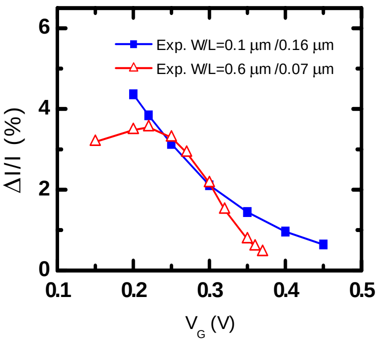


Fig. 5 The measured RTS amplitude versus gate voltage for two devices.

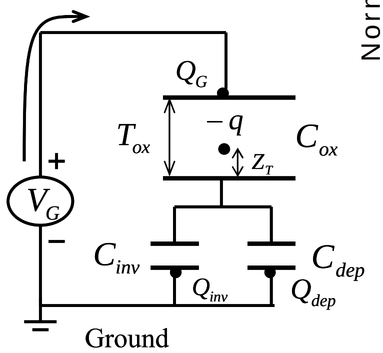


Fig. 6 A capacitive coupling model taking the effect of the trap depth into account.

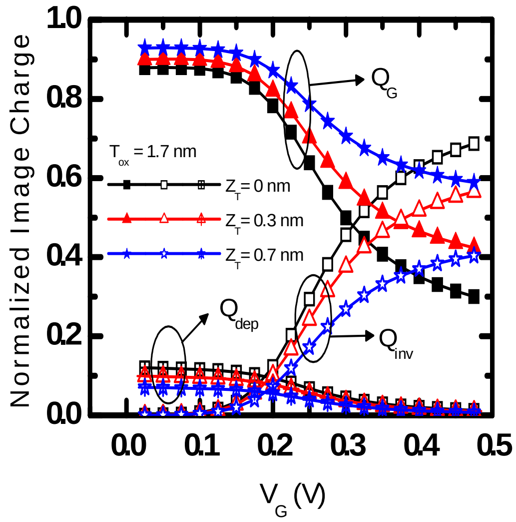


Fig. 7 The image charge on the gate, the inversion layer, and the depletion region versus gate voltage for different trap depths.

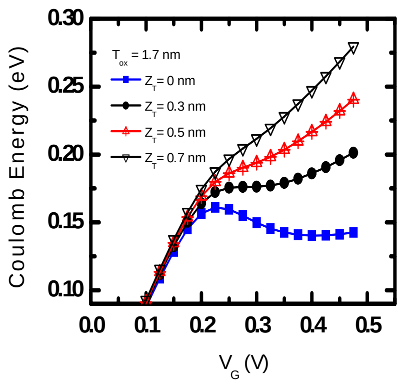


Fig. 8 The Coulomb energy versus gate voltage for different trap depths.

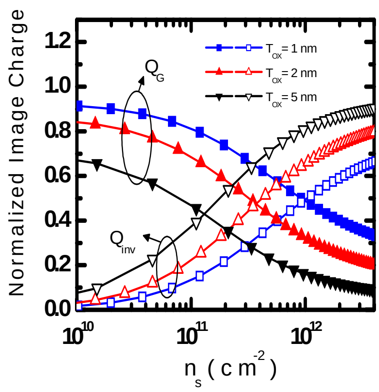


Fig. 9 The image charge versus inversion layer carrier density for different oxide thicknesses. $z_T = 0$.

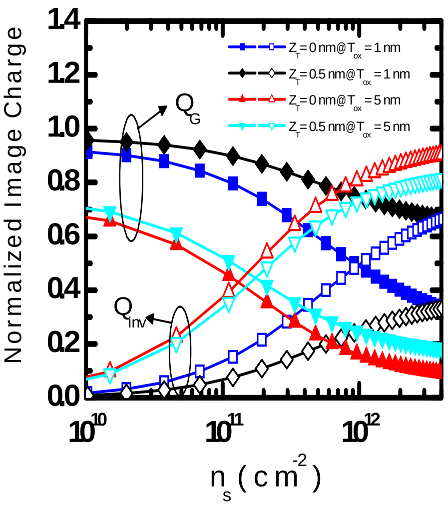
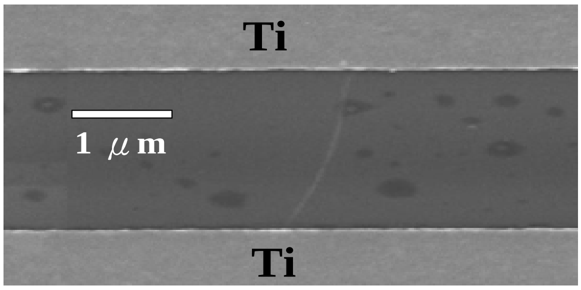
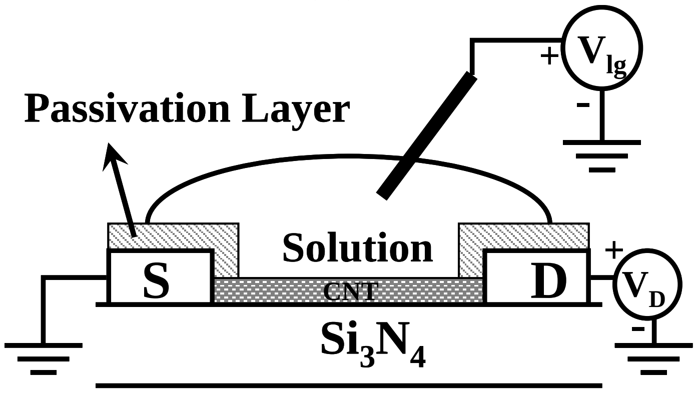


Fig. 10 The image charge versus inversion layer carrier density for different oxide thicknesses and different trap depths.



(a)



(b)

Fig. 11 (a) Topside view of the CNT FET testkey and (b) its measurement setup.

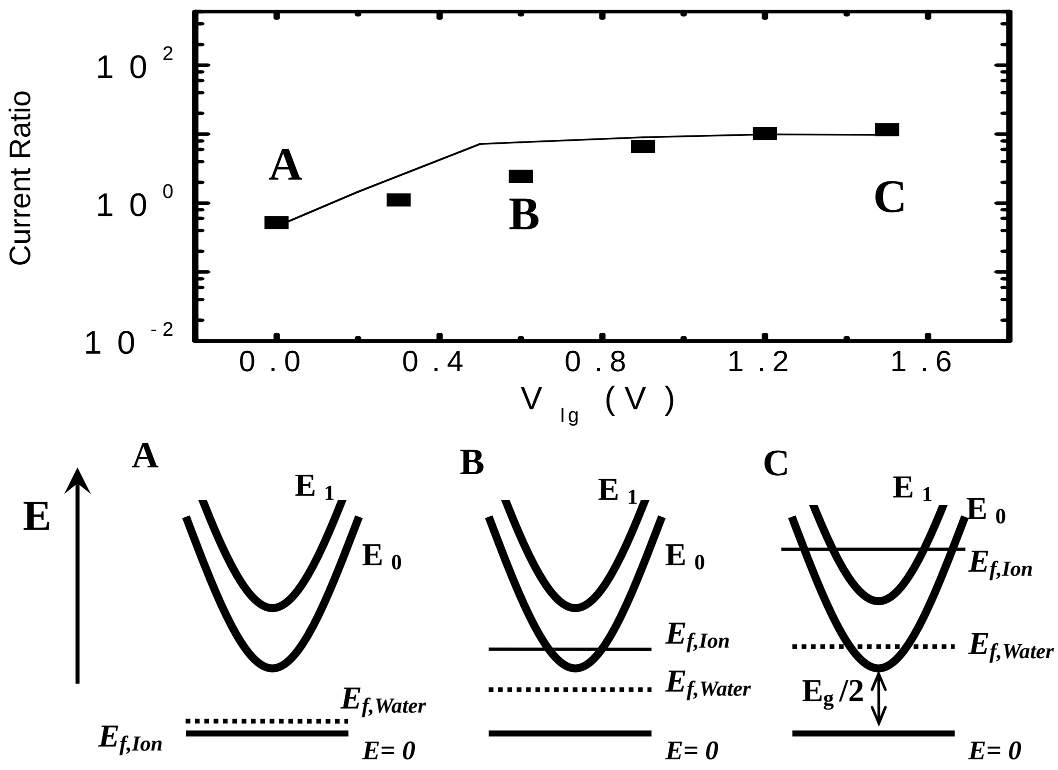


Fig. 12 Theoretical Calculation and Measurement Results corresponding to Fig. 11.