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高性能類比數位介面積體電路
High-Performance Analog-Digital Interface ICs

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一、摘要

本計畫將以嚴謹的設計技巧來研發高速且高解析度之類比數位混合訊號式積體電路。其中包括可變增益放大器、濾波器、取樣電路、類比數位轉換器、以及頻率合成器。這些電路可構成通訊實體層接收機中之類比前端電路。規劃的電路規格是訊號頻寬至少 100 MHz，取樣頻率至少 100 MHz，信號雜訊比至少 86 dB，以及解析度至少 14 Bits。所設計之電路都將以先進之 CMOS 製程，如 0.18 um，製作成晶片來加以驗證。雖然本計畫沒有明確指明應用範圍，以上規格可用於 Digital Software Radios，或 Base Station Multi-Channel Receivers，或未來高性能 Base-Band Receivers。

本計畫除了電路架構的創新外，同時會以數學化的設計方法，例如設計考量公式化以及最佳化，求得最好之高速低雜訊電路特性。並且應用數位校正的技術來達成所要求之電路線性度及解析度。除此之外，由於目前一般儀器無法量測到預期之電路性能，本計畫會發展所需要之高解析度晶片量測技術。

關鍵詞：混合訊號式積體電路、類比數位轉換器、CMOS。

Abstract

This project is to design and realize several high-speed high-resolution mixed-signal integrated circuits, using rigorous design techniques. Circuits under studied include programmable-gain amplifiers, filters, sample-and-hold circuits, analog-to-digital converters, and frequency synthesizers. The above circuits can be assembled as the analog front-ends in the physical-layer receivers for communications. The specifications for the circuits are at least 100-MHz signal bandwidth, 100-MHz sampling rate, 86-dB signal-to-noise ratio, and 14-bit resolution. All circuits will be realized using advanced fabrication technologies, e.g., 0.18um CMOS. Although the specifications are not based on any particular application, they are suitable for applications such as digital software radios, base station multi-channel receivers, and future high-performance base-band receivers.

In addition to the required circuit innovations, mathematical design methodologies, such as formularization of design considerations and global optimization, will be used to attain best high-speed and low-noise performance. The required linearity and resolution are achieved by using digital calibration techniques. Since the planned circuit performances are beyond the capabilities of the present-day measurement instruments, the necessary high-resolution measurement techniques will also be developed.

Key Words: Mixed-Signal Integrated Circuits, Analog-to-Digital Converters, CMOS.

二、緣由與目的

由於深次微米 CMOS 製程技術之進步，及單晶片系統 (System on a Chip) 設計技術之成熟，現今之單晶積體電路 (IC) 可以包含數千萬顆電晶體而具有功能強大之運算能力。這些 IC 也因此能提供一般消費者能負擔得起之高性能數位通訊解決方案，而滿足其對寬頻服務之需求。高性能數位通訊系統通常都是利用複雜之訊號處理技術來克服傳輸失真及雜訊干擾。在目前之數位通訊用實體層發收機 (Physical-Layer Transceiver)

中，大部分之訊號處理皆以數位之形式運算，而類比電路則是用於數位電路與傳輸媒介間之介面及訊號轉換。類比電路在單晶片系統中所佔之面積不會很大，通常低於20%，然而卻是限制系統功能的主要因素。

類比電路對於元件的匹配、線性度、壓抑雜訊能力等要求都比數位電路高出許多。而 CMOS 製程技術的發展方向，對類比電路而言，除了速度頻寬能增加外，對於其他電路特性卻都有不利的影響。因此可以預測將來混合訊號式（Mixed-Signal）單晶片系統的基本性能會由其中之類比電路所決定。

類比電路在設計時須考量許多不同之參數，如速度、失真度、雜訊、功率消耗、面積等。而個別的應用對於同樣的參數也有不同的定義方式及要求。放置於晶片中，類比電路容易受週遭環境及本身的佈局方式所影響。由於以上因素，再加上沒有通用且嚴謹的設計方法可適用於各種不同類型之電路，類比電路之設計到目前仍只仰賴 30 年前即發展出來之 SPICE 電路模擬軟體，以及設計者本身的養成和經驗。

本計畫將研究在深次微米 CMOS 製程下的高性能混合訊號式積體電路設計技術。強調的是低雜訊、高線性度、高解析度、而且又寬頻的類比電路。欲研究的次系統包括可變增益放大器，濾波器，取樣電路（Sample and Hold, S/H），類比數位轉換器（Analog-to-Digital Converter, ADC），及頻率合成器（Frequency Synthesizer）等。所有的電路都會有大於 14 Bit 的解析度（Resolution）或 86 dB 的信號雜訊比（Signal-to-Noise Ratio），而頻寬或取樣速度都會超過 100 MHz。雖然本計畫沒有明確指明應用範圍，以上規格可用於 Digital Software Radio 或 Base Station Multi-Channel Receivers，或將來高性能 Base-Band Transceivers。所設計之電路都將以最先進之 CMOS 製程，如 0.18 um，製作成晶片。

本計畫不以 Over-Sampling Delta-Sigma Modulation 的技巧來提升系統的解析度。而是研究嚴謹的電路設計技巧，用來發展寬頻且低雜訊的類比電路，再配合數位校正（Digital Calibration）技術來提高電路本身的解析度。同時在設計時，還需考量深次微米 CMOS 製程元件特性及低電壓操作環境。此外，由於現有的量測儀器不容易測試到預期的電路規格，本計畫會依需要發展量測技術。

三、執行成果

A. Analog-to-Digital Converter (ADC)

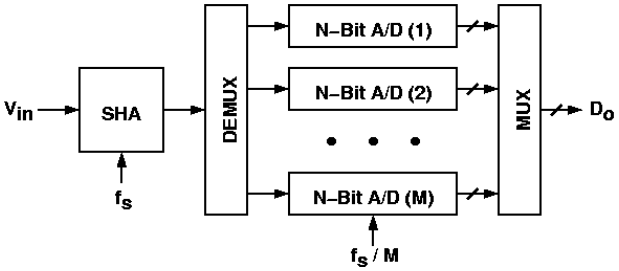

Fig. 1: Time-interleaved ADC with single SHA.

The time-interleaved configuration shown in Fig. 1 has been studied for high-speed high-resolution ADCs. The ADC uses M identical N-bit ADCs operating in parallel at f_s/M clock rate to achieve an equivalent f_s sampling rate and N-bit resolution. For this project, N will be larger than 14, and f_s will be more than 100 MHz. A single input sample-and-hold amplifier (SHA) is preferred to avoid the potential sampling phase offset if M distributed SHAs are used instead. The design of the input SHA is crucial, since it operates at sampling rate and needs to have N-bit resolution. The effects of the gain and offset mismatches among the sub-ADCs can be eliminated through calibration.

B. Sample-and-Hold Amplifier (SHA)

Fig. 2 shows the proposed SHA circuit architecture [1]. Analog switches S11-S14 and additional clock phases, ϕ_3 and ϕ_4, represent the input demultiplexer of a time-interleaved ADC system. During the channel-1 sample mode, $\phi_1 = 1$ and $\phi_3 = 1$, the input buffers B1 and B2 not only drive the C_{s1} and C_{s2} sampling capacitors but also precharge the opamp's output nodes including C_{L1} and C_{L2}. When switching to the hold mode ($\phi_1 = 0$), the opamp's outputs can settle to their final values in a much shorter time period without slewing due to the precharging. During the channel-2 sample mode, $\phi_1 = 1$ and $\phi_4 = 1$, the channel-2 capacitive loading of C_{L3} and C_{L4} are precharged alternately.

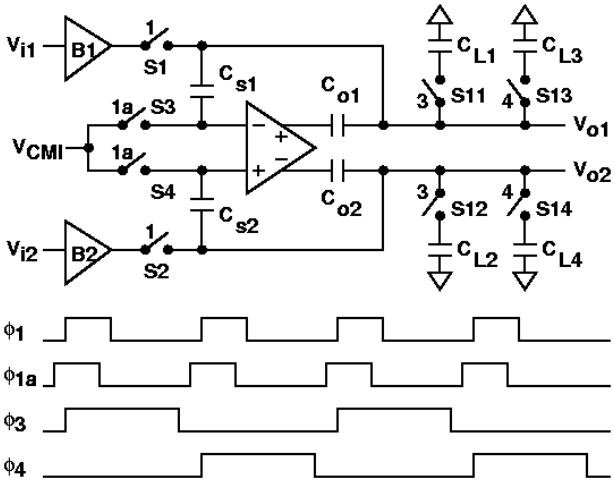

Fig 2: Precharged SHA for a 2-path time-interleaved ADC.

The two output coupling capacitors, C_{o1} and C_{o2}, are added to reduce the switching errors of S1 and S2. The combination of output capacitor coupling and precharging also reduce the opamp's the dc gain and output voltage swing requirements, so that higher speed can be achieved.

The schematic of the opamp is shown in Fig. 3. The telescopic configuration, consisting of M1-M9, is the most power efficient for similar speed performance. The circuit's limited output swing is not a concern in this precharged SHA application. The analog switch M10 is added to equalize the outputs during the sample mode. The continuous-time output common-mode feedback (CMFB) is realized using MC1-MC8. Due to the opamp's reduced output voltage swing, the opamp's output common-mode voltage can be sensed simply by dual source-coupled pairs, MC1-MC2 and MC3-MC4. The input and output common-mode voltage of the opamp, V_{CMI} and V_{CMO}, can be different, and both can be different from the common-mode voltage of the SHA's inputs. Realized in a 0.25 um CMOS technology, the opamp has a dc gain of 63 dB and a differential output swing of 800 mVpp. Its unity-gain frequency is 1.2 GHz when driving 1.5 pF capacitive loads while dissipating only 12.5 mW of power.

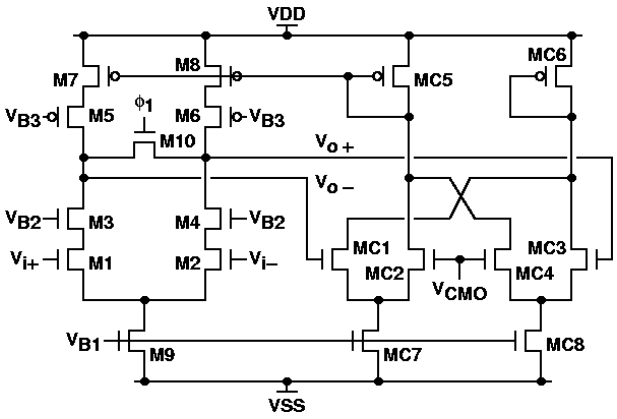

Fig 3: SHA operational amplifier circuit schematic.

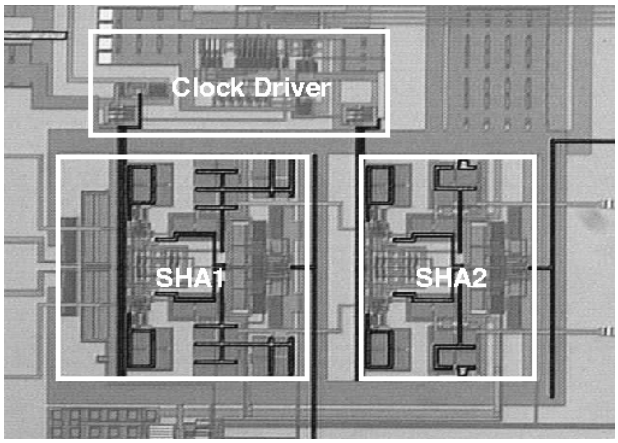

Fig 4: SHA chip micrograph.

The SHA is fabricated in a standard 0.25 um CMOS process. Fig. 4 is the chip micrograph. The active die area is 0.35 mm^2. Operating from a 2.5 V supply, the SHA's total power dissipation is 33 mW. The SHA can accommodate output swing as large as 2.7 Vpp with over 72 dB SFDR at 100 MHz sampling rate. It achieves 80 dB SFDR at 1.8 Vpp output.

C. 15-Bit 40 MS/s Pipelined ADC

The pipelined configuration shown in Fig. 5 offers good trade-off among power, speed, and dies area, and is suitable for implementing high-resolution Nyquist-rate ADCs. It consists of a front-end sample-and-hold amplifier (SHA), 17 radix-2 1.5-bit switched-capacitor (SC) pipeline stages, and a final 2-bit flash stage. It is known that gain errors caused by capacitor mismatches and opamp's finite gain in the pipeline stages can results in nonlinear A/D conversion for the entire pipeline. Calibration is required to achieve A/D resolution of more than 10 bits.

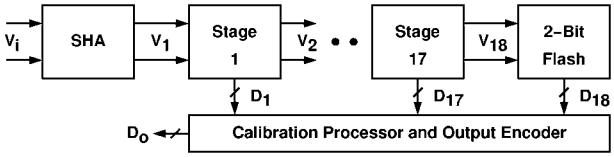

Fig 5: Pipelined ADC block diagram.

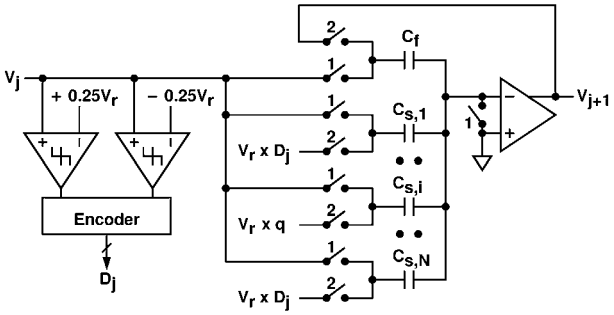

Fig 6: A radix-2 1.5-bit SC pipeline stage.

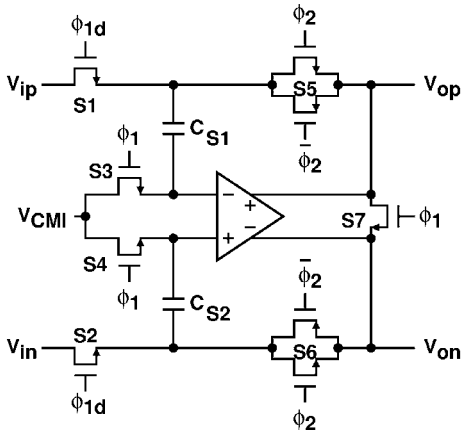

Fig 7: SHA circuit schematic.

A new background calibration scheme has been developed which can to measure and quantize the gain error of pipeline stages without interrupting the normal A/D operation [2]. To do this, a modified SC pipeline stage shown in Fig. 6 is used. A pseudo random signal is injected into this pipeline stage. The exact value of its voltage gain can then be obtained by extracting the random signal from the ADC's output code. Using this scheme, the procedures for calibration and A/D conversion can be performed simultaneously without interrupting each other.

Fig. 7 shows the SHA preceding the A/D pipeline. It employs a conventional flip-around configuration and has fast settling behavior due to large feedback factor. To apply bottom-plate sampling technique, S1 and S2 switches are turned off after S3 and S4 being turned off. The gate-controlling clocks for S1 and S2 are generated from two constant-V_{GS} bootstrapped clock generators.

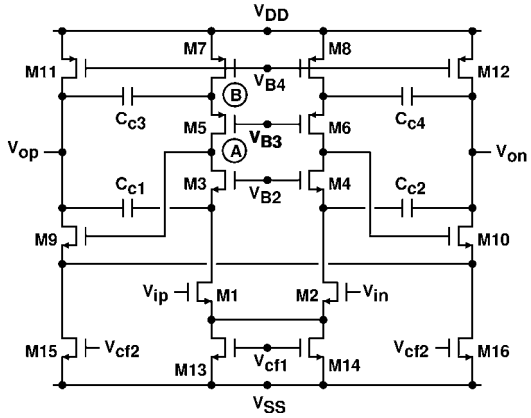

Fig 8: ADC operational amplifier circuit schematic.

Fig. 8 shows the topology of opamps used in SHA and all pipeline stages. The fully differential two-stage configuration consists of a telescopic first stage followed by a common-source second stage. Overall dc voltage gain is more than 90 dB. Operating under a 2.5 V supply, the opamp can provide a differential output voltage range as large as 2.8 Vpp. In the first pipeline stage, the opamp dissipates 22.5 mW of power and achieves a unity-gain frequency of 650 MHz with Cs=Cf=2 pF and an external load of 4 pF.

Digital functional blocks, such as calibration processor and output encoder, are also integrated on the same chip. All digital circuits are synthesized with standard cells by commercial CAD tools. Total gate count is approximately 27,000. This design doesn't require any multi-bit multiplier.

An experimental ADC prototype was fabricated in a 0.25 μm 1P5M CMOS technology with MIM capacitors [3]. Fig. 9 shows the ADC's chip micrograph. Chip area is 3.8x3.6 mm^2. Operating at 40 MS/s sampling rate under a single 2.5 V supply, the analog block consumes a total of 350 mW of power, while the digital block consumes only 20 mW. Operating at 40 MS/s sampling rate, the ADC achieves a signal-to-noise-plus-distortion ratio (SNDR) of 73.5 dB and a spurious-free-dynamic-range (SFDR) of 93.3 dB with a 8-MHz sinusoidal input.

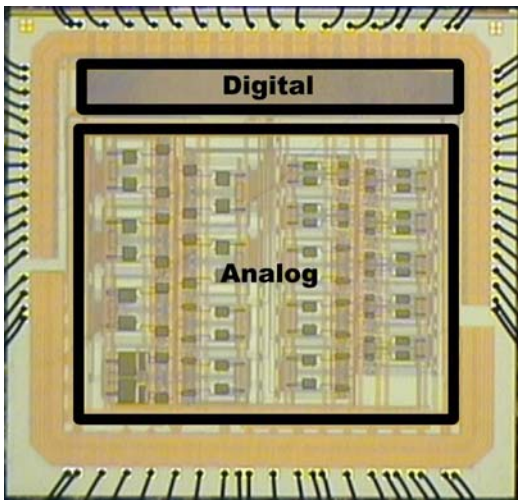

Fig 9: ADC chip micrograph.

四、結論

本計畫延續先前的計畫，將以 Time-Interleaved 架構設計 ADC。而此架構的主要問題包括取樣時間誤差以及子系統不匹配等。本計畫將繼續探討這些問題，並提出解決方案。

本計畫已成功設計出一個高性能的取樣電路。此電路利用 Time-Interleaved 架構的操作特性配合創新電路，可以簡化運算放大器之設計，進而降低功率消耗。

本計畫在 Pipelined ADC 設計方面有突破性的成果。所提出的 Digital Background Calibration 技術可以解決困擾多年之 Calibration 需停止正常 A/D 轉換的問題。此技術已申請專利。而利用此技術，我們已設計且成功製作了一個 15-Bit 40 MS/s 之 ADC 晶片。此晶片並且發表於國際知名的 ISSCC 上。

本計畫所發表的論文皆可放在主持人的網頁上：http://www.cc.nctu.edu.tw/~jtwu。

六、參考文獻

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