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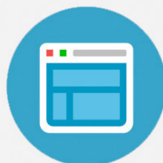

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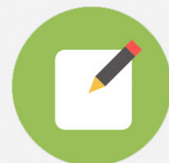

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Fabrication of sub-100-nm metal-oxide-semiconductor field-effect transistors with asymmetrical source/drain using I-line double patterning technique

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The authors present a simple double patterning technique with I-line stepper to define nanoscale structures and have successfully fabricated *n*-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) with sub-100-nm gate length. With this approach, polycrystalline silicon (poly-Si) gate with linewidth down to 80 nm could be formed with good control, which far exceeds the resolution limit of conventional I-line lithography. Moreover, ineffectiveness of end point detection in the second poly-Si gate definition is also addressed. For reliable process control in the second etching step, appropriate mask design is found to be essential. Finally, sub-100-nm MOSFETs with or without halo implemented symmetrically or asymmetrically are fabricated and characterized. © *2011 American Vacuum Society.* [DOI: 10.1116/1.3551527]

I. INTRODUCTION

Lithography has been playing a pivotal role in semiconductor manufacturing since the advent of integrated circuit (IC). Actually the successful evolution of IC technology strongly relies on the advancement of lithography tools and associated processes. To this date, immersion ArF-193 tools have been employed for 32 nm node manufacturing.[1] However, this is achieved at the expense of the skyrocketing equipment and process cost. The advanced tools suitable for high-volume manufacturing are usually out of reach in university-based laboratories. As a result most of the experimental studies on nanoscale devices carrying out in universities rely on alternative techniques such as photoresist (PR) ashing,[2,3] e-beam writing,[4] and imprinting[5] or using bottom-up approach (e.g., metal-catalytic growth[6]) to form the nanoscale structures.

I-line steppers have been employed for a long time for both manufacturing and research purposes, and the associated lithographic process is very mature and reliable. However, for conventional I-line process the generated PR pattern width is typically 0.3 μm or wider. Although nanoscale dimensions can be achieved by combining with the PR ashing technique,[2,3] it requires a highly stable asher to ensure good reproducibility and uniformity of critical dimension (CD) of the printed patterns. Besides, rounding of the top PR can be another concern for subsequent etching step.[3] On the other hand, immersion ArF-193 and deep ultraviolet (DUV) lithography are capable of generating nanoscale patterns. However, the immersion ArF-193 and DUV tools are outrageously expensive. Accounting for the tool and maintenance cost, most of studies carried out in universities thus opt for e-beam lithography to generate nanopatterns. Nonetheless, the scheme suffers from a very low throughput as compared with photolithography methods.

In this work, we propose a simple method which combines both I-line lithographic process and double patterning (DP) technique to address the above issues. As compared with the e-beam direct writing method, I-line process excels in throughput but is much worse in resolution capability which is limited by the optical diffraction phenomenon. On the other hand, DP technique which typically requires twice lithographic and/or etch steps has been proposed to increase the density of devices[7,8] and has also been demonstrated with the capability of breaking the resolution limit of an optical system.[9,10] As a matter of fact, it has been considered as a viable approach for sub-32-nm nodes by integrating with the immersion ArF-193 process.[11] Even with the I-line process, generation of structures with nanoscale dimensions is expected if the DP technique is incorporated. In this work we explore such feasibility by successfully fabricating sub-100-nm *n*-channel metal-oxide-semiconductor field-effect transistors (*n*-MOSFETs). Additional merit associated with the process demonstrated in this work is the implementation of asymmetrical source/drain (S/D) which could increase the flexibility in device design. Such capability is lacking with the aforementioned e-beam and PR ashing techniques. Nonetheless, an issue encountered in polycrystalline silicon (poly-Si) gate etch step of the present approach is also presented

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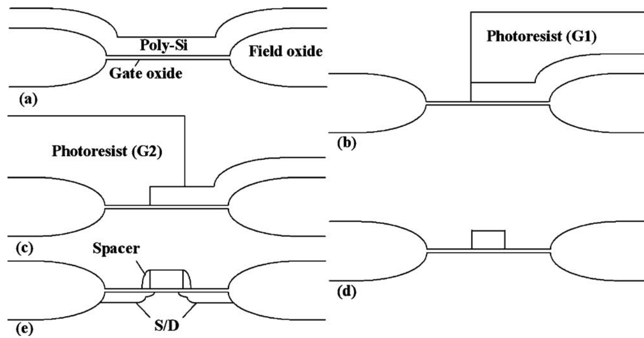

FIG. 1. Major process steps for fabricating *n*-MOSFETs with the DP method. (a) Formation of gate oxide and poly-Si on Si wafer with LOCOS isolation. (b) Generation of first PR pattern (G1), followed by the first poly-Si etching. (c) Generation of second PR pattern (G2) after removing the first PR. (d) Completion of the poly-Si gate after second poly-Si etching and subsequent PR removal. (e) Formation of S/D structure.

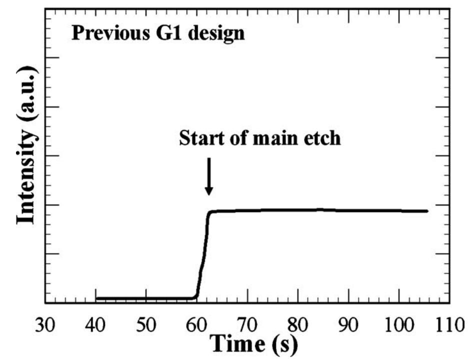

FIG. 3. Typical optical emissive signal recorded during the main etching stage of the second gate etching with the original mask design. No end point was detected.

and discussed. The characteristics of fabricated devices with symmetrical or asymmetrical S/D are analyzed and discussed.

II. DOUBLE PATTERNING METHOD

Figure 1 illustrates the major process steps in the fabrication of *n*-MOSFETs with the DP technique. For all lithographic steps carried out in this work, we used an I-line stepper (Canon FPA-3000i5+) to generate PR patterns. First, local oxidation of Si (LOCOS) was used for device isolation. Then, after *p*-well and threshold-voltage (V_{th}) adjustment implantations, thermal gate oxide of 3 nm was grown in a N_2O ambient, followed by the deposition of a 150 nm *in situ* phosphorous-doped poly-Si, as shown in Fig. 1(a). Subsequently, DP technique was executed to pattern the poly-Si gate. This procedure employed two masks denoted as G1 and G2 to define the gate electrode, as shown in Fig. 2. The two lithographic processes of G1 and G2 were aligned with the preexisting zero-layer alignment mark formed on the wafer. Mask G1 was first applied to generate PR patterns covering portion of the poly-Si, as shown in Fig. 1(b), followed by a reactive ion etch (RIE) step to remove the uncovered poly-Si. The second lithographic step with mask G2 was then employed to generate PR patterns which covered portion of the poly-Si layer remaining on the surface of the substrate [Fig. 1(c)], followed by a RIE step to complete the final poly-Si structure. As can be seen in Fig. 2, the most critical portion in the design is the overlapped region of the two gate patterns in the active area which determines the channel length (L_{ovp}) of the fabricated device. After the gate patterning [Fig. 1(d)], the remaining process steps follow the conventional flow, namely, source/drain extension implant, sidewall spacer formation, and deep S/D implant [Fig. 1(e)].

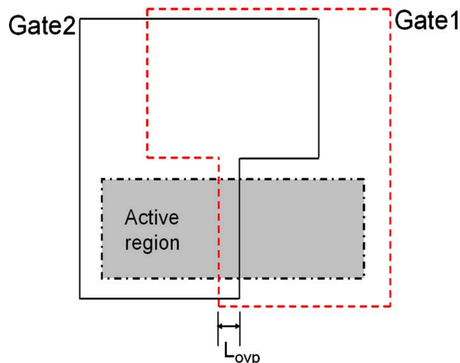

FIG. 2. (Color online) Layouts of the first (G1) and second (G2) gate patterns for defining the gate pattern on the active region. Gate length (L) of the final gate is determined by the overlap region of the two gate patterns.

III. END POINT DETECTION ISSUE

During device fabrication, a major issue related to the ineffectiveness of end point detection (EPD) in the second poly-Si etch step was found. Figure 3 shows the evolution of optical emission signal intensity during the second poly-Si etch on a test wafer. Normally the end point should be detected at around 20 s after the turning on of plasma, but this did not happen and the signal remained stable. Moreover, the signal intensity appeared to be much weaker than that recorded during the first poly-Si etch. Since the signal intensity is related to the etch by-products,[12] this is believed to be related to the layout design of mask G1. In the original version of G1 mask, over 90% of the blanket poly-Si area is not covered by the PR and is etched off in the first poly-Si etch step, so the end point (defined as the moment when the intensity drops to 90% of the peak intensity) can be easily detected in the main etch stage of the first etch step. However, with the scanty poly-Si left during the second etch, only a very weak optical signal is detectable, causing the failure of EPD.

Owing to the ultrathin gate oxide, EPD failure may cause the breakthrough of the gate oxide and result in device failure. Figure 4 illustrates the cross-sectional scanning electron microscopy (SEM) image of a MOSFET showing a recess in the Si substrate at the right side of the gate, an indication of the damage induced in the second etching process. When this happens, the devices exhibit very leaky characteristics and are no longer suitable for practical application.

The above issue could be resolved by modifying the layout design of the mask G1. This was done by adding dummy

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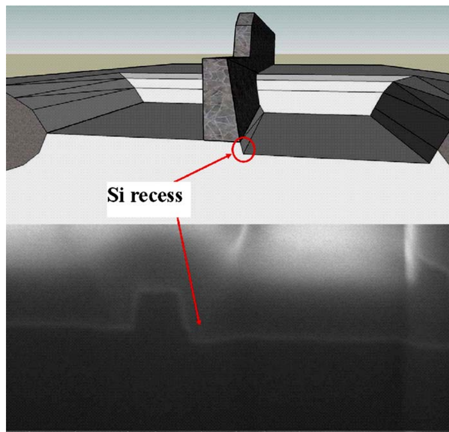

FIG. 4. (Color online) Cross-sectional SEM view of a MOSFET showing an etch-induced recess at the right side of the gate. Top illustration is used to help visualize the structure. The recess was formed during the G2 etching stage due to the failure of EPD.

patterns to the layout of the mask G1 to boost the remaining area of the poly-Si film after the first etching step. These dummy patterns removed in the second etching step could contribute more etch by-products and increase the optical signal for effective EPD. The feasibility of the modified mask design is evidenced by the EPD results recorded during the first and second poly-Si gate etchings shown in Figs. 5(a) and 5(b), respectively. In the two etching steps EPD could both be successfully carried out. To further highlight the effectiveness of the new layout design, the in-line SEM pictures of the poly-Si line after the second etch with original and modified layout are shown in Figs. 6(a) and 6(b), respectively. An obvious etch-induced damage region, corresponding to the Si recess region shown in Fig. 4, is observed at the right side of the gate in Fig. 6(a). In Fig. 6(b), with the modified layout, such damage could be completely eliminated.

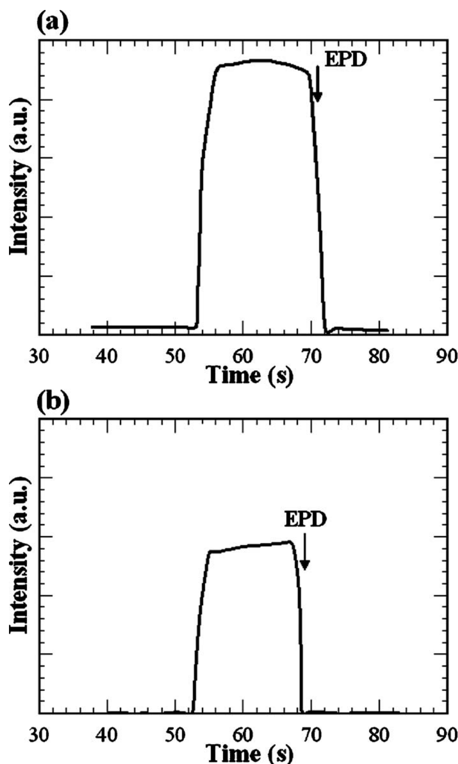

FIG. 5. Optical emissive signal recorded during the main etching stage of the (a) first and (b) second gate etchings with the modified mask design. Successful EPD is achieved in the two etch steps.

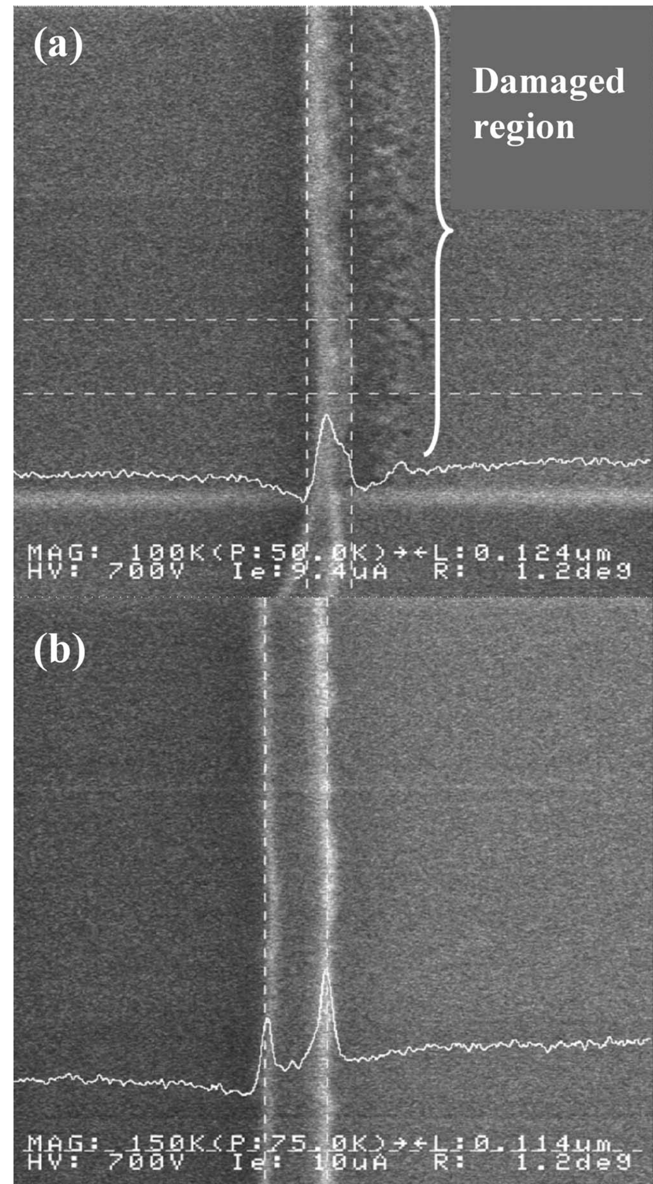

FIG. 6. In-line SEM views of gate patterns on active region etched with (a) original and (b) modified mask designs. The etch recess phenomenon can be resolved with the modified mask design.

IV. CRITICAL DIMENSION CHECK

In-line SEM was employed to measure the linewidth of patterned poly-Si gates. The results are shown in Fig. 7. Here, the horizontal axis is the nominal designed value denoted as L_{ovp} and the vertical axis is the actual value after the gate formation process mentioned in Sec. II, denoted as L_{poly}.

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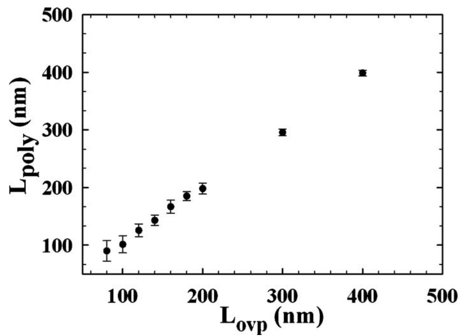

FIG. 7. Measured poly-Si gate length (L_{poly}) is shown as a function of nominal gate length (L_{ovp}).

As can be seen in this figure, the dimensions of the printed polygates are close to those of the mask patterns. Figure 8 shows the cumulative plots of the measured poly-Si gates with nominal lengths of 80, 300, and 400 nm, patterned with the DP technique. Also shown in the figure are the results of poly-Si gates with nominal length of 350 nm patterned with conventional I-line technique. In the figure each curve represents measured data obtained from 35 test samples distributed across the test wafer. The results clearly demonstrate the capability of this approach not only to shrink the gate length beyond the resolution limit of single patterning technique (>300 nm) but also to achieve a better dimension control as compared with conventional I-line process. Even with a much smaller gate dimension, the distribution in the measured gate width of the DP-patterned lines is obviously tighter than that of the conventional I-line method. Since the feature sizes of G1 and G2 patterns are much larger than the resolution limit of the I-line stepper, the CD variation is strongly dependent on the alignment accuracy of the exposure tool. According to the specifications of the employed stepper provided by the vendor, the overlay accuracy (3σ) is about 45 nm. This value is close to the deviation of the measured data (51 nm) with the DP technique shown in Figs. 7 and 8. In other words, the overlay accuracy of the exposure tool sets the limit for the CD control of the present approach. This may result in a noticeable variation in device characteristics as its dimensions are small. Fortunately, such concern can be relieved with a modification in process steps to tailor the device structure. An example is the implementation of asymmetrical S/D, which is characterized and discussed in Sec. V.

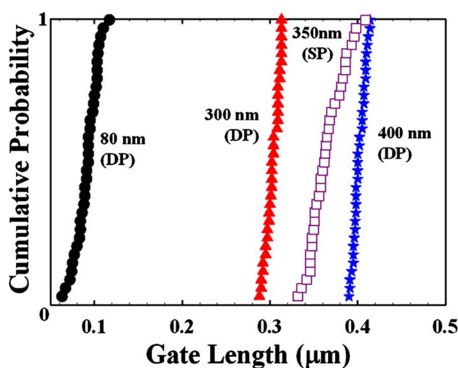

FIG. 8. (Color online) Cumulative plots of poly-Si gates patterned with DP method with nominal lengths of 80, 300, and 400 nm and with conventional single patterning with nominal length of 350 nm. Each curve represents the results measured from 35 test structures.

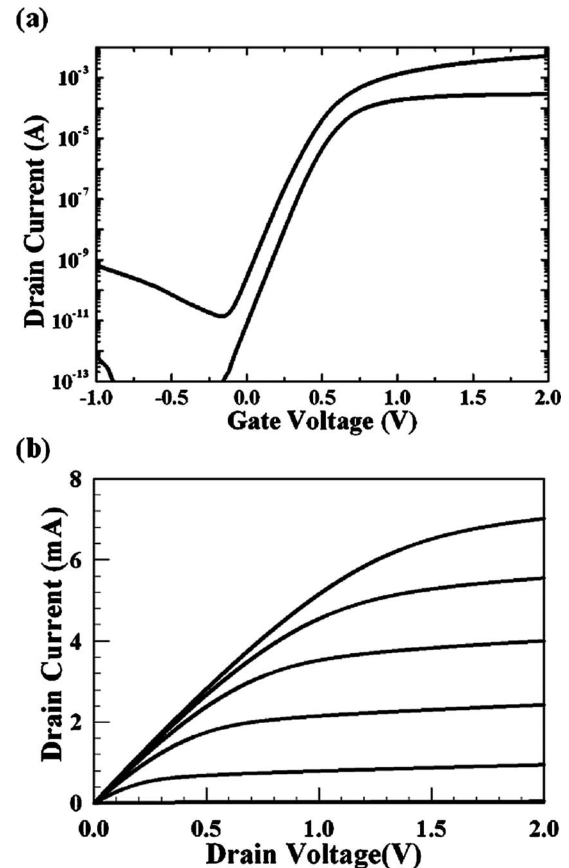

FIG. 9. (a) Transfer characteristics measured at $V_D=0.05$ and 1.5 V and (b) output characteristics of a control device with gate length of 100 nm and width of 10 μm measured at $V_{GS}-V_t=0-2$ V and step=0.4 V.

V. DEVICE CHARACTERISTICS

Figures 9(a) and 9(b) show the transfer and output characteristics of a MOSFET with $L=100$ nm fabricated with the process flow illustrated in Figs. 1(a)–1(e). In this case the shallow S/D extensions were formed by implanting As^+ (10 keV, 1×10^{15} cm^{-2}). After forming a 100 nm tetraethoxysilane oxide sidewall spacer, deep S/D junctions were formed by implanting As^+ (20 keV, 5×10^{15} cm^{-2}) and then annealed at 1000 °C for 10 s. Good device performance with drain induced barrier lowering (DIBL) of 119 mV/V and subthreshold swing of 80 mV/dec is obtained. These results are comparable to those presented in previous work on devices fabricated with DUV (193 nm) lithography.[13] We have also characterized the devices with $L=80$ nm and typical transfer characteristics are shown in Fig. 10. Figure 11 is a SEM picture showing the cross-sectional image of the device. Obviously, as compared with the results shown in Fig. 9, the device shows significant short-channel effect in terms of high subthreshold leakage and large DIBL. To address this

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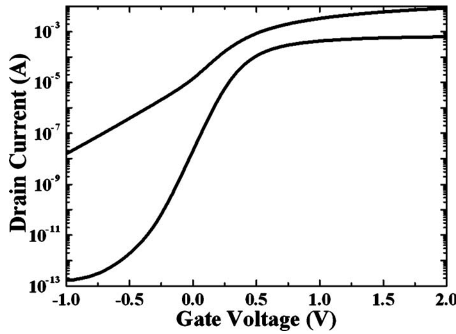

FIG. 10. Transfer characteristics of a control device with gate length of 80 nm and width of 10 μm measured at V_D=0.05 and 1.5 V. As compared with the device characteristics shown in Fig. 9(a), a much higher subthreshold leakage is observed in the device.

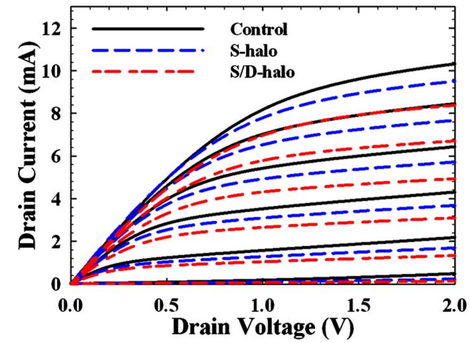

FIG. 12. (Color online) Output characteristics of control, S/D-halo, and S-halo n-MOSFETs with L=80 nm measured at $V_{GS}-V_t$=0–2 V and step=0.4 V.

issue, we have further implemented the halo scheme[14] in the device fabrication and the results are presented later.

Historically MOSFET fabrication usually adopts symmetrical S/D structure because of its simplicity and relatively lower cost as compared with the asymmetrical counterparts. In principle, an asymmetrical S/D, having different source and drain doing profiles in terms of doping concentration, junction depth, and even doping type, can offer more freedoms for device performance optimization,[15–17] but its formation may need additional lithographical and implantation steps in conventional single patterning scheme. In contrast, the DP method lends itself nicely to the implementation of an asymmetrical S/D. For example, we can perform the implantation of source- and drain-side extensions individually and specifically after the first [Fig. 1(b)] and second [Fig. 1(c)] etch steps of poly-Si gate, respectively, so a greater flexibility in extensions' profile design can be obtained. Moreover, implementation of one-side halo doping[15] for controlling the short-channel effects is also feasible with the DP approach. In this regard, we have fabricated and characterized three types of devices. The process flow of these devices is basically the same as that described previously for the devices shown in Figs. 9(a), 9(b), and 10, except the addition of several steps for forming the halo doping wherever necessary. One of the three types of devices denoted as "control" has no halo implemented. The devices characterized in Figs. 9(a), 9(b), and 10 belong to this category. The second type, denoted as "S/D halo," has halo doping embedded symmetrically in both source and drain. The last type denoted as "S halo" has halo doping embedded only in the source side. The former two types are symmetrical, while the last one is asymmetrical in structure. Halo implants were done with BF_2^+ (5×10^{12} cm^{-2}/50 keV/45° tilt angle). For the S/D-

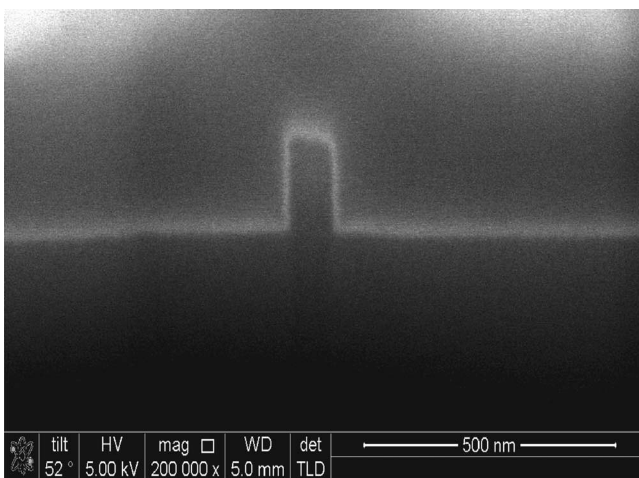

FIG. 11. Cross-sectional SEM image of an 80 nm poly-Si gate formed on active region.

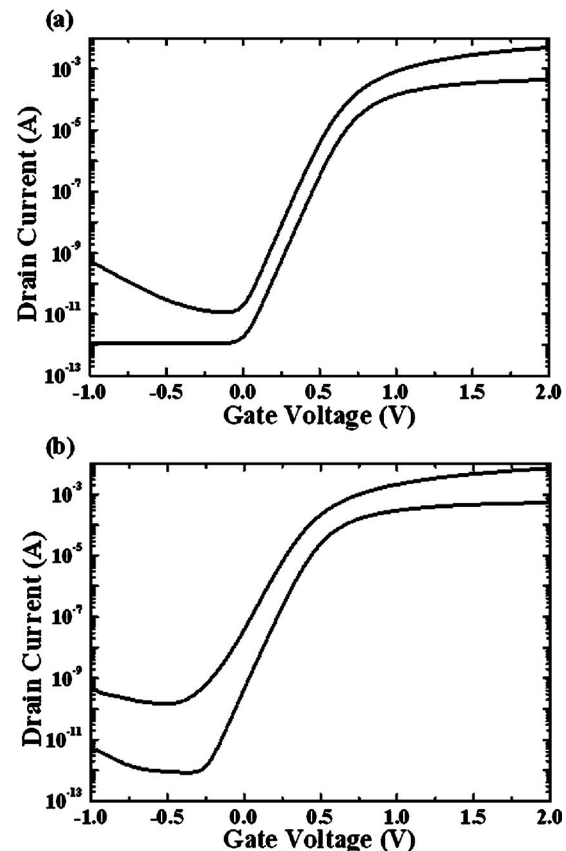

FIG. 13. Transfer characteristics of (a) S/D-halo and (b) S-halo n-MOSFETs with L=80 nm measured at V_D=0.05 and 1.5 V.

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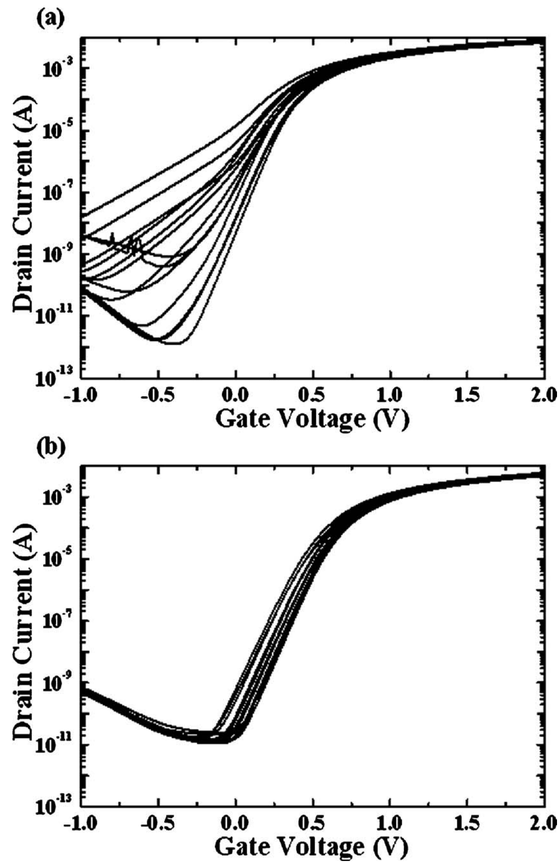

FIG. 14. Transfer characteristics of (a) 15 control and (b) 15 S/D-halo n-MOSFETs with $L=80$ nm measured at $V_D=1.5$ V.

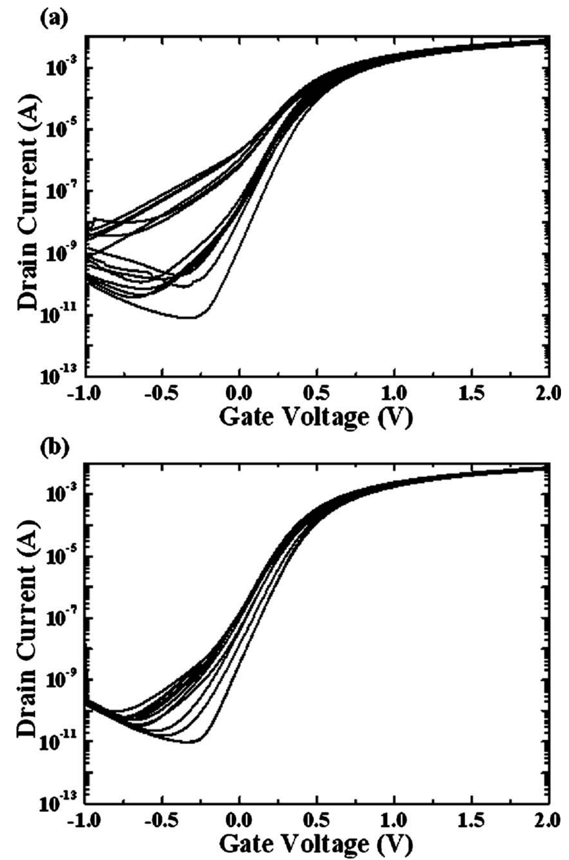

FIG. 15. Transfer characteristics of 15 S-halo n-MOSFETs with $L=80$ nm measured at $V_D=1.5$ V for (a) forward mode and (b) reverse mode. Forward mode is measured with the source grounded and the drain is applied with 1.5 V, while reverse mode is with the role of S/D switched.

halo split, the halo doping was performed after the extension implant [Fig. 1(d)]. For the S-halo one, it was done after the first gate etch [Fig. 1(b)]. Figure 12 shows and compares the output characteristics of the three types of devices. To evaluate the variation in device characteristics, each device shown in the figure represents the results from 15 test devices with nominally identical dimensions and mean performance among its group. As can be seen in the figure, the implementation of the halo doping tends to decrease the current drive. This is reasonable since halo introduces extra substrate doping in the channel and thus the carrier mobility is degraded. Nonetheless, the effectiveness of halo in alleviating the short-channel effects is evidenced by the transfer characteristics shown in Figs. 13(a) and 13(b) for S/D halo and S halo, respectively. In the figures, obviously, the two-sided halo is more effective than the one-sided halo. However, the degradation in on current with the introduction of halo is relaxed with the S halo, as shown in Fig. 12.

Another important merit of halo is the tightened variation of device characteristics. This can be understood with the transfer characteristics of control and S/D-halo devices shown in Figs. 14(a) and 14(b), respectively. In Fig. 15 devices of each type were measured at drain bias (V_D) $=1.5$ V. Clearly the S/D halo can help to reduce device variation. Similar measurements were also performed on S-halo devices, and the results are shown in Figs. 15(a) and 15(b) for forward and reverse modes of operation, respectively. Here, forward mode means the normal operation condition, while reverse mode is with the drain grounded and the source applied with 1.5 V. The results clearly show that the reverse mode exhibits a tighter distribution of the current-voltage curves, confirming the ability of drain-side halo in preventing the penetration of electric field from the nearby junction into the channel.

Finally, it should be noted that the feature of easily incorporating asymmetrical S/D with the present DP scheme makes this approach also suitable for fabricating tunneling field-effect transistors (TFETs) which demand source and drain of different doping types in order to form the gated p-i-n structure.[18,19] This can be done by performing the source doping after the first gate etch [Fig. 1(b)] and the drain doping with opposite type after the second gate etch. In other words, TFET is an inherently asymmetrical device and usually needs more mask counts than conventional MOSFETs[20] to fabricate; it is thus well suited for the DP scheme reported in this work as far as nanoscale gate length is concerned.

VI. CONCLUSIONS

In this work we have successfully demonstrated the generation of sub-100-nm patterns using DP technique with an

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I-line stepper, which is far beyond the resolution capability of conventional single patterning I-line lithography. Through in-line and cross-sectional SEM characterizations the feasibility of this approach is confirmed. Although an extra lithographic and the corresponding etching steps are required in the approach, the overall throughput is still much higher than the e-beam lithography, while the processing cost is much lower than the DUV lithography. This approach has been applied in this work for device fabrication. Microtrench damage was observed in the preliminary experiments due to the ineffectiveness of EPD in the second gate etching step. This issue was resolved by adding dummy patterns in the layout design of the first gate mask. Another concern is the limit set by the overlay accuracy of the exposure tool. For more precise CD control, tools with improved overlay accuracy are needed. To examine the feasibility of the I-line DP process, 80 nm *n*-MOSFETs with symmetrical and asymmetrical Ss/Ds were fabricated and characterized. The results clearly indicate the usefulness of the proposed I-line DP technique for nanoscale device fabrication and the effectiveness of the asymmetric S/D for improving the device characteristics. The extra mask thus provides not only greatly enhanced capability in shrinking the device dimensions but also more flexibility in device fabrication.

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