行政院國家科學委員會專題研究計畫　期中進度報告

子計畫一：矽射頻元件模型與技術(2/3)

計畫類別： 整合型計畫
計畫編號： NSC92-2215-E-009-031-
執行期間： 92 年 08 月 01 日至 93 年 07 月 31 日
執行單位： 國立交通大學電子工程學系

計畫主持人： 荊鳳德

報告類型： 精簡報告

處理方式： 本計畫可公開查詢

中　華　民　國 93 年 5 月 10 日

行政院國家科學委員會補助專題研究計畫

□成果報告　　■期中進度報告

（計畫名稱）

矽射頻元件模型與技術（2／３）

計畫類別：□ 個別型計畫　　■ 整合型計畫

計畫編號：NSC 92－2215－E－009－031－

執行期間：　92 年　8 月　1 日至　92 年　7 月 31 日

計畫主持人：荊鳳德

共同主持人：

計畫參與人員：

成果報告類型(依經費核定清單規定繳交)：□精簡報告 ■完整報告

本成果報告包括以下應繳交之附件：

□赴國外出差或研習心得報告一份

□赴大陸地區出差或研習心得報告一份

□出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

處理方式：除產學合作研究計畫、提升產業技術及人才培育研究計畫、列管計畫及下列情形者外，得立即公開查詢

□涉及專利或其他智慧財產權，□一年□二年後可公開查詢

執行單位：交通大學電子所

中　華　民　國　九十二　年　　月　　日

一、 中文摘要

本計畫主要是在研究當射頻電晶體製程從0.18微米微縮至0.13微米時，雖然f_T增加了，但NF_{min}卻也隨之增加了約0.2dB而變差。使用50指數的0.18微米 MOSFET在頻率5.8 GHz時有最小的NF_{min}值0.93dB，而無論是增加閘極數或減少都會提高其雜訊指數，此雜訊指數與閘極數不正常的相依性在0.13微米的電晶體中可正確地藉由結合閘極電阻與基板效應的等效電路模型分析出。

二、 英文摘要

As scaling down the RF MOSFET from 0.18 to 0.13 μm technology nodes, the f_T increases but the NF_{min} becomes worse by increasing ~0.2 dB. A small NF_{min} of 0.93 dB is measured at 5.8 GHz in 0.18 μm MOSFET using 50 fingers but increases as either increasing or decreasing finger number. This abnormal dependence and higher noise at 0.13 μm is accurately analyzed by equivalent circuit model and due to the combined gate resistance and substrate effect.

三、 報告內容：

甲、 前言：

The performance improvement and circuit area reduction are the driving force for continuously scaling down the MOSFET into RF frequency regime [1]-[2]. However, it is not clear if the RF noise can also be continuously improved as scaling down the MOSFET [1]. Next, the dominant noise sources in RF MOSFET are still not quite understood and the optimized device layout for achieving minimum noise figure (NF_{min}) is also unclear. In this paper, we have studied the RF MOSFETs scaled from 0.18 to 0.13 μm technology nodes. The scaling gives better RF power gain and fT. However, we have found that the scaling did not give better NF_{min} but increasing by ~0.2 dB at the same gate width. We have used the well calibrated equivalent circuit model to analyze such abnormal effect and the multi-fingered layout to optimize the NF_{min}. The NF_{min} decreases with increasing gate finger to a small value of 0.93 dB at 5.8 GHz using 50 fingers layout in 0.18 μm MOSFETs. Similar decreasing NF_{min} with increasing gate finger is also found uisng 0.13 μm technology node. However, we have measured another abnormal increase of NF_{min} when increasing gate finger >50 in 0.18 μm device. From our equivalent circuit

model analysis, the decreasing NFmin with increasing gate finger is due to the decreasing thermal noise generated by nonquasi-static gate resistance (Rg-nqs) [2] that is due to the delayed turn-on in gate electrode. The thermal noise generated by Rg-nqs is also the primary noise source in RF MOSFETs. The abnormal NF_{min} increase at >50 fingers is due to the increasing parasitic shunt RC pass to substrate and modeled by Zg-sub. This is the fundamental limitation of RF technology on high conductivity Si substrates [3]-[6] and is especially important for passive transmission lines and inductors. The small increasing NF_{min} as scaling down from 0.18 to 0.13 μm technology node is also due to the increased Rg-nqs because of the smaller gate area and larger resistance as scaling down. Therefore, the scaling below 0.13 μm technology node may further degrade the RF noise unless a modified T-gate structure is used.

乙、 研究方法

The RF MOSFETs using 0.18 and 0.13 μm technology nodes are studied in this work. In additional to the low resistance silicide gate technology, the multi-fingered gate layout can further reduce the gate resistance by connecting in parallel. The finger width is 5 μm and the finger number is ranged from 20 to 70 at an increment of 10. The devices are characterized by DC I-V and 2-port S-parameters using HP8510C network analyzer from 300 MHz to 30 GHz. Then regular de-embedding procedure is followed to eliminate the parasitic effect of probe pad. The NF_{min} and associate gain are measured using standard ATN-NP5B Noise Parameter Extraction System up to 7.2 GHz that covers the most important frequency range for wireless communication. The extraction of dominate RF noise sources were performed by using an equivalent circuit model of intrinsic MOSFET with additional terminal resistance and shunt pass to ground at both input and output ports. To avoid non-physically based data in the equivalent circuit model, DC and low frequency data are measured and referred in circuit model.

丙、 結果與討論（結論與建議）

A. Measured NF_{min} in RF MOSFETs used for circuit:

Fig. 1 shows the circuit schematic of a typical two-stage low noise amplifier (LNA) [7]. From the RF circuit theory, the noise of the whole LNA is determined by the MOSFET in

the first stage. Therefore, the choosing proper MOSFET to have a lowest NF_{min} is the key factor for LNA.

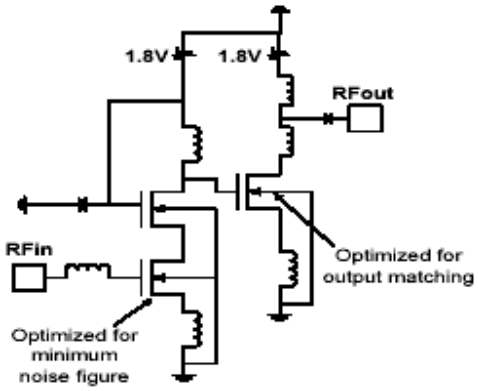

Fig. 1. The schematic of a two stage LNA. The MOSFET at first stage determines the minimum noise in LNA.

Fig. 2 shows the measured NF_{min} for RF MOSFETs at 0.18 and 0.13 μm technology nodes. The measured NF_{min} shows a general trend of decreasing RF noise with increasing the gate finger for MOSFETs in both technology nodes. A small NFmin of 0.93 dB is measured at 5.8 GHz using 50 gate fingers in 0.18 μm case, which shows the excellent noise performance at such high frequency and can be used for wireless LAN application. However, the NF_{min} increases by ~0.2 dB as scaling down from 0.18 to 0.13 μm technology node, which is opposite to the scaling trend. In addition, an abnormal increase of NF_{min} is observed as gate fingers increasing >50 in 0.18μm case.

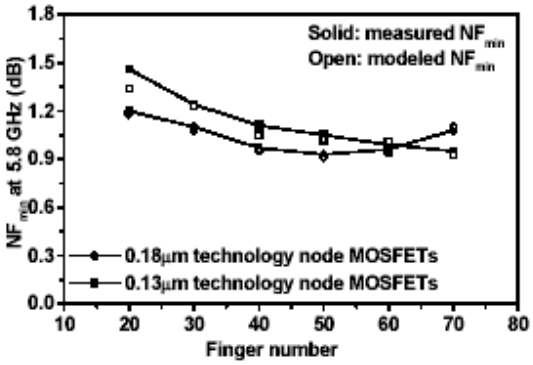

Fig. 2. The measured NFmin of RF MOSFETs at 0.18 and 0.13 μm technology nodes. The scaling from 0.18 to 0.13 μm technology gives a worse NF_{min}. An abnormal increase of NF_{min} at gate finger > 50 is also observed in 0.18 μm case. The modeled data is fromthe equivalent circuit model in Fig. 7.

It is noticed that the measured NFmin of MOSFET at 0.13 μm node is comparable with the data published in the literature by IBM [1]. Therefore, the increasing NF_{min} in 0.13 μm case may be intrinsic to device physics rather than the different technology among different companies. Fig. 3 shows the associated gain measured at 5.8 GHz under NF_{min} condition. A decreasing trend of associated gain with increasing gate finger is measured for both MOSFETs using 0.18 and 0.13 μm technology nodes. Therefore, the decreasing RF noise in Fig. 1 is traded off by the decreasing associated gain. The reason why such decreasing associated gain is explained by following relation derived from equivalent model [2]: Although the decreasing RF noise is achieved by decreasing Rg-nqs using parallel gate fingers, the increasing finger number also increases the undesired Cgd that decreases the associated gain.

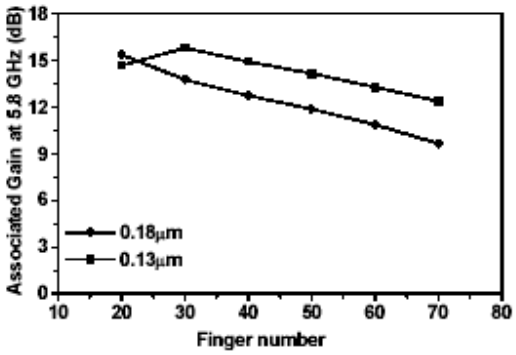

Fig. 3. The associated gain measured at 5.8 GHz under NF_{min} condition for RF MOSFETs at 0.18 and 0.13 μm technology nodes. The scaling from 0.18 to 0.13 μm gives higher associated gain but increasing finger number decreases the associated gain.

The increasing gate finger for achieving lower RF noise is also trades off the decreasing f_T. Fig. 4 shows the f_T of MOSFETs using 0.18 and 0.13 μm technology nodes. The scaling from 0.18 to 0.13 μm technology improves the f_T to ~100 GHz that shows the good device performance. It is noticed that the f_T decreases as increasing the number of gate fingers, which can be understood by following relation [2]: The increasing finger

number improves the RF noise but also increases the parallel Cgd that decreases the f_T.

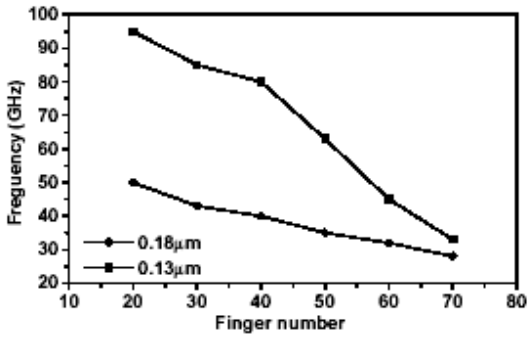

Fig. 4. The finger number dependent f_T of RF MOSFETs using 0.18 and 0.13 μm technology nodes. The increasing finger number decreases the f_T.

The large gate finger number layout in RF MOSFET not only achieves a lower RF noise but also has better output matching. Fig. 5 shows the S22 of MOSFETs at 0.13 μm nodes. The increasing gate finger shifts the measured S22 and pushes the output resistance of MOSFET (by extending the S22 to low frequency) close to 50 Ω. This is important to choose the proper transistor layout at second stage of LNA shown in Fig. 1.

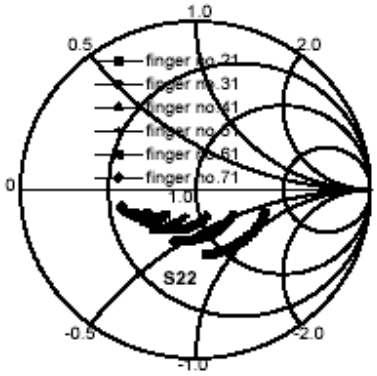

Fig. 5. The measured S22 of RF MOSFETs in 0.13 μm nodes. The increasing finger number shifts the output resistance of S22 and close to the desired 50 Ω.

B. NF_{min} analysis using self-consistent model of S-parameter & NF_{min}:

To further analyze the RF noise, we have developed a self-consistent model for both S-parameter and NF_{min}. Figs. 6(a) and 6(b) show the measured and modeled S-parameters

using the model shown in Fig. 7. Good matching between measured and modeled S-parameters and DC I-V (not shown) are obtained for RF MOSFETs in 0.13 μm nodes with the smallest 20 and largest 70 gate fingers. The good agreement between measured and modeled data is also obtained in other gate fingers of MOSFETs using both 0.13 and 0.18 μm technologies.

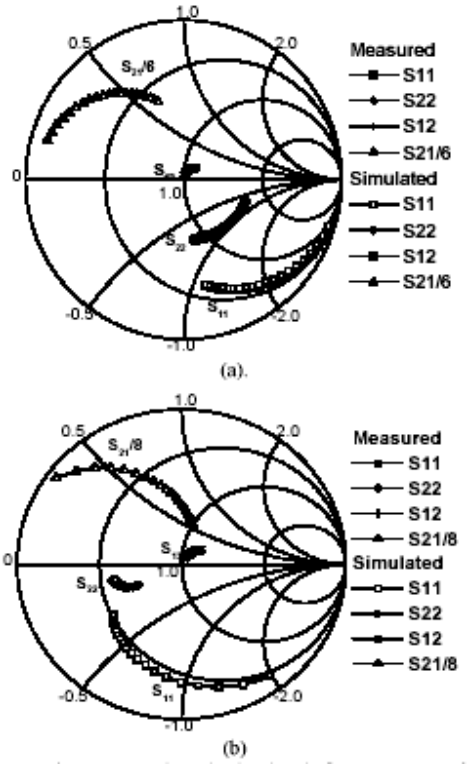

Fig. 6. The measured and simulated S-parameters of RF MOSFETs with (a) the smallest 20 fingers and (b) largest 70 fingers using 0.13 μm technology node. The S21 in (a) and (b) is divided by 6 and 8 respectively, to fit in the Smith chart.

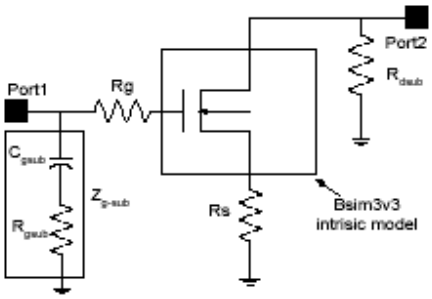

Fig. 7. The self-consistent model for DC I-V, S-parameters and NF_{min}.

Using the same model, we have further simulated the NF_{min} self-consistently with S-parameter and DC I-V. Figs. 8(a) and 8(b) show the measured and modeled NF_{min}. The good agreement between measured and modeled NF_{min} in Fig. 8 and other gate fingers and technology nodes in Fig. 2 indicates the good accuracy of the self-consistent model. Using the well-calibrated model, we have further analyzed the main noise source in MOSFETs. The Rg-nqs generates the dominate thermal noise in RF MOSFETs, which decreases as increasing parallel finger numbers. The Rg-nqs also increases with decreasing gate length from 0.18 to 0.13 μm nodes, which explains the abnormal increasing NF_{min} and opposites to the scaling trend. The next important noise source is from the shunt pass of Zg-sub. The increasing Zg-sub with increasing parallel gate fingers in 0.18 μm case fits well the abnormal increasing NF_{min} when gate finger > 50 as shown in Fig. 2. The Zg-sub represents the RF signal loss to shunt pass to ground, which has been identified as the primary RF technology challenge for circuits on current VLSI technology using low resistivity Si substrates [3]-[6].

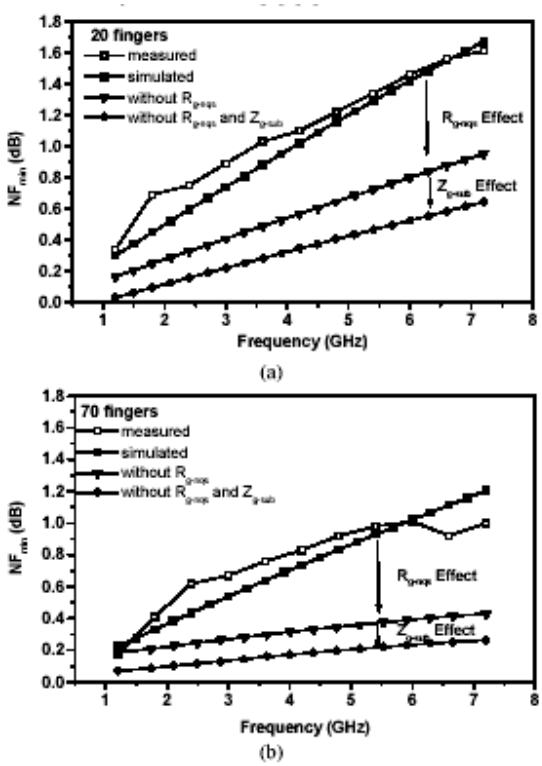

Fig. 8. The measured and simulated NF_{min} of RF MOSFETs with (a) the smallest 20 fingers and (b) largest 70 fingers using 0.13 μm technology. Good agreement is obtained for all other gate fingers and also for 0.18 μm case.

四、 參考文獻

[1] N. Zamdmer, A. Ray, J.-O. Plouchart, L. Wagner, N. Fong, K. A. Jenkins, W. Jin, P. Smeys, I. Yang, G. Shahidi, and F. Assaderaghi, “A 0.13- m SOI CMOS technology for lowpower digital and RF applications,” *VLSI Tech. Symp. Dig.*, pp. 85-86, June 2001.

[2] Y. H. Wu, A. Chin, C. S. Liang, and C. C. Wu, “The performance limiting factors as RF MOSFETs scaling down,” *IEEE RF-IC International Microwave Symp. Dig.*, pp. 151-154, June 2000.

[3] K. T. Chan, A. Chin, C. M. Kwei, D. T. Shien, and W. J. Lin, “Transmission line Noise from Standard and Proton- Implanted Si,” *IEEE MTT-S International Microwave Symp. Dig.*, pp. 763-766, June 2001.

[4] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, S. C. Pai, C. C. Chi, and C. P. Liao, “RF loss and cross talk on extremely high resistivity (10K-1M -cm) Si fabricated by ion implantation,” *IEEE MTT-S International Microwave Symp. Dig.*, pp. 221-224, June

2000.

[5] K. T. Chan, A. Chin, Y. B. Chan, T. S. Duh and W. J. Lin, “Integrated antenna on Si, proton-implanted Si and Si-on- Quartz,” *International Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 903-906, Dec. 2001.

[6] K. T. Chan, C. Y. Chen, A. Chin, J. C. Hsieh, J. Liu, T. S. Duh, and W. J. Lin, “40-GHz Coplanar Waveguide Bandpass Filters on Silicon Substrate,” *IEEE Wireless & Microwave Components Lett.* 23, no. 11, pp. 429-431, 2002.

[7] D. K. Shaeffer and T. H. Lee, “A 1.5V, 1.5 GHz CMOS Low Noise Amplifier,” *Symp on VLSI Circuit Dig.*, pp. 32-33, June

五、 計畫成果自評

The abnormal NF_{min} increases as scaling the MOSFET from 0.18 to 0.13 μm nodes has been identified by the increasing Rg-nqs. The abnormal increasing NF_{min} of 0.18 μm MOSFETs at gate finger > 50 is modeled by the increasing shunt pass loss to ground. Unless a T-gate MOSFET structure is used similar to III-V RF FET, the increasing gate resistance with continuous scaling is the fundamental limitation of RF noise in MOSFETs.