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# Improved Retention Characteristic in Polycrystalline Silicon–Oxide–Hafnium Oxide–Oxide–Silicon-Type Nonvolatile Memory with Robust Tunnel Oxynitride

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In this paper, we present a simple novel process for forming a robust and reliable oxynitride dielectric with a high nitrogen content. It is highly suitable for n-channel metal–oxide–semiconductor field-effect transistor (nMOSFETs) and polycrystalline silicon–oxide–hafnium oxide–oxide–silicon (SOHOS)-type memory applications. The proposed approach is realized by using chemical oxide with ammonia ($NH_3$) nitridation followed by reoxidation with oxygen ($O_2$). The novel oxynitride process is not only compatible with the standard complementary metal–oxide–semiconductor (CMOS) process, but also can ensure the improvement of flash memory with low-cost manufacturing. The characteristics of nMOSFETs and SOHOS-type nonvolatile memories (NVMs) with a robust oxynitride as a gate oxide or tunnel oxide are studied to demonstrate their advantages such as the retardation of the stress-induced trap generation during constant-voltage stress (CVS), the program/erase behaviors, cycling endurance, and data retention. The results indicate that the proposed robust oxynitride is suitable for future nonvolatile flash memory technology application. © 2011 The Japan Society of Applied Physics

## 1. Introduction

For conventional floating-gate flash memory devices, tunnel oxide thickness cannot be scaled below 7 to 8 nm owing to problems with stress-induced leakage current (SILC) that cannot meet the 10-year retention requirement.[1)] Recently, polycrystalline silicon–oxide–nitride–oxide–silicon (SONOS)-type nonvolatile memories (NVMs) have attracted much attention as one of the most promising candidates to replace the conventional floating-gate flash memory when the industry moves to 45 nm and beyond.[2–4)] On the basis of its discrete charge-trapping nature, the SONOS-type NVMs have the potential to achieve a low operation voltage, better endurance, and good compatibility with the conventional CMOS process. However, it is a challenge for SONOS-type NVMs to achieve fast programming and long retention simultaneously. Several attempts have been made to improve the SONOS performance and reliability, for example, band-gap engineering for the tunnel oxide[5)] or trapping layer[6)] to improve charge retention, and the use of high-$k$ dielectrics as a blocking oxide[7)] or trapping layer[8,9)] to improve program speed or retention characteristics. However, considering the density of trap states and deep trap energy levels, hafnium oxide ($HfO_2$) is expected to be a promising candidate for the charge-trapping layer for SONOS-type NVMs instead of $Si_3N_4$ film.[10)]

In addition, it has been reported that the oxynitride used as the tunnel oxide shows high immunity to the SILC for a longer data retention characteristic.[11,12)] Various approaches to produce modified oxides have achieved varying degrees of success, such as NO, $N_2O$, $NH_3$, or plasma nitridation.[13–16)] However, some studies have revealed that the amount and distribution of nitrogen atoms in the oxynitride must be optimized because an excessive or wrongly positioned peak nitrogen concentration would result in the deterioration of reliability.[17,18)] If the nitrogen atoms accumulate at the oxynitride/substrate interface, it will result in device performance degradation. Therefore, it should be better to keep a high nitrogen concentration away from the oxynitride/substrate interface.

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In this paper, robust nitrogen concentration profile engineering of the oxynitride is proposed with the aim of producing the peak nitrogen concentration away from the oxynitride/substrate interface. We further integrated this robust oxynitride with polycrystalline silicon–oxide–hafnium oxide–oxide–silicon (SOHOS)-type NVMs instead of a tunnel oxide film. Reliability measurement shows that the proposed robust tunnel oxynitride presents superior data storage performance than the conventional $SiO_2$ tunnel oxide. It is clear that the robust tunnel oxynitride is a very promising candidate for SOHOS-type NVMs beyond the 45 nm node.

## 2. Experimental Methods

Figure 1 shows the schematic cross section and process flow of the fabricated device used in this study. The n-channel SOHOS-type NVMs with gate stacks of a hafnium oxide ($HfO_2$) trapping layer were fabricated on 6-in. p-type (100)-oriented Czochralski (CZ) silicon wafers with a resistivity of 1–10 Ω·cm. After the standard RCA cleaning by a hydrofluoric (HF) acid-last process, the substrates were immersed in hydrogen peroxide ($H_2O_2$) solution for 20 min at room temperature to grow a 1-nm-thick chemical oxide layer, followed by conventional horizontal low-pressure chemical vapor deposition (LPCVD) furnace nitridation in ammonia ($NH_3$) ambient at 750 °C. Subsequently, the nitrided oxide was reoxidized by atmospheric-pressure chemical vapor deposition (APCVD) in a furnace in oxygen ($O_2$) ambient at 900 °C to form a robust tunnel oxynitride. Furthermore, conventional $SiO_2$ grown at 900 °C was also prepared to serve as the control sample. The thicknesses of the robust tunnel oxynitride and conventional oxide were ~2.5 and ~3 nm, respectively, measured by spectroscopic ellipsometry. Then, a $HfO_2$ trapping layer (~5 nm) was deposited with the AIXTRON metal organic chemical vapor deposition (MOCVD) system at 500 °C, followed by post-$HfO_2$-deposition annealing (PDA) in nitrogen ($N_2$) ambient at 700 °C for 30 s. The blocking oxide (~15 nm) was deposited by LPCVD TEOS [Si $(OC_2H_5)_4$], followed by the deposition of a 200-nm-thick polycrystalline silicon (poly-Si) gate in the LPCVD system using silane ($SiH_4$) gas at 620 °C. After gate patterning, a conventional self-aligned implantation was

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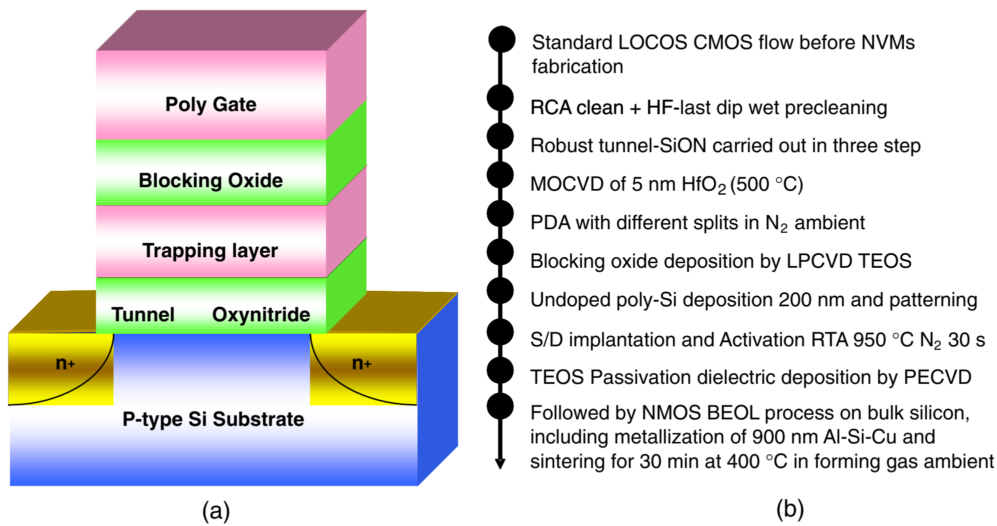


**Fig. 1.** (Color online) (a) Schematic cross section and (b) process flow of SOHOS flash memory with tunnel oxynitride.

**Table I.** Summary of gate stack equivalent oxide thickness ($EOT_{total}$) of the SOHOS with tunnel oxynitride and with conventional tunnel oxide for different post-$HfO_2$-deposition annealing (PDA) conditions.

| Conditions of PDA | | $EOT_{total}$ for the whole gate stack with tunnel oxynitride (nm) | $EOT_{total}$ for the whole gate stack with conventional tunnel oxide (nm) |
|---|---|---|---|
| Temperature (°C) | Time (s) | | |
| 700 | 30 | 19.5 | 20.2 |
| 700 | 60 | 20.5 | 20.8 |
| 800 | 30 | 20.5 | 21.1 |

applied to extend the $n^+$ source/drain with a phosphorous dosage of $5 \times 10^{15}\,cm^{-2}$ at an energy of 25 keV, and then was activated in $N_2$ ambient at 950 °C for 30 s. Finally, contact hole etching and Al metallization were performed using a standard complementary metal–oxide–semiconductor (CMOS) fabrication process, followed by forming gas annealing in $N_2/H_2$ ambient at 400 °C for 30 min to reduce the interfacial trap density. The transistor structures tested in this study have gate width to gate length dimensions of $W/L = 10\,\mu m/0.35\,\mu m$ for the nMOSFET and $W/L = 10\,\mu m/1\,\mu m$ for the SOHOS, respectively.

The electrical properties and reliability characteristics of such devices were measured using a Hewlett-Packard 4156C semiconductor parameter analyzer and a Hewlett-Packard 81110A pulse generator. The gate stack equivalent oxide thickness ($EOT_{total}$) was extracted from the high-frequency (1 MHz) capacitance–voltage ($C$–$V$) curves at a strong inversion without considering the quantum effect and is summarized in Table I. Furthermore, the distributions of the nitrogen and oxygen atoms in the robust oxynitride film were analyzed by secondary-ion mass spectroscopy (SIMS).

## 3. Results and Discussion

Figure 2 shows the SIMS depth profile of the proposed robust tunnel oxynitride. The results show that there is a high nitrogen concentration with a peak near the poly-Si/oxynitride (Poly/SiON) interface and a low nitrogen concentration in the oxynitride/substrate interface. The results indicate that the proposed approach is effective for the desirable nitrogen profile engineering to meet the requirement of device performance.

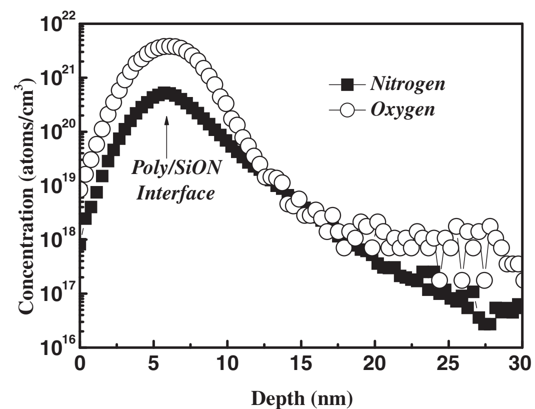


**Fig. 2.** SIMS profiles of nitrogen and oxygen distributions of robust oxynitride.

To study the reliability characteristics, nMOSFETs with the proposed robust oxynitride were fabricated. Constant-voltage stress (CVS) was subsequently applied to verify the robust oxynitride performance at room temperature by measuring the transfer curves and charge pumping to monitor the threshold voltage shift and the interface state density shift at various stressing times. Figure 3(a) shows the threshold voltage shift as a function of CVS time at effective electric fields of $E_{eff} = 10.6$ and 13.7 MV/cm. The stress-induced interface state trap generation is shown in Fig. 3(b). After CVS, both bulk trap generation (not shown) and interface trap generation decreased while the robust oxynitride process was introduced. This result can be attributed to the higher nitrogen concentration at the top interface (polysilicon/oxynitride) and the smooth surface at the bottom interface (oxynitride/substrate), which result in less electron trapping and interface state generation. It is clear that the robust oxynitride shows a higher reliability characteristic. Therefore, we further integrated the robust

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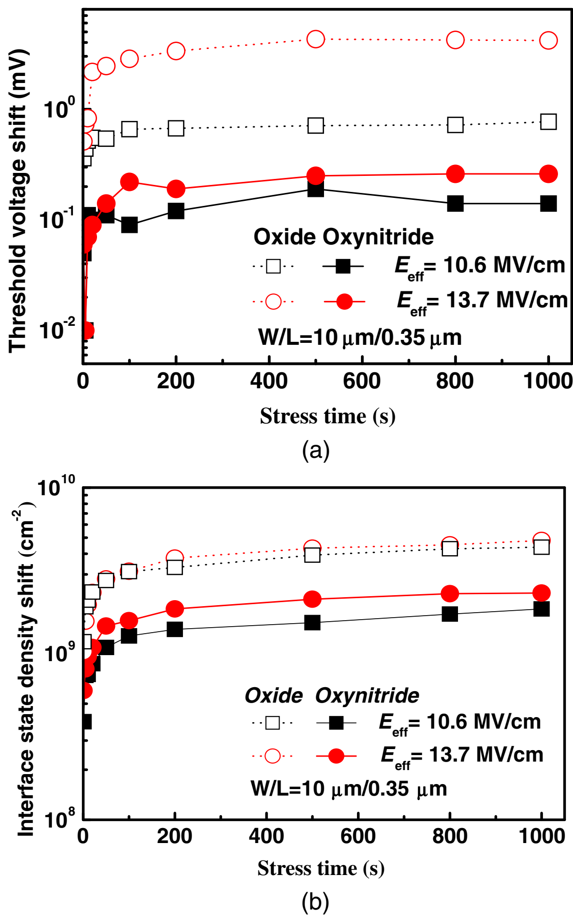


**Fig. 3.** (Color online) (a) Threshold voltage shift and (b) interface state density shift of nMOSFETs with robust oxynitride and with conventional oxide as gate dielectric during constant-voltage stress (CVS) at $E_{\mathrm{eff}} = 10.6$ and 13.7 MV/cm.

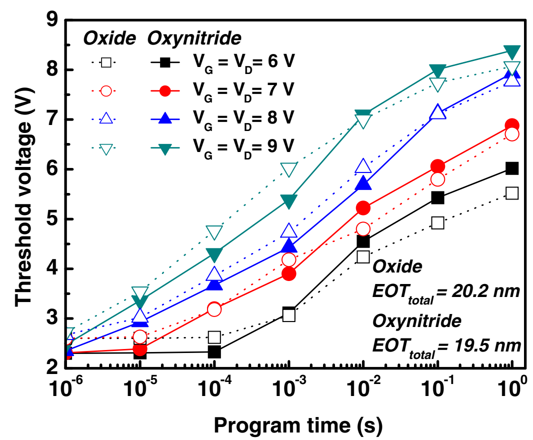


**Fig. 4.** (Color online) Program characteristics of SOHOS memory devices with tunnel oxynitride and conventional tunnel oxide under different program conditions. A memory window of SOHOS with tunnel oxynitride at about 3 V can be achieved with program operation at $V_{\mathrm{G}} = V_{\mathrm{D}} = 9$ V and 1 ms pulse width.

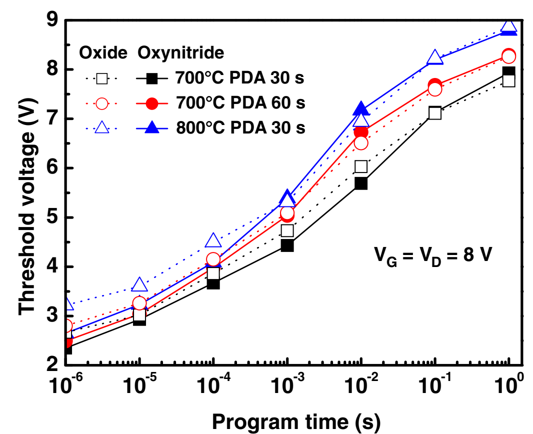


**Fig. 5.** (Color online) Program characteristics of SOHOS memory devices with tunnel oxynitride and conventional tunnel oxide with different post-$HfO_2$-deposition annealing conditions.

oxynitride into SOHOS-type NVMs and expected to reveal better device characteristics for NVM applications.

Figure 4 shows the program speed characteristics of the SOHOS-type NVMs with the proposed robust tunnel oxynitride and the conventional tunnel oxide. The initial threshold voltages $V_{\mathrm{th}}$ are ~2.3 and ~2.6 V for the tunnel oxynitride and tunnel oxide devices with PDA at 700 °C for 30 s, respectively. We used channel hot-electron injection (CHEI) for the programming under the bias conditions at (i) $V_{\mathrm{G}} = V_{\mathrm{D}} = 6$ V, (ii) $V_{\mathrm{G}} = V_{\mathrm{D}} = 7$ V, (iii) $V_{\mathrm{G}} = V_{\mathrm{D}} = 8$ V, and (iv) $V_{\mathrm{G}} = V_{\mathrm{D}} = 9$ V. The $V_{\mathrm{th}}$ of both devices increases with increasing applied gate and drain voltages, and the program speed can be as fast as a 1 ms pulse width with a 3 V memory window for the program condition at $V_{\mathrm{G}} = V_{\mathrm{D}} = 9$ V. This is because the higher the voltage applied is, the more hot electrons are generated. More electrons are able to cross the barrier height and are trapped in the $HfO_2$ film; thus, $V_{\mathrm{th}}$ increases. In addition, no significant difference in the program speeds (slopes) between the samples is observed.

Figure 5 shows the program characteristics with different pulse widths for the SOHOS-type NVMs with the tunnel oxynitride and conventional tunnel oxide with different PDA temperatures and durations. With an annealing temperature or duration increase, the program speed and the memory window of all the devices show similar increase trends. This indicates that a higher temperature or longer duration of PDA will induce greater $HfO_2$ trapping layer crystallization. Hence, a higher program speed can be obtained owing to the extra trapping level.[19,20]

The erase speeds of the SOHOS-type NVMs with the proposed robust tunnel oxynitride and conventional tunnel oxide are also shown in Fig. 6. We used the band-to-band hot hole (BTBHH) for erasing under the bias conditions at (i) $V_{\mathrm{G}} = -5$ V, $V_{\mathrm{D}} = 5$ V, (ii) $V_{\mathrm{G}} = -6$ V, $V_{\mathrm{D}} = 6$ V, (iii) $V_{\mathrm{G}} = -7$ V, $V_{\mathrm{D}} = 7$ V, and (iv) $V_{\mathrm{G}} = -8$ V, $V_{\mathrm{D}} = 8$ V, respectively. The erase speed of both devices increases as the gate voltage becomes more negative. The special saturated behaviors of both devices are observed with a high erase voltage. The over-erase phenomenon is minimized by using $HfO_2$ because $HfO_2$ is considered to act as a charge trapping layer, which means the holes have to tunnel through a much thicker barrier to the $HfO_2$ valence band in the erase operation.[20] Once all the programmed charges have been removed during erasing, the reduction of the

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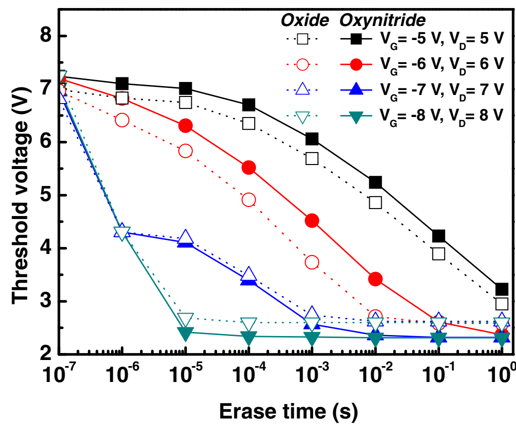


**Fig. 6.** (Color online) Erase characteristics of SOHOS memory device with tunnel oxynitride and conventional tunnel oxide at different erase voltages.

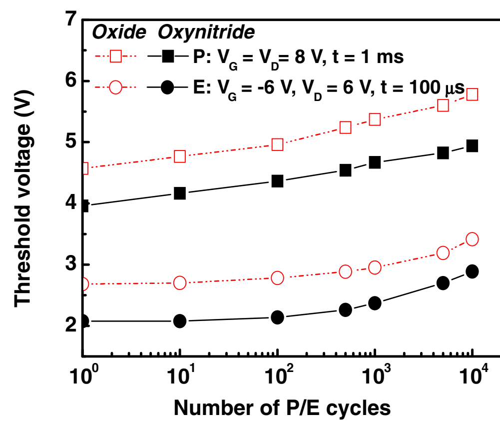


**Fig. 8.** (Color online) Endurance characteristics for SOHOS memory devices with tunnel oxynitride and conventional tunnel oxide.

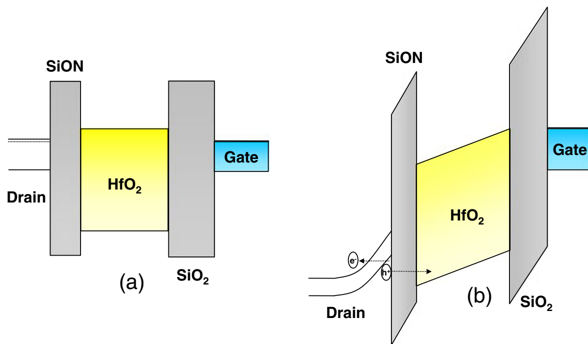


**Fig. 7.** (Color online) Energy band diagram of SOHOS NVMs with robust tunnel oxynitride under (a) flat band and (b) erase operation conditions.[20]

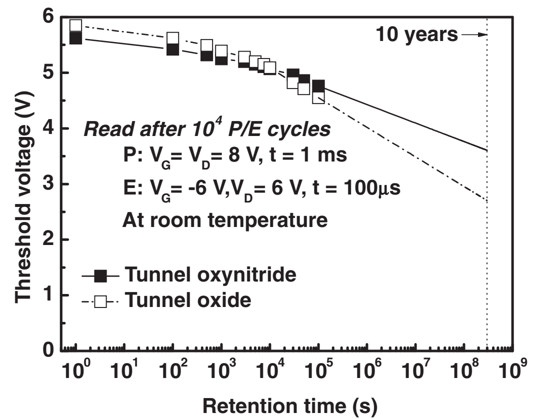


**Fig. 9.** Retention characteristics of tunnel oxynitride and conventional tunnel oxide for cycled SOHOS devices extrapolated to 10 years.

vertical electric field will make it difficult for holes to tunnel into the $HfO_2$ trapping layer. Therefore, the over-erase phenomenon is almost minimized in SOHOS devices. The ideal band diagram for SOHOS-type NVMs is also shown in Fig. 7.

Figure 8 shows the endurance characteristics of the SOHOS-type NVMs with the tunnel oxynitride and conventional tunnel oxide after $10^4$ program/erase (P/E) cycles. The device is programmed under $V_G = V_D = 8$ V for 1 ms, and is erased under $V_G = -6$ V and $V_D = 6$ V for 100 µs. We can observe that the memory window is slightly increased after the shift; this is attributed to the residual charge trapped inside $HfO_2$ not being discharged yet, therefore resulting in increasing the memory window slightly. The lack of significant window narrowing verifies the reliability of the SOHOS-type NVMs with the proposed robust tunnel oxynitride. For further study, Fig. 9 displays the retention characteristics of the devices after $10^4$ P/E cycles under the program conditions of $V_G = V_D = 8$ V for 1 ms and erase conditions of $V_G = -6$ V and $V_D = 6$ V for 100 µs. The $V_{TH}$ vs time at room temperature for cycled devices was extrapolated to 10 years. If the conventional tunnel oxide is replaced by a robust tunnel oxynitride, considerable improvement of the charge storage capability can be achieved. In contrast, the charge storage capability in conventional SOHOS-type NVMs after $10^4$ P/E cycles cannot even meet the 10-year charge storage capability. It is obvious that the robust tunnel oxynitride shows better stress immunity after P/E cycles. Hence, fewer defects being formed after P/E cycles for the robust tunnel oxynitride can result in higher post-endurance retention performance.

Long-term (10 years) retention is of concern for NVMs. $HfO_2$ is a dielectric film that has multiple electron traps, and each trap corresponds to one unique trap energy. It is unlike floating-gate memory, which is a conducting material in which its charges are stored at the conduction band. The study of data retention characteristics and charge loss mechanisms for scaled SONOS structures using ultrathin tunnel oxides has been reported.[21] Thermal excitation is the predominant mechanism of charge decay for temperatures above 150 °C. Moreover, with decreasing temperature, such as in an intermediate temperature range from 150 to 70 °C, the tunneling mechanisms of trapped electrons become more important. At room temperature, the tunneling processes dominate the discharge. Figure 10 illustrates the charge retention characteristics of the SOHOS-type NVMs with the tunnel oxynitride and the conventional tunnel oxide at room temperature and 125 °C, respectively. The retention data has


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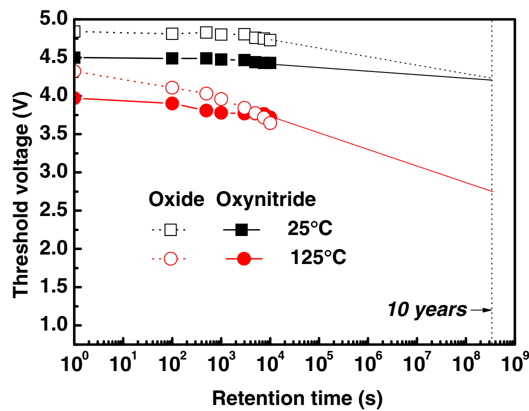


**Fig. 10.** (Color online) Retention characteristics of SOHOS memory devices with tunnel oxynitride and conventional tunnel oxide at temperature $T = 25$ and 125 °C, extrapolated to 10 years. Very low charge loss is seen for the device with the tunnel oxynitride even after $10^4$ s.

been extrapolated to 10 years. The results demonstrate that the room-temperature curve of the sample with the proposed tunnel oxynitride exhibits a better charge storage ability of ~93% at $3 \times 10^8$ s (10 years). Even at a temperature of up to 125 °C, the proposed device has a lower charge loss of ~36% compared with the conventional tunnel oxide. We speculate that both the thermionic emission and the tunneling processes contribute to the electron discharge of the $HfO_2$ trapping layer at 125 °C. We attribute the improved 125 °C retention in the proposed devices to fewer bulk defects and less interface trap generation in the tunnel oxynitride, resulting in less tunnel leakage and longer charge retention. We verified both the bulk defects and interface state in the oxynitride. The interface state densities of MOSFETs with the oxynitride and a oxide gate dielectric have been verified as $1.02 \times 10^{-11}$ and $1.95 \times 10^{-11}$ cm$^{-2}$, respectively. The stress-induced $V_{th}$ shift shows a small amount of shift of the oxynitride gate dielectric, which can also be ascribed to lower fresh bulk defect density. The results show that the oxynitride has fewer defects than the conventional tunnel oxide. This can explain why the device with the tunnel oxynitride has a lower charge loss than that with the conventional tunnel oxide. It can be inferred that the proposed device exhibits good retention characteristics for charge storage.

## 4. Conclusions

In this paper, we proposed a novel and simple technique for fabricating a robust, reliable, high-nitrogen-content oxynitride dielectric and its application to nMOSFETs and the SOHOS memory structure. The SIMS analysis indicated a peak of nitrogen distribution away from the oxynitride/substrate interface. Nitrogen profile engineering improved the reliability characteristics. Both bulk trap and interface trap density shifts were drastically suppressed during subsequent CVS. For further analysis, we have verified the performance of SOHOS-type NVMs in terms of the program/erase behaviors, charge retention, and endurance, such as a better charge storage ability of ~93% for extrapolated 10-year retention. The retention characteristic was significantly improved for the SOHOS device with the tunnel oxynitride. It was clear that the robust oxynitride possesses high potential for application to current or future nonvolatile flash memory technology.

## Acknowledgements

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