NSC92-2220-E-009-030-

92   11   01   93   07   31

93   5   31

積極低功率最佳化下之平面規劃
Floorplanning with Aggressive Power Optimization

計畫編號：92-2220-E-009-030
執行時間：92年11月01日至93年07月31日
主持人：陳宏明 助理教授 國立交通大學電子工程學系

一、中文摘要

在目前的許多積體電路設計中，低功率和功率認知的設計的重要性已經和先前我們注重的降低連線延遲和縮小面積的考量已不相上下了。這其中有兩個很重要的因素。第一是需要高速計算和複雜功能但必須消耗極少功率的可攜式應用急速增加。第二是功率消耗所產生的熱會增加封裝和冷卻的成本，同時縮短晶片的壽命。

在功率消耗極小化同時，我們著重於考慮降低操作電壓和實體設計上的權衡。我們以在双電壓設計上功率域/電壓島生成的想法為基礎，先做第一階段功率認知的置放，以期能使第二階段的平面規劃更盡理想。在系統單晶片的設計上使用電壓島的想法提供了有效的實體設計方法，使得某個區塊可以被關上，減少功率消耗。而為求設計實際化，我們加入許多新考量於設計中。我們要在平面規劃的區塊中找到最低操作電壓分配，使得晶片的功率消耗降至最低。我們採用一個以力平衡原理為基礎的的置放方法，可以在有計時限制下達到初步功率最低化。

關鍵字：功率認知、電壓島、平面規劃、置放方法

英文摘要(Abstract)

In designs nowadays, the importance of lowering power dissipation and power awareness design is given comparable weight to reduced interconnect delay and area minimization. Two factors mainly contribute to this trend. Firstly, there exists extreme

growth of portable applications which demand high-speed computation and complex functionality with low power consumption. Secondly, power dissipation will increase the packaging and cooling costs and shorten the life of ICs as well.

Our interests lie at the boundary between voltage scaling methods and physical design issues for power minimization. We develop a dual-voltage power domain/voltage island generation strategy, and plan to implement a power-aware floorplanning/placement system. The use of voltage islands at functional unit level in a System-on-a-Chip (SoC) provides an effective physical design approach to gating the power supply of the entire macro in order to completely turn it off. To be realistic, we add some new considerations into our design. We try to obtain the assignment of cells/blocks in a floorplan for their lowest operating voltage so that it can overall lower the power dissipation of the chip. In this first stage, we achieve initial power minimization under particular timing constraint by adopting a placement strategy which is based on force-balanced algorithm.

Keywords : power awareness, voltage island, floorplan, placement.

二、計畫的緣由與目的(Background and Objective)

1. Background

In deep submicron (DSM) era, power consumption issues become more and more important. Designers should put much effort to reduce the power consumption to make their design practical. [1, 2] also mentioned that for large designs in particular, design constraints due to power require a new methodology and flow, the early floorplanning stage is especially important since it is greatly constrained in DSM environment. For portable designs, power consumption especially becomes a major measure for the performance of the system.

Many researches have been trying to search for methods to reduce power consumption. The concept of multiple supply/threshold voltages is a main branch of such researches. We focus on applying multiple supply/threshold voltages techniques to physical design automation. Some design styles and relevant skills for multiple supply/threshold voltages have been introduced [3 - 6]. Figure.1 demonstrates such designs.
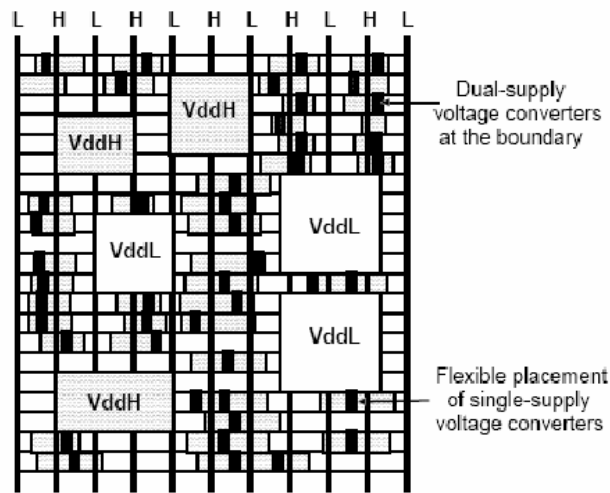
Figure1. Generic voltage island layout style [4].

We will use multiple supply voltage and voltage island concepts to develop algorithms for power-driven/timing-aware floorplanning/placement.

2. Objective

Our goal is to develop an efficient-yet-effective active and static power reduction floorplanning/placement framework to handle the floorplanning and packing for VLSI chips. For digital systems with a single supply voltage, some logic devices typically operate faster or more frequently than necessary, consuming extra power. This motivates the need for multiple-voltage design for an aggressive power optimization as slow operation allows a reduced voltage level. We will build an efficient multiple-supply-voltage cell placer/floorplaner. Figure 2 demonstrates the design methodology.
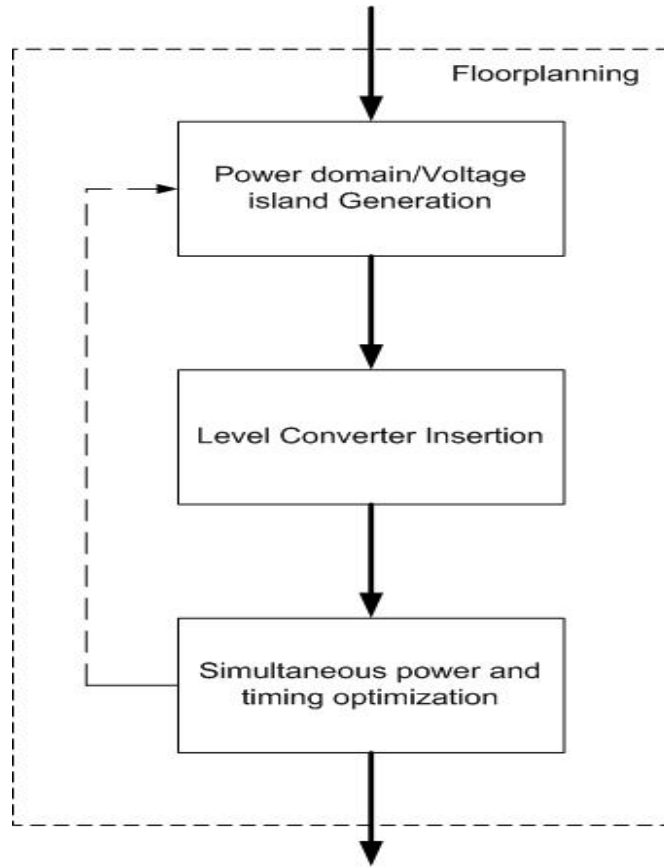
Figure 2. Floorplanning with aggressive power optimization methodology

Our plan is to optimally generate power domains-like placement instead of using generic power domains/voltage islands. Generic method is convenient in routing wires and minimizing area; but it's not good enough to minimize the power consumption. So we introduce an automatic-update force-balanced placer that can save more power than generic method. However the whole job is too large to be finished within one year. So we set our objective to designing a post-placement optimization to refine the placement from some well-known placers which supports single-supply-voltage designs.

We can place the target standard cells by some well-known efficient placers, such as Capo [7], Kraftwerk [8], or Dragon [9]. These placers are known for their run-time efficiency and good quality of achieving minimum total half-perimeter wirelength [10]. Obviously, shorter wire length results in less power consumption, so the power consumption may be kept low. Then we further flip the supply voltage of some cells to lower their Vdds while a given timing constraint is still satisfied.

三、研究方法及成果 (Method and Result)

1. Problem Formulation and Proposed Method

Our post-placement optimization is designed as follows. At first we set all cells to be operated on high supply voltage. Then we flip as more cells as possible to be fed with low supply voltage, while minimizing the total number of level converters inserted [6]. However the timing constraint must be satisfied. We use a method similar to Fiduccia-Mattheyses algorithm in partitioning (a well-know partition algorithm, invented by Fiduccia and Mattheyses). At first, we place the standard cells by some well-known high quality placer (eg. Kraftwerk, Capo, or Dragon). Secondly, we identify the paths, nets, and the corresponding timing. Then we iteratively select some cells and flip their supply voltages until no more improvement can be made.

This is our main algorithm for our approach:
- Initial partition: |L|=0, |H|= All
- Perform the initial timing analysis on each path
- Evaluate the score of each cell (calculate the reduction in power if their supply voltage are altered, considering the level converters simultaneously)
- DO
  - Alter the supply voltage of the winner cell (highest score)
  - Insert/remove level converters if necessary
  - Update the timing
  - If there's timing violation, give a certain penalty
- WHILE there is improvement or timing violation

We also need to consider the level converter insertion since, for a given cell placement, there may be no white space reserved for the converters to be inserted. The insertion of level converters may affect the local placement. A simple heuristic is to attach level converter to the corresponding cell which needs it. We have two candidates to solve this problem. We can update the placement in each iteration by shifting the relevant cells one by one toward a given direction to the boundary. It is relatively precise but time-consuming and it may causes oscillations. The other one is to forget the cell area of

all the converters during iterations. After all iterations are finished, we post-process the insertion of level converters and refine the circuit to meet the timing constraint with minimum power increasing.

2. Result

We give a simple example to show the method we used.
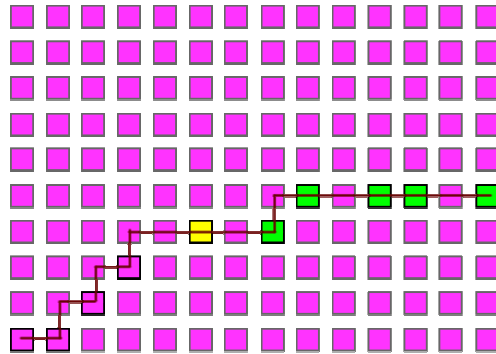
Starting phase of a path

A cell on the most slacked path P*i* (which has the most timing budget among all the paths) has the highest score, so it is chosen and its supply voltages is flipped to Vdd*low*
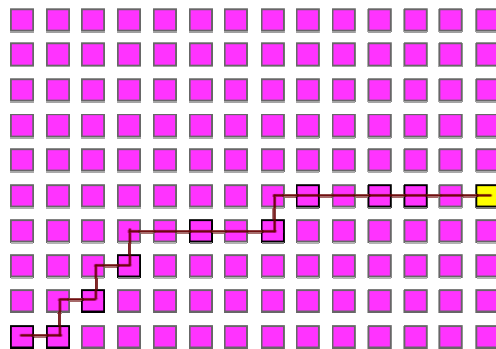

Growing phase of a path

Cells adjacent to the previous highest-scored one along P*i* may be chosen because it introduces no extra level converters. Similarly, more and more cells on Pi are selected and their supply voltages are flipped to Vdd*low*, while the timing budget on Pi is gradually decreased.
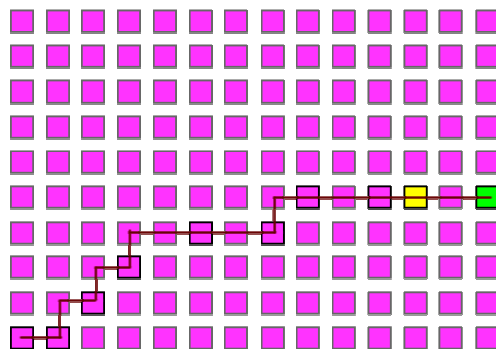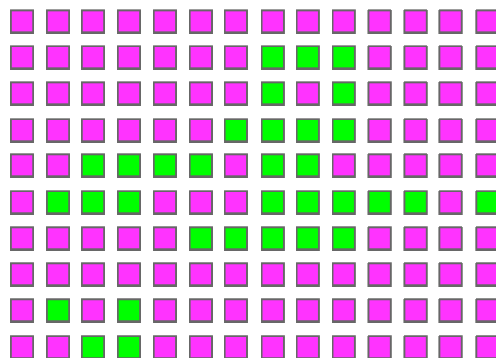
Retiring phase of a path

P*i* is no more competitive with another path, and the Vdd*low* power domain along P*i* stops to grow. Another winner path P*j* start to enter its life cycle. Continue this process until no more power reduction is available or no more timing budget remains.
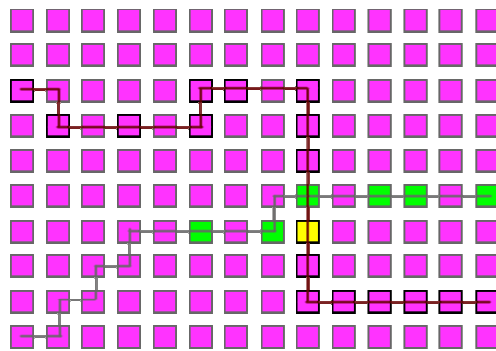
Final result

四、結論與討論(Conclusion and Discussion)

In this report, we described a new method to lower the power dissipation by using dual voltage supply during post placement period .Based on some preliminary results, our method can reduce about 15% of the power dissipation or more. We will obtain more experimental results and submit our work to leading conferences for publication.

五、研究方向(Future Work)

In the future, we plan to design a force-balanced/force-directed algorithm for power-driven/timing-aware floorplanning/placement which supports multiple supply voltage. Force-balanced/force-directed gives good guidance on the distribution of the cells geometrically with minimal total cost increase. However, its complexity directly proportion to the exponential function of the circuit size. We plan to formulate this problem as a convex quadratic programming problem. The proposed algorithm is as follows.

Force-balanced algorithm depiction:

• Initial expansion

A. Perform the initial cell-shifting by putting the cells along most critical signal path on the shortest geometrical path from input pin to output pin, within the placing region

B. Suppose that the placing region is a pre-determined

• Solve CQP

A. Cost function: $\sum wx(xi-xj)2+wy(yi-yj)2$ (attracting forces)

B. Repulsive forces: overlapping

• Decide the weighting parameter

A. Wx and Wy are non-negative weighting coefficients to set the amount of distance to displace and we can use those coefficients to control the desired cost function

B. Strongly connected cells (on critical nets) are applied with larger Wx and Wy, and lose nets are applied with small Wx and Wy

• Cell shifting

    A. Cells should be shifted to reduce the overlapping

    B. According to our objectives (timing, power, congestion), choose a certain cells to be shifted apart step by step

• Placement scope

    A. Two phases of placing: coarse (global) and detailed (local)

    B. This algorithm needs strong repulsive force to totally remove all the cell overlapping

五、參考文獻(References)

[1] C. Chen. "Physical Design with Multiple On-Chip Voltages," ACM ISPD, p. 118, 2002

[2] R.X. Nijssen and E.P. Huijbregts. "A Complete Design for Power Methodology and Flow for Large ASICs," ACM ISPD, pp. 106-108, 2003

[3] David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn, "Managing Power and Performance for System-on-Chip Designs using Voltage Islands" IEEE/ACM ICCAD, pp.195-202, 2002

[4] Yuvraj Singh Dhillon, Abdulkadir Utku Diril, Abhijit Chatterjee, and Hsien-Hsin Sean Lee, "Algorithm for Achieving Minimum Energy Consumption in CMOS Circuits Using Multiple Supply and Threshold Voltages at the Module Level" IEEE/ACM ICCAD, pp.693-700, 2003

[5] Ruchir Puri, Leon Stok, John Cohn, David Kung, David Pan, Dennis Sylvester, Ashish Srivastava, Sarvesh Kuldarni, "Pushing ASIC performance in a power envelope", ACM/IEEE DAC, pp.788-793, 2003

[6] Mutsunori Igarashi, Kimiyoshi Usami, Kazutaka Nogami, Fumihiro Minami, Yukio Kawasaki, Takahiro Aoki, Midori Takano, Chiharu Mizuno, Takashi Ishikawa, Masahiro Kanazawa , Shinji Sonoda, Makoto Ichida and Naoyuki Hatanaka, "A Low-power Design Method Using Multiple Supply Voltages", ACM/IEEE ISLPED, pp.36-41, 1997

[7] Andrew E. Caldwell, Andrew B. Kahng and Igor L. Markov,"Can recursive bisection alone produce routable placements?", ACM/IEEE DAC, pp.477-482, 2000

[8] Hans Eisenmann and Frank M. Johannes, "Generic global placement and floorplanning", ACM/IEEE DAC, pp.269-274, 1998

[9] Maogang Wang Xiaojian Yang Majid Sarrafzadeh, "Dragon2000: standard-cell placement tool for large industry circuits", IEEE/ACM ICCAD, pp. 260-263, 2000

[10] Saurabh N. Adya, Mehmet C. Yildiz, Igor L. Markov, Paul G. Villarrubia, Phiroze N. Parakh, and Patrick H. Madden, "Benchmarking for large-scale placement and beyond", IEEE TCAD, v.23, pp.472-487, April 2004