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子計畫五：低電壓差動信號傳輸接收器之設計與量測(2/3)

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執行單位：國立交通大學電子工程學系

計畫主持人：吳錦川

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1. Introduction

The primary components of a data link are the transmitter, receiver, and cable [1]. In the first year of this research project had designed a CMOS serial link transmitter and receiver at a data rate of 480 Mb/s using LVDS (low voltage differential signal). In the second year, we had tried to increase the data rate to 1~1.2 Gb/s using TSMC 0.35um 2P4M process with 3.3V supply. Three transmitters were designed, fabricated and measured. Three receivers were designed; two were fabricated and measured.

2. Transmitter

With a broadband signal used in digital systems, the Inter symbol Interference (ISI) always exists. This effect is most pronounced in the case of a single 1 (0) in a field of 0s (1s). A transmitter with pre-emphasis can eliminate the frequency dependent attenuation by detecting the magnitude of transmitted signal to give a flat frequency response. Figure 1 shows a transmitter with pre-emphasis. It is consisted of a PLL, an 8 to 1 data multiplexer, an 8 to 1 emphasis multiplexer and an emphasis data driver.

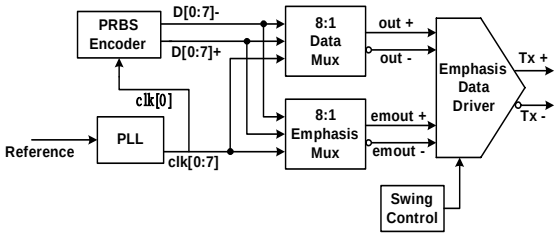

Fig. 1 Pre-emphasis transmitter block diagram

With a 31.25 MHz reference frequency, the PLL can form a 125MHz output with eight uniformly distributed phases as clock signals for the multiplexer. Therefore we can achieve bit rates of 1 Gb/s. The multiplexer consists of two stages: a differential input multiplexer and a source coupled pre-driver as Fig. 2 [2]. The speed of the multiplexer circuit is mainly determined by the resistance of PMOS and the total capacitance of the output node. Increasing the PMOS size relative to the NMOS size would increase the speed while reducing the swing of the output nodes A and B. The ratio of the PMOS and NMOS sizes has to be chosen such that the swing at the multiplexer outputs A and B are enough to switch the pre-driver in the worst case. The schematic of the pr-emphasis multiplexer is identical to Fig. 2 except it is delayed by one bit period 1ns [3].

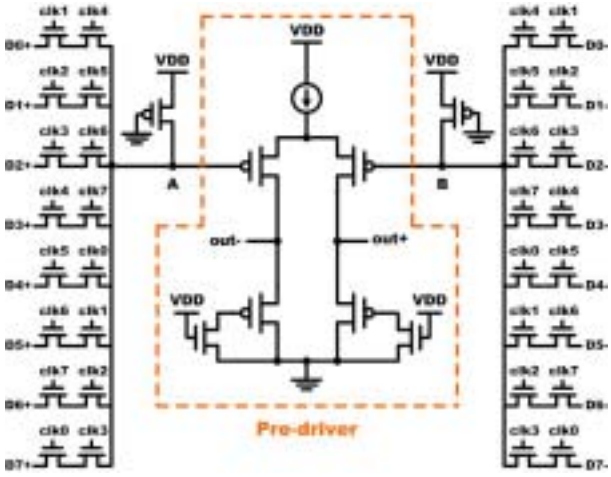

Fig. 2 Schematic of data multiplexer.

The pre-driver is composed of a source coupled pair with active inductive peaking load. The active inductive peaking load can substantially enhance the bandwidth of gain stages [4]. The implementation of the active inductor is shown in Fig. 2, which consists of a PMOS device and a

resistor Rs placed in series with the gate of PMOS.

The data driver, as shown in Fig. 3a, is an open-drain current-mode driver, which is composed of a differential source coupled pair with a stable constant current source Id. The main issue of the data driver is the settling time control, that is, the bandwidth limitation of the driver. When the bit time of the data is smaller than the settling time of the data driver, the values of the previously transmitted signal will affect the current bit's waveform. This interference is called inter-symbol interference (ISI). As shown in Fig. 3b, a pre-emphasis driver is applied directly on the output pins to enhance the settling ability of the data driver.

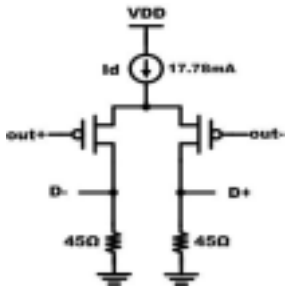

Fig. 3a. Transmitter data driver.

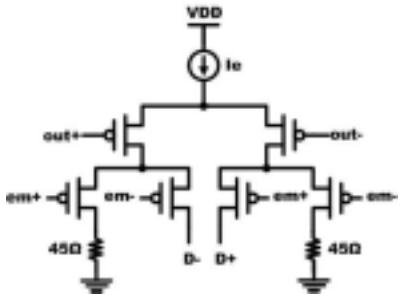

Fig. 3b. Pre-emphasis data driver.

The data driver in Fig. 3 is pseudo-differential, i.e., its logic low level is at 0V. A truly differential data driver is also designed, as shown in Fig. 4. The driver uses the typical configuration with four MOS switches in the bridge configuration [5], M1- M4: with M1 and M4 switched on, the polarity of the output current is positive together with differential output voltage, |Vout+ -Vout-|. On the contrary, if M1 and M4 are switched off, the polarity of the output current and voltage is reversed. In Fig. 4, the right half circuit is the common mode feedback control to achieve higher precise output that fall within the LVDS standard specifications.

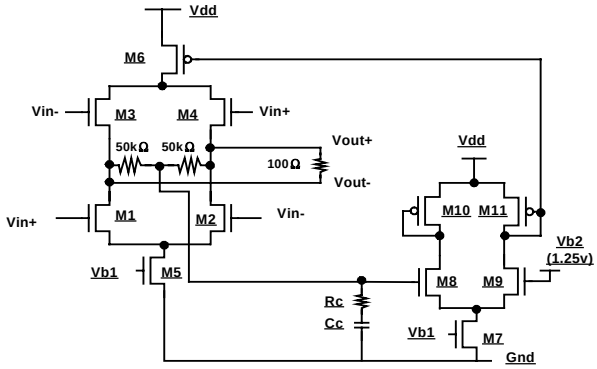

Fig. 4. Data driver with common mode feedback.

3. Receiver

Generally speaking, there are two ways which can be adopted to recover the system clock, including oversampling and tracking schemes. Oversampling receivers in this report uses 3 samples per bit. Each sample is compared with neighboring samples to indicate whether a data transition occurs or not. With this information, the bit value and boundary can be determined. Oversampling receiver has several advantages compared to the tracking receiver. First, it is simpler to implement since there is no need for summing networks and phase interpolators. Second, it could reject high frequency jitter because it determines the bit value by comparing it directly with its nearest neighbor [6]. However, this receiver requires a faster sampling rate and the chip area occupied by the decision logic block is significant. Besides, the quantization jitter (which is the uncertainty in the position of each detected transition) is also introduced by the oversampling receiver.

Figure 5 shows the block diagram of the tracking data recovery receiver. It consists of demultiplexing samplers, shift registers, a control logic circuit, a synchronizer, a phase shifter, phase selectors, a PLL and two interface circuits.

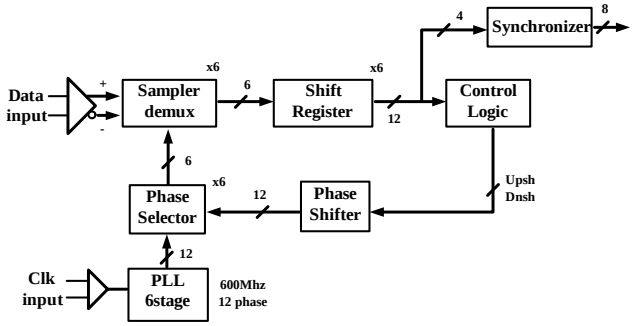

Fig. 5. Block diagram of 2-bit oversampling receiver.

In order to recover 1.2 Gb/s data input, the PLL output is 600 MHz with 12 phases outputs, i.e., equivalent to 7.2 GHz resolution. Six phase selectors are used to select 6 phases out of the 12-phase clocks. The Sampler produces 6 samples at 600 MHz rate, i.e, 2 data bits were sampled each time. Another oversampling receiver is shown in Fig. 6. It only samples 1 bit at 600 MHz rate. Therefore, its PLL is working at 1.2 GHz, but only has 6 phase outputs. Only 3 phase selctors are needed. Both circuits are operating at equivalent frequency of 7.2 GHz, but the die size of the circuit in Fig. 6 is smaller.

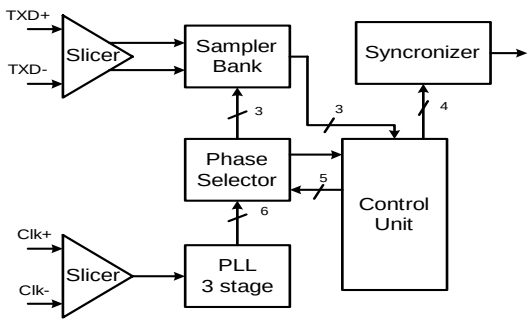

Fig. 6. Block diagram of 1-bit oversampling receiver.

Another receiver is shown in Fig. 7. It uses half-rate clock and data recovery circuit. With input data at 1 Gb/s, the half-rate CDR is operating at 500 MHz.

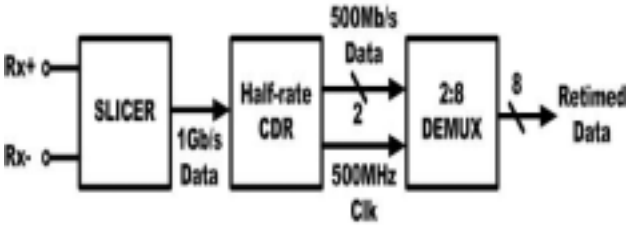

Fig. 7. Block diagram of the half-rate receiver.

4. Experimental Result

The transmitter is implemented in tsmc 0.35um 1P4M CMOS process. Fig 8 is the chip photo of transmitter.

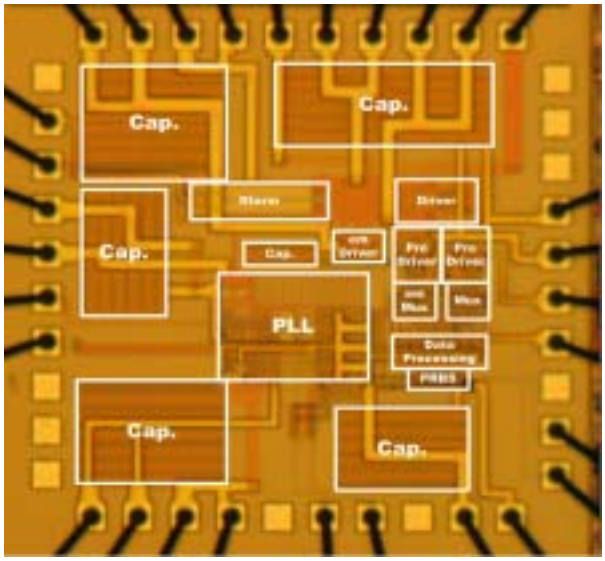

Fig. 8. Chip photo of the Transmitter.

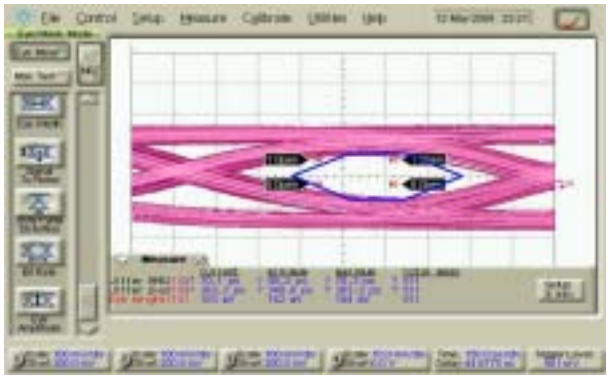

Fig. 9. Waveform without pre-emphasis (5.4m cable)

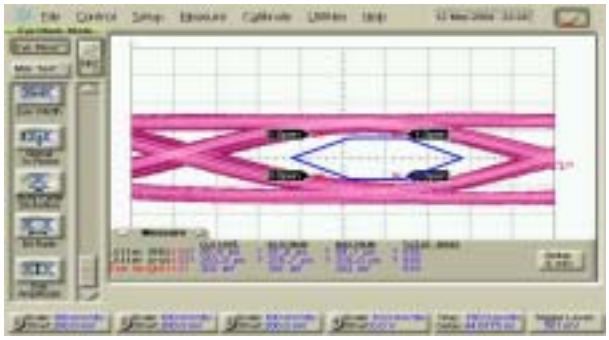

Fig. 10. Waveform with pre-emphasis (5.4m cable)

Fig. 9 and Fig. 10 are observed through 5.4m cable without and with pre-emphasis, at 1 Gb/s data rate. The eye size observed with pre-emphasis is much bigger. For the LVDS transmitter, the measured waveform of the data driver alone is shown in Fig. 11.

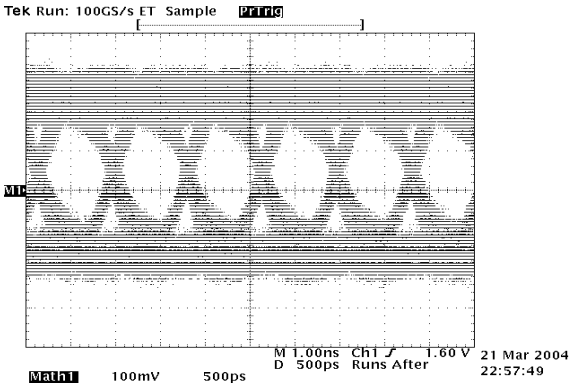

Fig. 11. Waveform of the LVDS data driver.

The data rate is 1.2 Gb/s. Its eye size is greater than 200mV. The waveform of the entire transmitter is shown in Fig. 12. There is no eye at all.

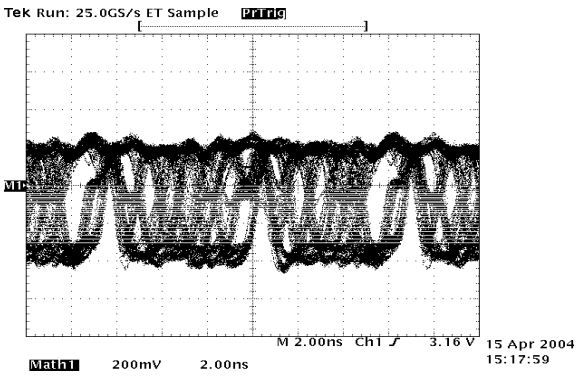

Fig. 12. Waveform of the LVDS transmitter.

5. Conclusion

Two kinds of LVDS transmitter circuit with pre-emphasis has been designed and fabricated in 0.35um 2p4M CMOS process. The pseudo differential transmitter is verified to perform at 1.2 Gb/s with 3.3V supply. The true differential data driver also worked at 1.2 Gb/s, but the transmitter has serious jitter. It may be from the PLL and the MUX circuit. The two oversampling receivers were fabricated. The bit error rate of the 2-bit over-sampling receiver is quite high. The 1-bit over-sampling receiver's PLL does not work properly. A new round the receiver will be design in next year.

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