Capacitance Characteristics Improvement and Power Enhancement for RF LDMOS Transistors Using Annular Layout Structure

Chia-Sung Chiu, *Member, IEEE*, Kun-Ming Chen, *Member, IEEE*, Guo-Wei Huang, *Member, IEEE*, Ming-I. Chen, Yu-Chi Yang, and Kai-Li Wang

***Abstract*—This paper presents an annular-structure lateral-diffused metal–oxide–semiconductor (LDMOS) RF transistor using a 0.5-μm LDMOS process. This paper also examines the dc, small-signal, and large-signal characteristics of RF LDMOS transistors with different closed structures. In particular, the problem of evaluating the LDMOS aspect ratio for annular structure is addressed. The capacitance characteristics improvement in the LDMOS device design using the annular structure was also investigated. The power gain and efficiency of annular structure give nearly 5% enhancement compared to the traditional structure with 80-μm gatewidth at 1.9 GHz. Results show that the annular structure appears to be a better layout design for RF LDMOS transistors.**

***Index Terms*—Annular structure, lateral-diffused metal–oxide–semiconductor (LDMOS) transistor, power, power-added efficiency (PAE), X-parameters.**

I. Introduction

SILICON lateral-diffused metal–oxide–semiconductor (LDMOS) transistors have been of great interest due to their applications in RF amplifiers in wireless communication systems or base-stations [1]. LDMOS transistors provide several advantages, including high efficiency, low cost, and good linearity capability on silicon substrates. Scaling down the gate length or the drift length of LDMOS transistors improves their performance by producing lower on-resistance and higher transconductance. However, these scaling approaches may limit high-voltage endurance during power-amplifying operations.

In addition to scaling down the device or changing device processes, researchers have studied several transistor layout styles in their search for the best device performance [2]. These designs must deal with the tradeoff between layout area and reduced parasitic. The results presented in this study show that closed transistors offer many promising characteristics. The most widely used closed topology is the square-structure transistor. However, square-structure corners contribute very little to the current drive, but significantly increase the gate input capacitance [3]. If the applied voltage is high with respect to the channel length, the electric field in the corners could break the device. In this case, a circle-type layout, called an annular structure in this paper, would be the optimum layout type for ensuring the most uniform current flow. However, some works are only published in a square shape or polygonal shape due to foundry process restrictions [4], [5]. Besides, this study also performs the capacitance analysis. Due to the capacitance influence of the input and output of enclosed devices, which are significant in dynamic operation and have an impact on device high-frequency performance, many studies have been published on the capacitance characterization and modeling of LDMOS transistors [6]–[8]. In this study, for the first time, the power performance and linearity are also compared between the annular structure and square structure.

This paper analyzes a dc, small-signal, and power performance for a 1.9-GHz annular-structure LDMOS. Section II describes the layout design and fabrication. Section III estimates the effective width and capacitance performance for annular- and square-structure transistors. Section IV describes the power performance and characteristics of an RF LDMOS, as well as the nonlinear characteristics using X-parameters. Finally, conclusions are given in Section V.

II. Device Design and Fabrication

In this study, the annular-structure RF LDMOS transistors were fabricated using a 0.5-μm LDMOS process. The standard LDMOS layout consists of a source and a drain separated by a channel of width W and length L. An annular-structure LDMOS consists of a transistor with the source diffusion in the middle, encircled by the gate channel and the drain diffusion to achieve a lower ON-resistance [9]. The channel width for annular structure is the length of the curve lying at midchannel.

Fig. 1 shows a die photograph. This photograph depicts the annular-structure RF LDMOS with total 400-μm width length (ten cells and 40 μm per cell). The cell layouts of an annular-structure and square-structure LDMOS transistor were shown in Fig. 2. Fig. 3 illustrates the schematic cross section of this device. The drain region was extended under the field oxide (FOX), consisting of a lightly doped N-well drift region and an N region with higher doses for on-resistance control. This

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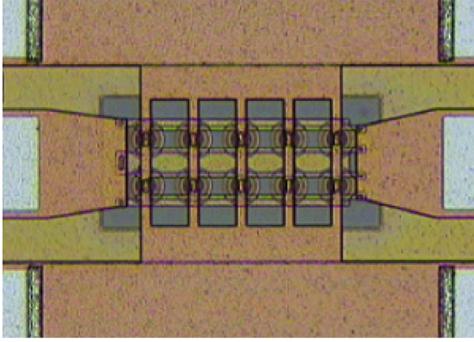


Fig. 1. Annular-structure RF LDMOS with total 400-μm width length (ten cells and 40 μm per cell).

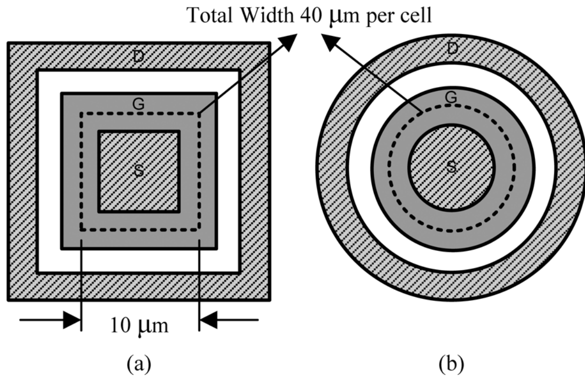


Fig. 2. Layout structure of a LDMOS transistor cell. (a) Square structure. (b) Annular structure.

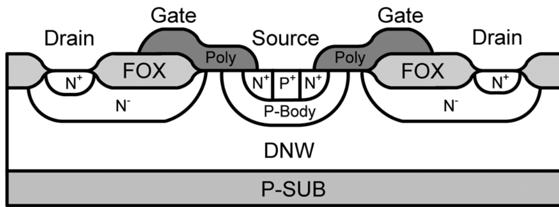


Fig. 3. Schematic cross section of the LDMOS transistor.

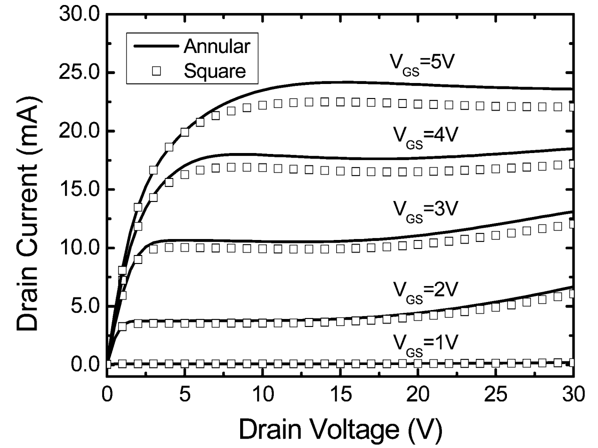
design ties the source region and the p-body together to eliminate extra surface bond wires, reduce the source inductance, and improve the RF performance in a power amplifier [10]. This study optimizes the LDMOS transistor layout for high-frequency performance with a ground–signal–ground (GSG) structure adapted for on-wafer measurement.

III. DC and Capacitance Performance

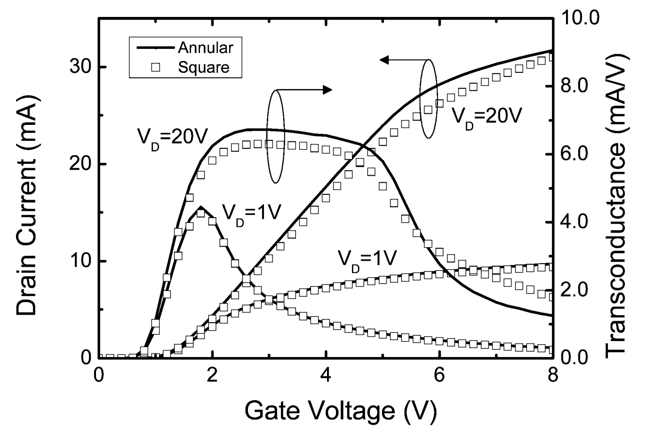
A. Effective Width

The initial problem in an annular-structure LDMOS is the definition of the aspect ratio W/L, which is not as complicated as in standard devices. However, defining the width (W) of the annular structure is less straightforward. For example, the width (W) can either be the length of the curve lying at midchannel or the drain/source diffusion perimeter.

This study extracts the experimental W/L values by comparing the $I_D - V_{\rm GS}$ characteristics of an annular-structure transistor and a standard transistor with the same L. The SPICE



(a)



(b)

Fig. 4. (a) Output and (b) subthreshold characteristics of LDMOS transistors for different layout structures.

model can be used to extract W/L from the ratio of transconductances g_m as follows [11]:

$$g_m = \frac{\partial I_D}{\partial V_{\rm GS}} = \left(\frac{W}{L}\right)_{\rm eff} \mu C_{\rm ox} V_{\rm DS}(1+\lambda V_{\rm DS}) \quad (1)$$

$$\left(\frac{W}{L}\right)_{\rm eff}^{\rm closed} = \left(\frac{W}{L}\right)_{\rm eff}^{\rm std} \frac{g_m^{\rm closed}}{g_m^{\rm std}} \quad (2)$$

where superscripts std and closed refer to the square structure and annular structure, respectively. As the effective aspect ratio of the square structure was known, the aspect ratio of the annular structure can be determined.

Fig. 4 shows the *I–V* characteristics of an LDMOS under static conditions. The actual schematic layout of the annular-structure LDMOS transistor was shown in Fig. 5. The dc characterization of the device-under-test (DUT) was performed using an Agilent semiconductor parameter (4156C) analyzer. In the saturation region, the annular structure shows a higher drain current and transconductance than the square structure. These are attributable to the larger equivalent W/L and smaller drain parasitic resistance. The effective annular-structure width is 83.2 μm compared with the square structure (two cells, the total $W = 80$ μm). These results show that the annular structure has better dc performance than the square structure.

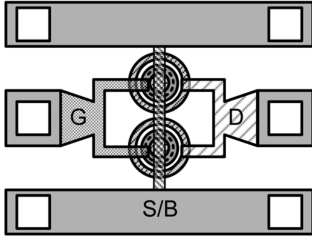


Fig. 5. Simplified layout for test structure of annular-structure LDMOS transistor with 80-μm channel width (two cells).

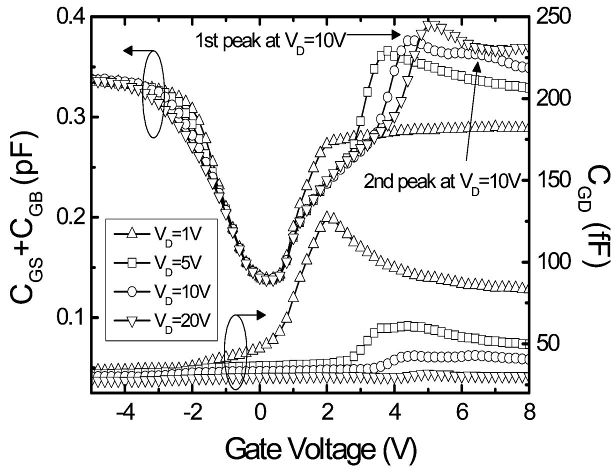


Fig. 6. Extracted $C_{\rm GS} + C_{\rm GB}$ and $C_{\rm GD}$ versus gate voltage with different drain biases for square-structure LDMOS transistor.

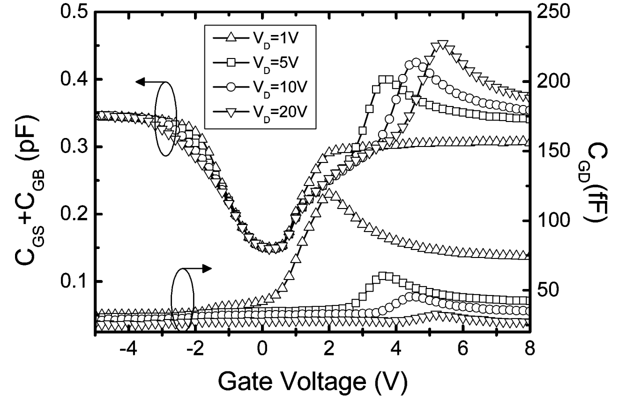


Fig. 7. Extracted $C_{\rm GS} + C_{\rm GB}$ and $C_{\rm GD}$ versus gate voltage with different drain biases for annular-structure LDMOS transistor.

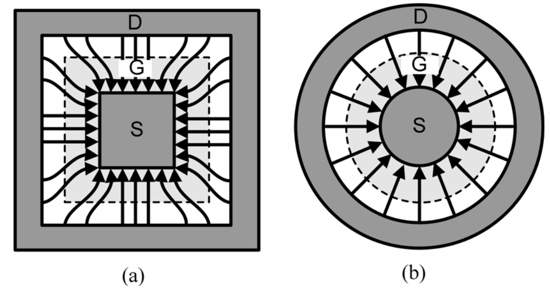


Fig. 8. Schematic view of layout structure and current distribution in RF LDMOS. (a) Square structure. (b) Annular structure.

B. Capacitance Characteristics

This section extracts the gate-to-source/body capacitance $(C_{\rm GS} + C_{\rm GB})$ and gate-to-drain $(C_{\rm GD})$ capacitance from the de-embedded S-parameters in the low-frequency range [12], [13]. Figs. 6 and 7 show the extracted $C_{\rm GS} + C_{\rm GB}$ and $C_{\rm GD}$ of RF square-structure and annular-structure LDMOS transistors at room temperature. At $V_{\rm DS} = 1$ V, both square and annular structures have similar curve traces because they share the same physical mechanism. In terms of the lateral nonuniform doped channel in the LDMOS, the drain end will be inverted prior to the source end, resulting in a peak in $C_{\rm GD}$. As the drain voltage $V_{\rm DS}$ exceeds 5 V, $C_{\rm GS} + C_{\rm GB}$ and $C_{\rm GD}$ all start to reveal distinct peaks. This is because the inversion charges are injected to the depleted area of the drift. Therefore, $C_{\rm GD}$ and $C_{\rm GS} + C_{\rm GB}$ increase with increasing V_G, and $C_{\rm GS} + C_{\rm GB}$ increases suddenly over the flat of the inversion area to reach the maximum at the onset of quasi-saturation [14]. The reason for this phenomenon is that a higher V_D leads to a higher V_G at the onset of quasi-saturation, and thus the peaks shift to a higher V_G. Besides, the capacitance improvement is approximately 3% in the accumulation region at $V_G = -5$ V and $V_{\rm DS} = 1$ V, which was resulted from current drive of the annular structure.

However, for the square structure, Fig. 6 shows a second peak in $C_{\rm GS} + C_{\rm GB}$ and $C_{\rm GD}$ at $V_{\rm DS} = 10$ V. This abnormal peak generated from the square structure will be hard to be predicted and increase modeling complexity. Fig. 8 shows a uniform current distribution across the region from drain to source in annular structures. From this figure, it is a reason that the uniform current distribution results in the second peak appeared in square structure. Since the corners of the drift of the square structure show a lower current density than the edges, the square-structure device must provide higher gate voltage to go into quasi-saturation. In other words, besides the first peak results from the edges of the square structure, which went into the quasi-saturation region in advance, the second peak appears when the corners start to go into quasi-saturation at V_G is 6.5 V when $V_{\rm DS} = 10$ V.

IV. Small-Signal and Power Performance

A. Small-Signal Performance

To characterize the high-frequency performance and determine the maximum cutoff frequency (f_T) and maximum oscillation frequency $(f_{\max})$ of the annular-structure LDMOS transistor, this study measures S-parameters on wafer from 0.1 to 20 GHz using an Agilent performance network analyzer (E8361C). In these measurements, parasitics pad capacitances were de-embedded using an OPEN dummy pad structure. Fig. 9 shows the high-frequency characteristics of an LDMOS with an annular structure analyzed from S-parameters at different gate bias. The cutoff frequency and maximum oscillation frequency are the frequency where the current gain was 0 dB and the frequency where the MSG was 0 dB, respectively. At $V_G = 2.5$ V

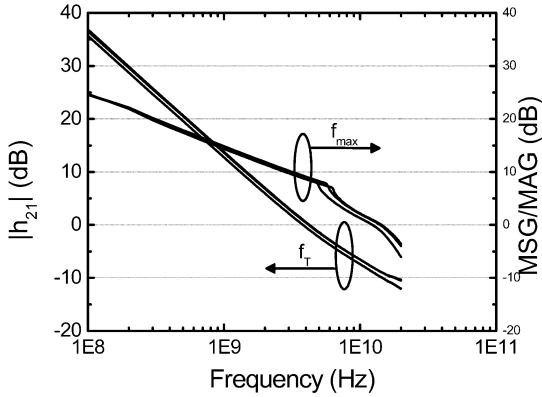


Fig. 9. Dependence of $|h_{21}|$ and MSG/MAG on frequency obtained from S-parameter measurements ($Vd = 20$ V and $Vg = 1.5, 2.5,$ and 3.5 V).

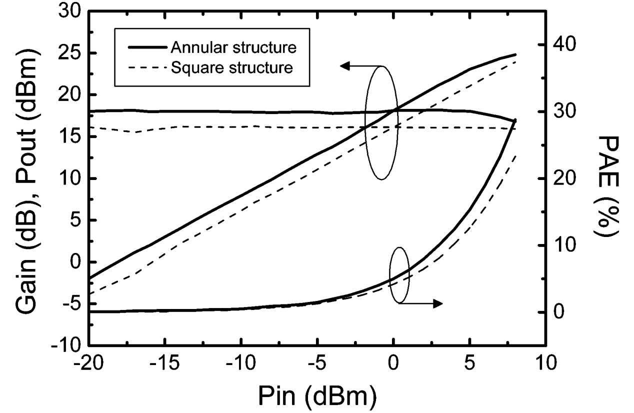


Fig. 11. Output power and efficiency versus input power at 1.9 GHz, $V_D = 20$ V, and $V_G = 2.5$ V with different layout structure ($W = 400\ \mu$m).

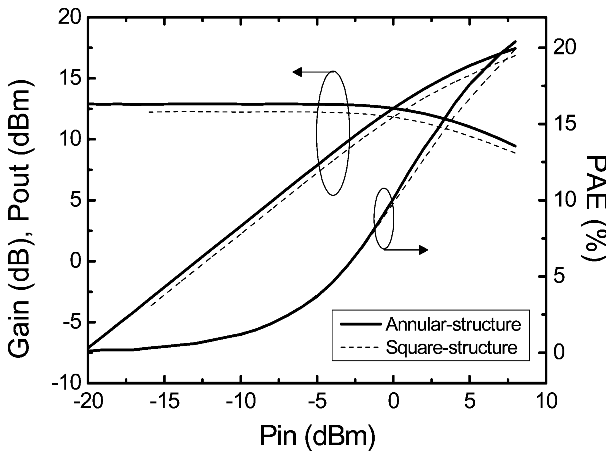


Fig. 10. Output power and efficiency versus input power at 1.9 GHz, $V_D = 20$ V, and $V_G = 2.5$ V with different layout structure ($W = 80\ \mu$m).

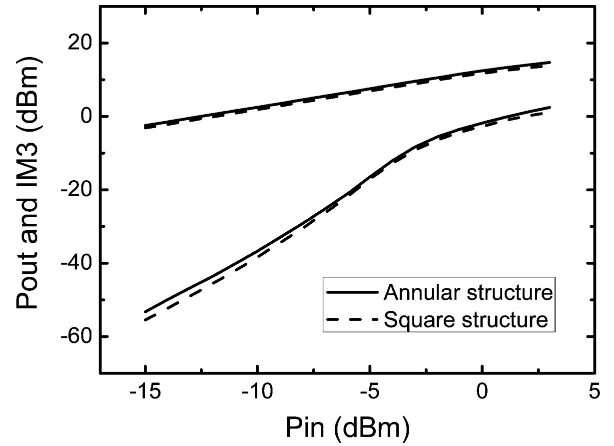


Fig. 12. Output power and IM3 power versus input power with different layout structure ($W = 80\ \mu$m).

and $V_D = 20$ V, the cutoff frequency and maximum oscillation frequency are approximately 5 and 12 GHz, respectively.

B. Large-Signal Performance and Characterization

This study measured power performance using a load–pull system consisting of HP85122A and ATN LP1 at the cascade probe station with the probe calibrated using a standard calibration substrate. Input and output impedance matching conditions were selected to yield optimum power gain and power-added efficiency (PAE). Fig. 10 shows the transducer power gain and efficiency of different layout structures, taken at $W = 80\ \mu$m. In the case of the load–pull measurement, the operating frequency was 1.9 GHz and the source and load impedances were biased at $V_D = 20$ V and $V_G = 2.5$ V, which are maximum cutoff frequency values. Fig. 10 indicates a power gain of over 12 dB and an input power 7 dBm at the 1-dB compression point. The PAE at this point is over 20%. Fig. 10 also shows that the annular structure had higher power gain and efficiency than the square structure. The gain and PAE of the annular structure is higher than the square structure by almost 5%. This result might be attributed to the larger equivalent transconductance of the annular structure. The transducer power gain and efficiency of different layout structures with 400-μm gatewidth are shown in Fig. 11. The improvement of gain and PAE are around 11% and 23%, respectively. The linearity of RF LDMOS device is also analyzed in this study. The comparison between the annular structure and square structure is shown in Fig. 12. In this figure, third-order intermodulation intercept point (IIP3) and output third-order intercept point (OIP3) of the annular structure are similar to the linearity performance of square structure. This results show that the variety of LDMOS layouts has a much smaller influence on linearity performances.

This study used an Agilent nonlinear vector network analyzer capable of nonlinear calibration and measurements to extract the nonlinear model formed by X-parameters as simulation results [15], [16]. This system also includes high-gamma tuners and an interface for other instruments to automatically control X-parameters characterization and extraction. Fig. 13 shows that the X-parameters accurately predict the measured transducer power gain and the third-order intermodulation (IM3) with the load impedance far from 50 Ω. Using a standard nonlinear analysis tool in Agilent Design System (ADS), the measured DUT X-parameters can be immediately used to simulate nonlinear figures of merit such as gain $P_{1\ \mathrm{dB}}$, IP_3 and other nonlinear performance [17]. The simulation results

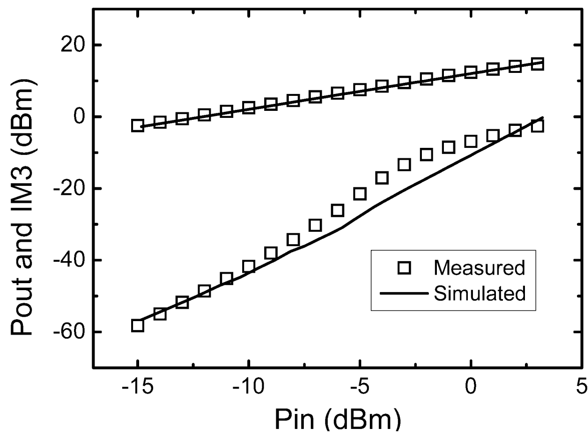


Fig. 13. Measured and simulated results of the intermodulation distortion for 1.9 GHz with a tone spacing of 1 MHz and $V_D = 20$ V, and $V_G = 2.5$ V. The total width length of the annular-structure LDMOS transistors is 80 μm.

agree well with the nonlinear behavior of the annular-structure LDMOS transistor with 80-μm width length at 1.9 GHz.

V. Conclusion

Two types of layout structures of RF LDMOS transistors for dc, capacitance, and power characteristics were investigated. The annular-structure LDMOS transistor had a better performance than the square structure without changing the process flow. The higher drain current and g_m in the annular-structure LDMOS was due to less corner effect compared with the square structure. Besides, by using the annular structure, it is possible to improve the capacitance characteristics of the RF LDMOS transistor. Due to the larger equivalent transconductance of the annular structure, the power gain and PAE of the annular structure is higher than the square structure by at least 5%. Moreover, this study also shows linearity performance of the RF LDMOS transistor does not degrade with the variety of LDMOS transistor layouts. The nonlinear behavior of annular-structure LDMOS transistors using X-parameters also presented in this study. The linearity can be predicted using this model without any optimization and curve fitting. According to the capacitance extraction results and power performances, the annular structure is superior to the square structure in the layout type of the LDMOS transistor.

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