Generalized Hot-Carrier Degradation and Its Mechanism in Poly-Si TFTs Under DC/AC Operations

Ya-Hsiang Tai, Shih-Che Huang, Po-Ting Chen, and Chih-Jung Lin

***Abstract*—In the previous report, we had reported the mechanism for the degradation of poly-Si TFTs under OFF region gate ac operation with the source and drain electrodes grounded. In this paper, the study is extended to the degradation of the devices under various ac and dc operation conditions. It is discovered that, though these stress conditions are different, the corresponding degradation behaviors in their I–V and C–V curves all resemble the degradation behavior of the device under dc hot-carrier stress. Two important factors, namely, the electric field across the junction and the number of carriers flowing through the junction, are taken into discussion in this paper and comparison of these stress conditions. It is then categorized that these operation conditions can be described as the "generalized hot-carrier effect," since the degradation is found to occur near the junctions by the energized carriers, just as that under dc hot-carrier stress. The qualitative comparison of the electric field and carrier flow through the junction for the four stress conditions as well as the difference in the degradation mechanism between MOSFETs and poly-Si TFTs are also provided.**

***Index Terms*—AC stress, dynamic stress, poly-Si TFTs, reliability.**

I. Introduction

Poly-Si TFTs, which have the similar structures as the MOSFETs, are now under extensive studies for the applications in display system. The high device mobility of these devices enables the possibility to form both the in-pixel switches and integrated circuits with the poly-Si technology, which may greatly reduce the process complexity and fabrication cost. [1] The high device mobility also enables some special value-added functions to be integrated into the display panel. [2], [3] Devices in such applications would be dynamically operated and the operation conditions could be very different from those in the pixel. Though recently, several kinds of products formed with poly-Si technology have hit the market, the degradation mechanisms of the devices under dynamic operation are still not so clear. Y. Uraoka previously reported that the degradation behavior of the devices under gate ac operation between its ON and OFF regions with source/drain grounded can be attributed to the swept carriers as the device is about to be turned off. [4], [5] In addition to the gate ac ON/OFF region toggling, the device could also be operated some time in the OFF region alone. However, there are few papers on such reliability behavior. We had reported the degradation behavior for the device operated in the OFF region with source/drain grounded and it had been experimentally proposed that the degraded behavior can be attributed to the source and drain junction degradation during stress. [6] Nevertheless, the detailed degradation mechanism about how the junction would degrade under such operation is still not clear. In this paper, the explicit degradation mechanism would be explored, starting with the comparison of the device behavior under gate ac OFF region operation and the dc hot-carrier stress. The carrier source and the electrical field distribution during stress would be discussed and other stress conditions would be performed and compared. The idea of the "generalized" degradation model for the various stress conditions would be provided. The four stress conditions are summarized in Table I and named as "condition #1" to "condition #4" in the following discussion in order to make the manuscript more legible.

TABLE I
STRESS CONDITIONS AND THE CORRESPONDING DENOTATIONS

	Stress Conditions	
Condition #1	Gate AC stress in the OFF region	V_G=0~ -20 V, 500kHz, V_S=V_D=0V
Condition #2	DC hot carrier effect	V_G=3V, V_S=0V, V_D=20V
Condition #3	DC OFF region drain-biased stress	V_G= -5V, V_S=0V, V_D=20V
Condition #4	Gate AC stress between ON/OFF region	V_G=15~ -15 V, 500kHz, V_S=V_D=0V

II. Experiments

Top-gate poly-Si TFTs with width/length of 20 μm/5 μm were fabricated using low-temperature process. First, the buffer oxide and a-Si:H films with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then placed

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in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was then applied. The laser scanned the a-Si:H film with beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 50-nm SiO_2 and 25-nm SiN_X were deposited with PECVD as the gate insulator. Next, the TFT gate was formed by metal sputtering and then defined by photolithography. The lightly doped drain (LDD) and the n^+ source/drain doping were formed by PH_3 implantation with dosage 2×10^{13} cm^{-2} and 2×10^{15} cm^{-2} of PH_3, respectively. The LDD implantation was self-aligned and the n^+ regions were defined using a separate mask. Then, the interlayer of SiN_X was deposited. Subsequently, dopants were activated via rapid thermal annealing while the poly-Si film was hydrogenated simultaneously. Finally, the contact hole formation and metallization were performed to complete the fabrication work. The typical value of the threshold voltage for the fresh devices is 1.63 V.

Rectangular pulses applied to the TFTs are generated with an Agilent 41501B pulse generator and the dc stress is performed by using an Agilent 4156A precision semiconductor parameter analyzer. The capacitance–voltage (C–V) curves were measured with an Agilent E4980A precision LCR Meter.

III. Result and Discussion

A. Gate AC Stress in the OFF Region

Fig. 1(a) shows the transfer characteristics of poly-Si TFTs before and after gate ac stress in the OFF region. The stress condition is that the ac signal toggling between 0 V and -20 V at 500 kHz with 50% duty cycle is applied to the gate electrode while the source and drain electrodes are grounded during stress. During stress, there should be no induced carriers formed and the degradation should be negligible since the device is kept in the OFFregion. However, it would be surprising to find that the device exhibits severe degradation after stress, particularly for the ON current and the transconductance. Fig. 1(b) gives the gate-to-drain capacitance–voltage (C–V) behavior C_{GD} for the device before and after 200-s gate ac stress. The C_{GD} behavior is measured with the source electrode floated. The stress condition is the same as Fig. 1(a). The normalized capacitance is the ratio of the measured capacitance to the gate insulator capacitance of the TFT. As for its C–V behavior, the effect of such stress is that for the low measuring frequency, the curve for the stressed device shows slight shift, but for the high measuring frequency, the curve for the stressed device shows both shift and distortion. In other words, the effect of such degradation on the device's C–V behavior is frequency-dependent. This behavior somehow indicates that the degradation can be attributed to the states generated during stress rather than the trap charges, since trap charges would not respond to different measuring frequencies or result in the dispersion behavior in the C–V curves [7]. Such degradation behavior would be worthy of discussion since for the similar device structure, namely, MOSFETs, there is no such degradation behavior reported.

The difference between MOSFETs and poly-Si TFTs one may first think of is the difference between their structures.

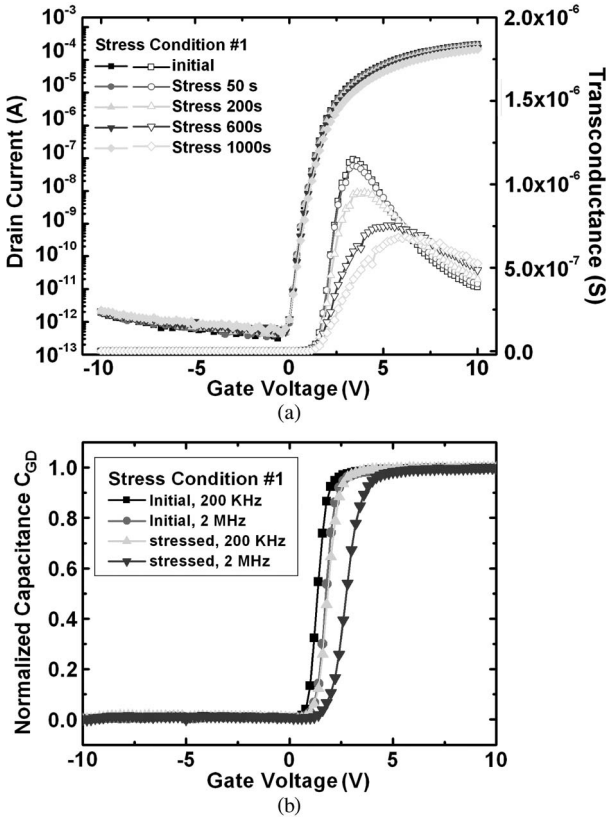


Fig. 1. (a) The current transfer behavior at $V_D = 5$ V and (b) the normalized gate-to-drain capacitance C_{GD} for the poly-Si TFT before and after 200-s gate ac stress in the OFF region.

There is a substrate electrode in MOSFETs and the carriers may be discharged through the substrate electrode during the OFF state toggling operation. The existence of the substrate electrode would also greatly affect the electric field near the substrate since in most operation conditions, it is grounded. As in the case of poly-Si TFTs, the lack of substrate electrode leaves the electric field near the substrate floated and also makes it rather difficult to analyze the behavior in the channel and substrate when the device is in the OFF region. One way to analyze the electric field distribution is by utilizing the TCAD simulation tools. However, the present programs available could only simulate the field distribution in dc operation, and thus it may not help to solve the degradation behavior under such ac operation.

Regarding such anomalous degradation behavior, we had proposed a device circuit model composed of the gate insulator capacitance, the channel resistance, and the source/drain junction to analyze what could happen during stress. By examining the voltage distribution across each element during stress, it was inferred that during the gate ac stress in the OFF region, the largely reverse-biased junction could lead to the degradation. The gated p-i-n device was then specially adopted to verify our inference. [6] However, in that report, we had not discussed how the largely reverse-biased junction could lead to the changes in the mobility and the C–V behavior for the stressed device. In the following discussion, several other stress conditions would be performed to help discover the explicit degradation mechanism. The first one to be discussed and compared is the

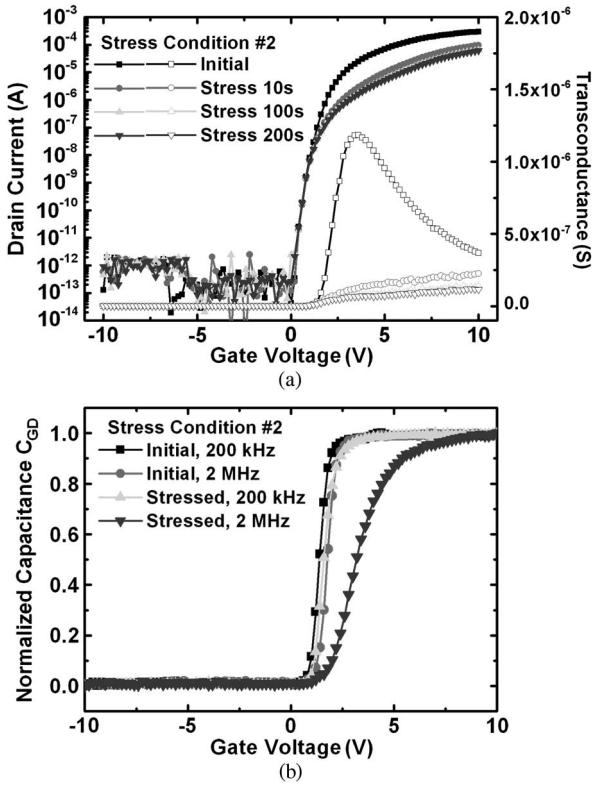


Fig. 2. (a) The current transfer behavior at $V_D = 5$ V and (b) the normalized gate-to-drain capacitance $\mathrm{C_{GD}}$ for the poly-Si TFT before and after 200-s dc hot-carrier stress.

hot-carrier effect. Its features on poly-Si TFTs are the obvious mobility and ON current degradation while the subthreshold region remains almost unchanged, which resembles the behavior in Fig. 1(a). It would be a good start since there are already reports on the behaviors of poly-Si TFTs under hot-carrier stress conditions. [8]

B. DC Hot-Carrier Effect

Hot-carrier effect, as many works have reported, is closely related to the distribution of the lateral electric field in the channel and therefore is in relation with the applied drain voltage V_{DS} and gate voltage V_{GS}. As referred to the studies of hot-carrier effect on MOSFETs, for the n-type devices, the high electric field near the drain region would accelerate the carriers and these carriers may attain enough energy to break the Si bonds as well as the $\mathrm{Si/SiO_2}$ interface, resulting in the increase of states. The increase in states would affect the conduction for the gate voltage larger than the threshold voltage V_{TH} and then degrade the device mobility [9]. For MOSFETs, when the large V_{DS} is applied, the degradation mechanism is different for different applied V_{GS}. Generally, the degradation is worst when V_{GS} is around $V_{\mathrm{DS}}/2$. [10], [11] Unlike in MOSFETs, hot-carrier effect in TFTs becomes most severe as V_{GS} is just above V_{TH} and V_{DS} is large [8]. Since the active region in the poly-Si TFTs contains many grain boundaries, the effect of hot-carrier stress may be more complicated than that in MOSFETs. Fig. 2(a) shows the current transfer characteristics for the poly-Si TFTs before and after hot-carrier stress. The stress condition is that the stress gate voltage V_{GS} is 3 V and the drain voltage V_{DS} is 20 V. Referring to the previous report, the hot-carrier effect causes the increase of the tail states in the band gap of the poly-Si film [10]. Fig. 2(b) gives the normalized $\mathrm{C_{GD}}$ behavior for the device before and after 200-s stress. It can be observed that the C–V behaviors for the stressed device show slight shift for the lower measuring frequency and the apparent shift and distortion for the higher measuring frequency. A more detailed discussion was reported in our other publication. [13] However, comparing the I–V and the C–V behaviors of the gate ac stress in the OFF region and the dc hot-carrier stress, respectively denoted as "stress condition #1" and "stress condition 2" hereafter, these two stress conditions result in the very similar degradation behaviors. The difference between them is just the degree of the degradation. Stress condition #2 leads to much worse degradation than stress condition #1.

The explicit degradation mechanism for the stress condition #1 is still not clear yet, but there are already several reports on the stress condition #2. The mechanism of hot-carrier stress is that the large electrical field across the drain-side junction and the channel carriers under this large field could achieve high energy and interact with lattice. Thus, the two key components, the electric field over the junction and the carriers under such field, can be used in analyzing the degradation mechanism of stress condition #1. Though in the previous paper, the degradation is found to be resulted from the electrical field over the junctions, there should be no induced carriers since during stress, the applied V_{GS} is kept all below its V_{TH}. One possible carrier source could be the junction leakage current, but it would be rather difficult to probe the current during stress. Also, the current level of such leakage current is much smaller than that under the dc hot- carrier stress. Still an alternative method can be adopted, that is, by changing the experiment to dc stress with large V_D biased in the OFF state, which would be studied in the following section and denoted as stress condition #3. The purpose of such study is that under large V_D in the OFF region, the drain-side junction would be subject to the large electric field and at the same time, there would be a small dc leakage current flowing across the junction. The comparison between the degradation behavior under stress condition #3 and the previous two degradation behaviors would help us find the explicit degradation mechanism for the different stress conditions.

C. DC OFF Region Drain-Biased Stress

Fig. 3(a) shows the transfer characteristics of the n-type poly-Si TFT before and after stress condition #3 and Fig. 3(b) shows the normalized $\mathrm{C_{GD}}$ curves before and after 200-s stress. The stress condition is that the stress V_{GS} is -5 V and V_{DS} is 20 V. The stress condition is chosen to make the large electric field occur at the drain junction but at the source side, the voltage difference is not large such that the degradation near the source side is small and thus simplifies the analysis. The I–V and C–V behaviors for the device after stress condition #3 are just very similar to those under the previous two kinds of stress conditions, as given in Figs. 1 and 2. However, in the case of stress condition #3, there is a large electric field over the drain

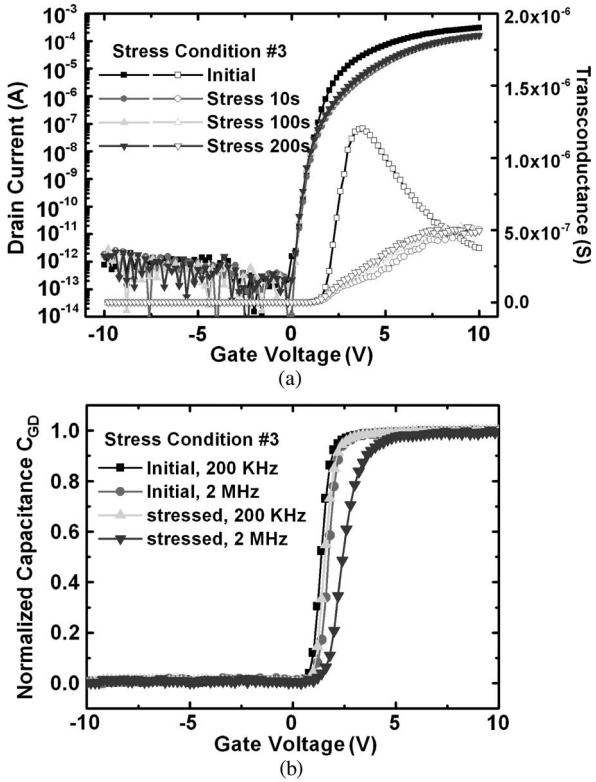


Fig. 3. (a) The current transfer behavior at $V_D = 5$ V and (b) the normalized gate-to-drain capacitance C_{GD} for the poly-Si TFT before and after 200-second dc OFF region drain-biased stress.

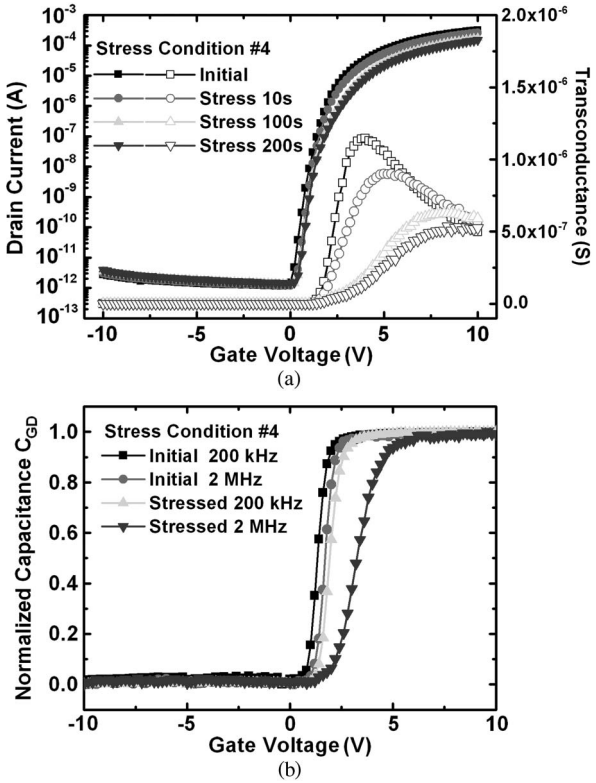


Fig. 4. (a) The current transfer behavior at $V_D = 5$ V and (b) the normalized gate-to-drain capacitance C_{GD} for the poly-Si TFT before and after 200-s gate ac stress.

junction but the only possible current source is the dc junction leakage. It could be surprising to find the degradation behavior is obvious and similar to the previous two stress conditions. The difference between them is just the degree of degradation.

The similarities between the degradation behaviors could enlighten us to find the explicit degradation mechanism. Under the OFF region drain dc stress, namely, stress condition #3, the depletion region near the drain side will be large and forms the large electric field near the drain-side junction. The gate voltage is purposely kept below the device's V_{TH}, making the device stay in the OFF region. In this case, only the junction leakage current could be present and thus it can be inferred that the degradation can be attributed to the effect of the leakage current under the large drain-side electric field. As compared to the dc hot-carrier stress, namely, stress condition #2, though the current level is different, device under drain dc stress also exhibits the degradation behaviors similar to the other two stress conditions. Compare the above three degradation behaviors, it may thus inferred that once the large electric field is applied across the junction, the device would then suffer the degradation similar to the hot-carrier effect, no matter the carrier source is the ON current, the dc junction leakage current or the current through the junction when the gate ac signal below its V_{TH} is applied. The difference between the effects of stress is just the degree of degradation.

Still, it would be of interest to compare the aforementioned degradation behaviors with another dynamic operation, namely, the gate ac signal toggling between the ON and OFF regions. It was previously reported that such degradation behavior can be categorized as another kind of hot-carrier stress, which may be relevant to our discussion. [5] The study and comparison of this behavior would be helpful to clarify the degradation mechanism.

D. Gate AC Stress Toggling Between ON/OFF Region

Fig. 4(a) gives the I_D–V_G curves before and after gate ac stress toggling between the ON/OFF regions, which would be denoted as stress condition #4 in the following discussion. The stress condition is that the stress gate voltage toggling between -15 V and 15 V while the source and drain electrodes are grounded. The stress gate voltage is of 500 kHz with 50% duty ratio. Fig. 4(b) gives the C–V behaviors for the device before and after 200-s stress. All these degradation behaviors are just similar to the behaviors under previous three stress conditions.

It is previously reported that the degradation of the device under stress condition #4 can be attributed to the induced carriers being swept to the source and drain regions as the gate voltage is switched from ON to OFF region. [5] Since the falling time of the gate pulse is around several hundred nanoseconds, the lateral electric field would be large and thus electrons could attain high energy and become hot carriers. These electrons could interact with the lattice and in turn lead to the generation of defect states. Such gate ac stress condition satisfies the aforementioned two factors for the hot-carrier effect, namely, the electric field over the junction and the carriers flow through the junction. In this case, the electric field over the junction

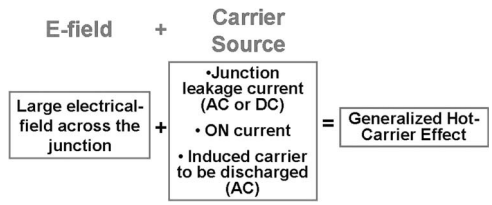


Fig. 5. Two components for forming the generalized hot-carrier stress effect.

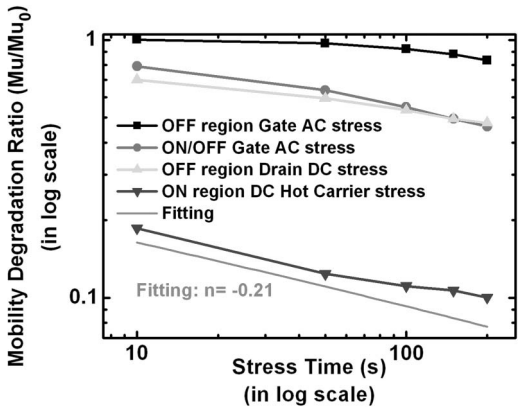


Fig. 6. Mobility degradation ratio for the four stress conditions.

becomes large as the gate signal is switched from ON to OFF and the carriers are the induced channel carriers.

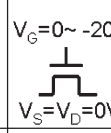
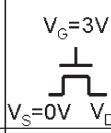
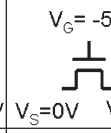
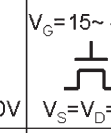
E. Discussions

Comparing all four stress conditions, it can be summarized that once the electric field is across the junction, the device can then suffer the hot-carrier-like degradation. The carrier source can be the dc ON current, the dc OFF current, the induced carriers to be swept to the source and drain region, and the leakage current through the junction when the gate ac signal in the OFF region is applied. Thus, all these four stress conditions can be categorized as the "generalized hot-carrier effect," as illustrated in Fig. 5. Though the current level and the voltage drop across the junction may be different from each other, it can be observed that the device will all suffer the similar degradation. The difference is just the degree of the degradation. Fig. 6 gives the mobility degradation ratio for the device under the four aforementioned stress conditions. It can be observed that the degradation behaviors under the four stress conditions all exhibit the similar power-law time dependence. The mobility degradation can be fitted with the power-law At^n, where A and n are fitting parameters. The fitting curves as well as the parameter n are also shown in the figures and it can be observed that the fitting curves can fit the degradation trend very well. This behavior resembles the degradation behavior of MOSFETs under dc hot-carrier effect. [14] Refer to the figure, it can be observed that the dc hot-carrier stress results in the most severe degradation, and the OFF region gate ac stress leads to the smallest degradation. A guessed table of the electric field magnitude and the carrier number as well as the degree of degradation for all four stress conditions is given in Table II. As for the electric field near the junction, dc operation should lead to a larger value of electric field and among stress condition #2 and #3, because in stress condition #3, the device is in the OFF state, the voltage difference $V_{\rm GD}$ would mainly occur at the drain junction and thus it poses the largest electric field near the junction. And for ac stress, because in stress condition #1, the device is kept in OFF state, the total 20 V voltage difference would almost be at the junctions. For stress condition #4, as the device is switched from $+15$ V to around its $V_{\rm TH}$, which is around 1.6 V, the channel can still be easily discharged since it is still in ON region. As the gate voltage is switched to a more negative voltage, namely, -15 V, the device is in the OFF state and the voltage difference $V_{\rm GD}$ would be mainly occurred at the junction. Though during the transient moment, the electric field distribution is hard to calculate, the value of the electric field near the junction should be less than that in stress condition #1.

As for the carrier number during stress, the number of the carrier should be the largest in stress condition #2 since this operation condition is in the ON region. Another one that partially operated in the ON region is stress condition #4. Though the applied gate voltage is larger than stress condition #2, many of the induced carriers may just be discharged during the period the gate voltage switching from $+15$ V to its $V_{\rm TH}$. Stress conditions #1 and #3 are in the OFF region so the current level would be relatively small and the leakage current in stress condition #3 would be larger than that in condition #1 since its electric field is larger. Considering the electric field and the carrier number for each stress condition and comparing it with the degradation in mobility, it is discovered that the degradation itself is more like a synergy effect containing the electric field and carrier number, and not simply depends on one of the two components. It can be found that stress condition #2, namely, the hot-carrier stress, leads to the worst degradation because of its high electric field and large number of channel carrier. Stress condition #3, namely, the OFF region drain dc stress, results in the worse degradation behavior because of the largest electric field, though its current is relatively small. Stress condition #1 and #4 are of relatively small electric field and carrier number, and since stress condition #4 induces more carriers, the degradation is more serious. In brief, by considering the electric field at the junction and the carrier number flow through the junction during stress, the degree of degradation can be roughly ranked and compared.

So far, it is clarified that how these generalized hot-carrier operation conditions would lead to different degree of degradation. And the degradation is found to be closely related to the electric field over the junction and carrier number. This finding helps to elucidate that the degradation mechanism is the carriers get accelerated by the large electric field near the junction and then interact with the lattice. Still there is one question left: Why such degradation behavior is not observed in the MOSFETs. There may be several reasons to this question. First, the operation voltage for poly-Si TFTs is usually above 10 V in the display applications, which is around two to three times larger than that for MOSFETs and thus the degradation would be much worse. Also, the poor crystallinity of the poly-Si film may be a critical factor, since it was reported that in poly-Si TFTs, the hot carrier effect is closely related to the behavior and number of the grain in the poly-Si film. [15] Another

TABLE II
GUESSED TABLE FOR THE ELECTRIC FIELD AT THE JUNCTIONS AND THE CARRIER NUMBER ALONG WITH THE MOBILITY DEGRADATION FOR EACH STRESS CONDITION

	Condition #1 	Condition #2 	Condition #3 	Condition #4 
Electric field (over the junction)	3	2	1	4
Carrier number (through the junction)	4	1	3	2
Degradation in mobility	4	1	2	3

Note: 1=largest 4=smallest

main reason is the difference in the leakage behavior between the MOSFETs and poly-Si TFTs. The main leakage current sources of MOSFETs are P-N reverse bias current (between the drain side and well junction), the subthreshold conduction (along with the drain-induced barrier lowering effect), the gate-induced drain leakage, and the punch-through effect, which, respectively, corresponds to different places inside or near the device. [16] On the other hand, the main leakage source of poly-Si TFT is in the drain-side depletion region. As the drain junction is largely reverse-biased, three conduction mechanisms associated with traps, namely, the tunneling, thermionic emission, and thermionic field emission, may happen. [17] Because poly-Si film is composed of small grains, in the drain-side depletion, a large number of traps would exist in the band gap, which in turn enhances the leakage behavior. This is very different from MOSFETs and thus the aforementioned degradation behavior is not observed in MOSFETs. This could also somehow explains why for poly-Si TFTs, once the large electric field is at the junction, the aforementioned generalized hot-carrier effect could occur.

As the advanced display applications adopting poly-Si TFT technology have hit the market, some more emerging applications, such as smart phone and touch panel with multiple value-added functions, require much more understanding of the reliability behavior and evaluation of poly-Si TFTs under various operation conditions. Since in these applications, the TFTs are expected to work as the in-pixel switches as well as the circuit elements in various kinds of circuits, the poly-Si TFTs would be operated under more complicated conditions in addition to simply switching conditions. Though there could be many kinds of operation conditions, the impact of this paper is that as the large electric field is at the source or drain junction, the device may then suffer the generalized hot-carrier effect, no matter the device is in the ON state, the OFF state or at the transient state toggling between the ON/OFF region. The idea and characterization of the generalized hot-carrier effect under various kinds of stress conditions and the study of the mechanism would help designers in designing the circuit with better understanding of device reliability and circuit performance under various operation conditions.

IV. CONCLUSION

Four stress conditions are performed and the corresponding degradation behaviors are compared to find the explicit degradation mechanism for the gate ac stress in the OFF region. Two factors are taken into the discussion of the hot-carrier stress, namely, the electric field at the junction and the carrier through it. It is discovered that, if the large electric field is at the junction, the device would suffer the generalized hot-carrier stress. The detailed degradation mechanism for the device under these generalized hot-carrier stress is attributed to the current under the large electric field and electrons may attain sufficient high energy to act as the hot carrier. This finding would be beneficial for the further modeling and reliability designing of the poly-Si TFTs in the advanced circuitry.

REFERENCES

[1] H. Ohshima and Y. Matsueda, "Poly-Si TFT and driver integration technology," *Electron. Commun. Jpn. (Part II: Electron.)*, vol. 77, no. 7, pp. 46–55, Jul. 1994.
[2] Y. Nakajima, "Latest development of 'system-on-glass' display with low temperature poly-Si TFT," in *Proc. SID Tech. Dig.*, 2004, pp. 864–867.
[3] H. Ohshima and S. Morozumi, "Future trends for TFT integrated circuit on glass substrate," in *IEDM Tech. Dig.*, 1989, pp. 157–160.
[4] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi, "Reliability of low temperature poly-Silicon TFTs under inverter operation," *IEEE Trans. Electron Devices*, vol. 48, no. 10, pp. 2370–2374, Oct. 2001.
[5] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi, "Reliability of high-frequency operation of low-temperature polysilicon thin film transistors under dynamic stress," *Jpn. J. Appl. Phys. 2, Lett.*, vol. 39, no. 12A, pp. 1209–1212, Dec. 2000.
[6] Y.-H. Tai, S.-C. Huang, and P.-T. Chen, "Degradation mechanism of poly-Si TFTs dynamically operated in OFF region," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 231–233, Mar. 2009.
[7] D. K. Schroder, *Semiconductor Material and Device Characterization,* 2nd ed. New York: Wiley, 1998, pp. 337, 543.
[8] Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi, "Analysis of hot carrier effects in low temperature poly-Si TFTs using

device simulator," in *Proc. IEEE Int. Conf. Microelectron. Test Struct.*, 2001, pp. 251–256.
[9] E. Takeda, "Hot-carrier effects in scaled MOS devices," *Microelectron. Reliab.*, vol. 33, no. 11/12, pp. 1687–1711, Sep. 1993.
[10] K. C. Moon, J.-H. Lee, and M.-K. Han, "The study of hot-carrier stress on poly-Si TFT employing C–V measurement," *IEEE Trans. Electron Devices*, vol. 52, no. 4, pp. 512–517, Apr. 2005.
[11] C. T. Wang, *Hot Carrier Design Considerations for MOS Devices and Circuits*. New York: Van Nostrand Reinhold Press, 1992, pp. 62–67.
[12] G. Groeseneken, R. Bellens, G. Van den bosch, and H. E. Maes, "Hot-carrier degradation in submicrometre MOSFETs: From uniform injection towards the real operating conditions," *Semicond. Sci. Technol.*, vol. 10, no. 9, pp. 1208–1220, Sep. 1995.
[13] Y.-H. Tai, S.-C. Huang, C. W. Lin, and H. L. Chiu, "Degradation of the capacitance-voltage behaviors of the low-temperature polysilicon TFTs under DC stress," *J. Electrochem. Soc.*, vol. 154, no. 7, pp. H611–H618, 2007.
[14] S.-H. Renn, J.-L. Pelloie, and F. Balestra, "Hot-carrier effects and reliable lifetime prediction in deep submicron N- and P-channel SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 45, no. 11, pp. 2335–2342, Nov. 1998.
[15] Y. Uraoka, K. Kitajima, H. Kirimura, H. Yano, T. Hatayama, and T. Fuyuki, "Degradation in low-temperature poly-Si thin film transistors depending on grain boundaries," *Jpn. J. Appl. Phys. 1, Regul. Papers Short Notes Rev. Papers*, vol. 44, no. 5A, pp. 2895–2901, May 2005.
[16] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.
[17] K. R. Olasupo and M. K. Hatalis, "Leakage current mechanism in sub-micron poly silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1218–1223, Aug. 1996.

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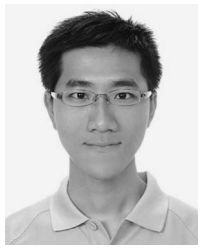

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