行政院國家科學委員會補助專題研究計畫 **■ 成 果 報 告**
□期中進度報告

金屬閘極金氧半場效電晶體關鍵技術

Key Technologies of Metal Gate MOSFET

計畫類別：■ 個別型計畫　　□ 整合型計畫
計畫編號：NSC 92－2215－E－009－001－
執行期間：　90 年 08 月 01 日至　93 年 07 月 30 日

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中　華　民　國　93 年　10 月　25 日

摘　要

本報告包含本三年期計畫之全部成果。內容分為三個部分：金屬閘極技術、高介電常數介電層技術、製程整合技術。

金屬閘極部分，本計畫提出以具有高、低功函數之金屬形成合金，藉由元素比例調變功函數的技術，以 Ta-Pt 以及 Ti-Pt 為實例，功函數調變幅度可達 1 電子伏特以上，符合種金氧半場效電晶體的需求。合金閘極的熱穩定性可達約 900°C，離子植入對功函數影響極微，製程穩定性極佳。金屬氮化物閘極方面，稍早的計畫已探討過 TaN 閘極，本計畫則研究 MoN 以及 WN 閘極的性質。藉由反應性離子濺鍍的氮氣流量可以調變金屬氮化物中的氮含量，功函數會隨之改變，但是調變幅度僅有約 0.4 電子伏特。MoN 的熱穩定很好，氮含量較高的 WN 在高溫下，會發生氮氣逸出(out-gassing)問題，造成薄膜剝離。WN 在 HfO_2 上會有費米能階固定(Fermi-pinning)的問題，MoN 則無此現象。顯見 MoN 是較佳的金屬氮化物閘極材料。

高介電常數介電層技術方面，著重在 HfO_2 的性質。以物理氣相沈積方式沈積 HfO_2 會因為氧氣電漿與矽基板反應生成近似 SiO_2 的介面層，使得電容等效二氧化矽厚度偏厚(CET)，即使使用表面氮化處理，仍然效果不佳，恐將無法實用。MOCVD 可以形成良好的 HfO_2 薄膜，本計畫改變表面處理方式、氣體導入順序、氣體組成比例、沈積溫度等製程參數，確定高溫(500°C)、高氧流量(500 sccm)條件下沈積的薄膜性質最佳。此條件沈積之薄膜經高溫退火，等效氧化層厚度增加極微，漏電流亦不至因結晶化而增加。穿透式電子顯微鏡分析顯示，退火後局部結晶會造成漏電流增加，但是全面結晶為緊密的複晶型態則不會有漏電流問題。

製程整合技術方面，首先探討高介電常數介電層的邊緣電場導致能障降低（FIBL）效應對奈米尺度元件之影響。藉由模擬，確認邊緣電場來自於閘極與汲極重疊處，降低重疊量可以有效改善此一問題。結合低閘極與汲極重疊、介面層、導電性側壁子等技術，可將此效應造成的漏電流增加幅度降低到兩倍以下。SOI 結構有較佳的免疫力，因此在 45 奈米世代以下，FIBL 效應不至於構成威脅。Hf 在 SiO_2 以及 Si 中擴散速率不高，也不是以離子狀態存在，對於元件隔離以及 pn 接面漏電幾乎不造成影響，不是嚴重的污染物質。本計畫最後開發出以 HF+IPA 溶液去除 HfO_2 的技術。適當的比例可以得到可接受的蝕刻速率以及對二氧化矽較高的蝕刻率選擇比，可應用於閘極蝕刻後的 HfO_2 薄膜去除，不至於影響到元件隔離結構。

本計畫三年內有兩名博士研究生、六名碩士研究生、四名大學生參與計畫執行。六名碩士研究生中的五名已經陸續獲得碩士學位。計畫成果已發表三篇 SCI **期刊論文、六篇研討會論文，另有三篇期刊論文在審查中。近期的成果將會陸續撰寫成至少三篇期刊論文發表。專利部分提出九件專利申請，其中兩件已經獲證，另七件在審查中。**

關鍵字：金屬閘極、高介電常數介電層、功函數、合金閘極、金屬氮化物、二氧化鉿、費米能階固定、邊緣電場導致能障降低、金屬污染、濕蝕刻。

Abstract

This final report includes all of the results of the 3-year project. This report is divided into three parts : metal gate technology, high dielectric (high-k) constant dielectric technology, and process integration issues.

In the part of metal gate technology, the novel method of work function modulation was proposed at first. With a proper composition of high and low work function metals, the work function of the metal alloys can be modulated from 4.16eV to 5.05eV continuously. The alloys show good thermal stability and inner chemical activity on both silicon dioxide and hafnium dioxide up to 900°C. The work function does not change after the incorporation of impurities of arsenic ions, boron ions and phosphorus ions. Therefore, the control of threshold voltage of the alloy-gate MOSFET could be easier, and not be disturbed by the S/D implantation process. Metal nitrides are possible metal gate candidates. MoN and WN were investigated in this project. 4. The work function of both metal nitrides increase with the increase of the nitrogen flow rate. The modulation range of work function can be up to 0.4eV from pure metal to metal nitride. 3. Nitrogen within WN_x would separate out quickly during rapid thermal annealing and caused the film to crack. MoN_x films do not exhibit Fermi-level pinning on both SiO_2 and HfO_2 while Fermi-level pinning of WN_x on HfO_2 was observed. Therefore, MoN is a better choice if metal nitride should be used as metal gate.

IN the part of high-k dielectric, we focused on the HfO_2 film. It is observed that using physical vapor deposition technique, it is difficult to totally eliminate the formation of interfacial SiO_2 layer. During reactive sputtering deposition of HfO_2 layer, an interfacial SiO_2 layer thicker than 3 nm would be grown. Such an unusual thick SiO_2 layer is formed due to the enhanced oxidation of O-radicals generated in the sputtering chamber. The traced oxygen in the sputtering chamber plays critical role on the formation of interfacial layer. The reactive sputtering is not a good method to prepare HfO_2 layer with negligible interfacial SiO_2 layer. For MOCVD, higher deposition temperature and purer O_2 ambient is benefit to the leakage current performance under the same capacitance-equivalent-thickness (CET). Higher O_2 flow rate supply more sufficient O_2 in reaction chamber is also important deposit high quality HfO_2. As the deposition temperature increases to 500℃, the surface treatment and post deposition annealing temperature play minor role on the leakage current. According to the above results, the best deposition conditions are recommended as : deposition temperature : 500℃, deposition ambient : pure O_2 ambient, O_2 flow rate:500sccm, bas pressure:5mbar. Nano-crystals are observed in films deposited at any conditions. For HfO_2 films deposited at

low temperature or with insufficient O_2 supply, the nano-crystals are separated by amorphous region and show round shape. The boundary layer accounts for the leakage current of these samples. Hf-precursor decomposes completely during high temperature deposition, and therefore, with sufficient O_2 supply, the film becomes polycrystalline completely. The lack of crystal-amorphous boundary layer results in very low leakage current.

In the part of integration technology, Fringing-Filed-Induced Barrier Lowering (FIBL) effect, Hf contamination, and HfO2 wet etching were studied. TCAD tools were used to investigate the FIBL effect of 25 nm devices. The key factor to affect the FIBL effect is the gate to drain overlap length. Most of the fringing field originates from this region. It is known that stack gate dielectric scheme with buffer layer (k<15) between high-k dielectric and Si substrate can relax the FIBL effect. Conductive spacer is another effective method to reduce the FIBL effect but the process is more complicated. A fully depleted SOI device shows better resistance to FIBL induced I_{off} degradation. Therefore, it is concluded that although FIBL effect can not be eliminated, its impact on device performance is diminished at sub-45nm technology node and beyond with suitable device structure. Hf element been knocked into source/drain or field oxide during ion implantation for source/drain extension may be a concern in device fabrication. Fortunately, since the diffusivity of hafnium is very low in both Si and SiO_2, we could not observe the effect of hafnium contamination. Our study implies that from the contamination point of view, the HfO_2 out of gate electrode have not to be removed immediately after gate patterning. In this project, we also developed a HF+IPA mixture which can etch HfO_2 film with reasonable etching rate and acceptable etching rate selectivity with respect to SiO_2. These results greatly relax the constraint on device process integration.

In the past three years, 2 Ph.D students, 6 graduate students, and 4 under-graduate students involved this project. Among them, 5 of the 6 graduate students have received their MS degree. Parts of the results have been published as 3 SCI journal papers and 6 conference papers. Another three SCI journal papers are under reviewing procedure. Recent results will be written as 3 SCI journal papers at least. We also applied 9 patents. Two of them have been authorized and the other seven are pending.

Key Words : Metal gate, high dielectric constant dielectric, work function, alloy gate, metal nitride, Fermi-level pinning, hafnium oxide, fringing-field-induced barrier lowering (FIBL), metal contamination, wet etch

Contents

Chapter 1
Introduction

1-1 Project Background

As conventional CMOS devices are scaled down to improve performance, gate engineering becomes a crucial issue. It was found that the conventional gate material, poly-silicon, suffered from gate depletion, high gate resistance, and boron penetration into the channel region in sub-100 nm CMOS technology node [1-5]. Poly-Si gate depletion increases the equivalent gate dielectric thickness by about 3 Å and degrades channel current drive capability [1-3]. High gate resistance increases the RC time delay to degrade high frequency performance. Salicide technology can reduce the gate resistance but it is difficult to maintain a proper aspect ratio for gate stack in scaled devices [4]. Boron penetration in PMOSFET reduces the ability of threshold voltage control and gate oxide reliability [1,5]. High dielectric constant (high k) materials are expected to replace SiO_2 for scaling gate dielectric thickness below 1.5 nm where direct tunneling current through SiO_2 may be too high to be acceptable [4]. Unfortunately, poly-Si is incompatible with most high k materials due to chemical reaction or interface layer formation [6,7]. It has been demonstrated that metal gate devices are free from gate depletion, high resistance, and boron penetration. Therefore, there is an immense interest in metals to be a replacement of gate electrode.

As the gate oxide thickness of metal–oxide–semiconductor (MOS) devices is scaled down to below sub-1.5nm tunneling current through gate dielectrics and reliability would become serious problems. Therefore, high dielectric constant (high-k) materials, such as ZrO_2-based [8] HfO_2-based [9] and Al_2O_3-based [10] metal oxide insulators, have been received considerable attention as alternative dielectric materials. They have been demonstrated to suppress the leakage current significantly as compared to the traditional SiO_2-based dielectrics with the same equivalent oxide thickness (EOT) because of their thicker physical thickness. Among these candidates, HfO_2 and its silicate not only have relatively high dielectric constants and wide band gaps, but also have been shown impressively thermal stability in contact with silicon substrate [11]. Therefore, HfO_2-based insulators would be the promising candidates for the sub-1.5nm gate dielectric generation. Although several groups have demonstrated the excellent electrical properties of MOS capacitors with the HfO_2-based gate dielectrics in recent years [12-14] there are still many

challenging issues, such as formation of interfacial layer and mobility degradation in MOSFET devices, have to be further investigated.

Even if suitable high-k dielectric technology can be developed successfully, a side effect called fringing-induced barrier lowering (FIBL) arising from the use of high-k gate dielectric has been reported [15-20]. The fringing electric field originated at drain penetrates into channel through the high-k gate dielectric and suppress the barrier height from source to channel. Therefore, the off-state drain current (I_{off}) increases and the maximum allowable k value of high-k dielectric is limited by the FIBL effect. Some works discussed the effect of device structure on FIBL. Yeap et al reported that remaining high-k dielectric under spacer greatly enhances the FIBL [15]. It is also proposed that an oxide buffer layer under high-k dielectric can suppress the FIBL. Therefore, the impact of high-k dielectric on device structure selection at sub-65nm technology node must be examined.

Most high-k materials, including HfO_2, belong to metal oxides, and metal contamination issue must be considered carefully. Metal contamination may come from equipment itself. It had been published that wafer surface becomes rough after standard RCA clean in hafnium-contaminated solution so that gate oxide integrity is degraded [21]. No literature studies metal contamination issues from the metal oxide on device. The self-contamination is very important to determine the device integration scheme.

High-k material is difficult to be etched by either dry etch or wet etch especially for thin film after high temperature annealing [22]. It is hard to remove HfO_2 film after gate electrode etching because dry etching of HfO_2 may damage the S/D extension region and wet etching of HfO_2 exhibit very poor selectivity between high-k dielectric and field oxide. Novel method must be developed to remove HfO_2 with low damage and high selectivity to the pre-existed material before integrating HfO_2 into MOSFETs.

According to the numerous issues mentioned above, we proposed a three-years project entitled “Key Technologies of Metal Gate MOSFET“ to try to solve these issues. This is the final report of this project.

1-2 Report Organization

This final report is organized as three parts : metal gate technology, high dielectric (high-k) constant dielectric technology, and process integration issues.

In chapter-1, we briefly explain the background of this project and the report organization. In chapter-2, a novel binary alloy was proposed for wide range work function

modulation. In chapter-3, the thermal and process stability of the proposed alloy gate were examined. In chapter-4 and chapter-5, metal nitrides of MoN and WN as gate electrode were examined, respectively.

Chapter-6 discusses the electrical properties and the interfacial layer formation of HfO2 film prepared by PVD method. The electrical characteristics of HfO2 film prepared by MOCVD are presented in chapter-7. The physical analyses of the MOCVD HfO2 film are discussed in chapter-8.

The FIBL effect of nano-scale MOSFET with channel length down to 25 nm was studied using TCAD tools and the results are shown in Chapter-9. Hf contamination due to the incorporation of HfO2 into front-end process of line is studied in chapter-10. We also developed novel chemistry to remove HfO2 film with low damage and high selectivity to SiO2. The results are presented in chapter-11.

Chapter-12 summaries the important conclusion achieved in this three years. The publications and patents generated from the execution of this project are listed in the appendix.

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Chapter 2
Alloy Gate Technology

2-1 Introduction

As MOS devices are scaled down, the gate oxide thickness will decrease to be thinner than 2 nm. Several problems were observed together with the thin down of gate oxide such as poly-Si gate depletion, boron penetration, quantum effect, and gate leakage current [1-4]. Using metal to replace poly-Si as gate electrode can solve the first two problems [5,6]. However, to fabricate surface channel devices with suitable threshold voltage (V_{th}), the gate electrode should have suitable work function (Φ_m), i.e. metals with F_m 4.0-4.2eV and F_m 5.0-5.2eV are suitable for NMOSFETs and PMOSFETs, respectively. It was reported that the Φ_m of metal nitrides could be modulated with the nitrogen content [7-9]. Unfortunately, the magnitude of modulation is not wide enough. Recently, metal alloys were proposed for work function modulation [10, 11]. However, the F_m drops abruptly once new alloy phase forms. Ni-Ti inter-diffusion was also proposed to produce dual work function metal gate [12], but the thermal stability is poor.

In this work, we propose a new Ta-based binary alloy system of Ta-Pt and Ta-Ti. Wide range and continuous Φ_m modulation from 4.16 eV to 5.05 eV could be achieved.

2-2 Experiments

A simple MOS structure was fabricated to characterize the binary alloy systems. The starting material was (100)-oriented phosphorus doped Si wafer. Following standard RCA cleaning, gate oxide of 11 nm thick was thermally grown. The gate electrodes were patterned using the lift-off process. Ta_xPt_y and Ta_xTi_y alloys were co-sputtered to a thickness of 60 nm on patterned photo-resist. Table 2-1 lists the deposition conditions and the atomic composition analyzed with Rutherford Backscattering Spectroscopy (RBS). After gate patterning, samples were annealed in N_2 ambient at 400, 500, and 600℃ for 30 min followed by Al deposition at the back.

2-3 Results and Discussion

The work function of an A_xB_{1-x} alloy can be approximately expressed as

$$\Phi_m = x\Phi_{m,A} + (1-x)\Phi_{m,B} + x(1-x)\left[\frac{(\Phi_{m,A} - \Phi_{m,B})(r_A - r_B)}{xr_A + (1-x)r_B}\right]$$

$$= x\Phi_{m,A} + (1-x)\Phi_{m,B} + x(1-x)\left[\frac{(\Phi_{m,A} - \Phi_{m,B})(\frac{r_A}{r_B} - 1)}{x\frac{r_A}{r_B} + (1-x)}\right]$$

, where $\Phi_{m,A}$ and $\Phi_{m,B}$ are the pure constituent work functions of A and B, respectively, and ρ_A and ρ_B are the pure constituent total densities of states [14]. The density of states at Fermi energy $\rho(\varepsilon_F)$ is proportional to the electronic specific heat constant $C_e = \frac{1}{3}p^2 r(e_F)k_B^2 T$, where k_B is Boltzmen constant and T is temperature. In the case of $C_{e,A}/C_{e,B}$~1, the Φ_m changes with *x* linearly as $\phi(x) = \phi_B + x(\phi_A - \phi_B)$ [15]. The C_e values of Pt, Ta, and Ti are 6.8, 5.9, and 3.35 mJ/mole/K^2, respectively [16]. Since the C_e values of Ta and Pt are very close, a nearly linear correlation can be expected.

The approximate work function ($\Phi_{m,app}$) of annealed samples was extracted by comparing the measured C-V curves with the theoretical C-V curve [9, 13]. The $\Phi_{m,app}$ is defined as $F_{m,app.} = F_m - Q_{ss}/C_{ox}$, where Q_{ss} is effective oxide charges and C_{ox} is capacitance at accumulation mode. As the gate oxide thickness is 11 nm, a Q_{ss} of $1x10^{11}$ cm^{-2} results in aF_m deviation of 0.05eV only. Fig. 2-1 shows the extracted$F_{m,app}$ of 400℃ annealed samples. The Q_{ss} of poly-Si gate devices is around $5x10^{10}$ cm^{-2}. The Q_{ss} of metal gate devices might be higher than that of poly-Si gate. However, since the interface state density (D_{it}) of metal gate devices is similar to that of poly-Si gate, it is believed that the Q_{ss} of metal gate will not be much higher than that of poly-Si gate. Therefore, the $F_{m,app}$ should be very close to the F_m. With increasing contents of high F_m elements, Pt in Ta-Pt alloys or Ta in Ta-Ti alloy, the$F_{m,app}$ shifts toward higher value. The $Ta_{0.63}Ti_{0.37}$ alloy and $Ta_{0.58}Pt_{0.42}$ alloy show $\Phi_{m,app}$ of about 4.16eV and 5.05 eV and is suitable for NMOSFETs and PMOSFETs, respectively. As expected, the $\Phi_{m,app}$ can be modulated continuously by adjusting the atomic composition of the alloy. This property allows for the use of the alloy system to obtain precise work function. For example, fully-depleted SOI devices require Φ_m of close to 4.6 eV [17], and can be achieved using the alloys with Ta/Pt ratio close to 0.74/0.26.

Fig. 2-2(a) and 2(b) show the Transmission Electron Microscopic (TEM) micrographs of $Ta_{0.58}Pt_{0.42}/SiO_2$ and $Ta_{0.63}Ti_{0.37}/SiO_2$ structures after annealing at 600℃, respectively. The alloys are almost amorphous and no interfacial layer was formed. Furthermore, no compound phases were observed from the X-ray diffraction (XRD) spectrums. The change of EOT after

annealing at 600℃ is less than 1%, i.e. less than 0.1nm. These results imply that the alloys are thermally stable up to 600℃ on SiO_2. This temperature is high enough for replacement gate process and is better than most of low work function elemental metals such as Ti [18].

Fig. 2-3(a) shows that the $\Phi_{m,app}$ decreases slightly with the increase of annealing temperature. Since the alloys are thermally stable on SiO_2, this phenomenon cannot be attributed to the interaction between alloy and oxide. Fig.2-3(b) shows that the D_{it} also increases with the increase of annealing temperature. It is thus postulated that the decrease of $\Phi_{m,app}$ comes from the thermal stress generated oxide charges. To reduce the effect of thermal stress, a stack gate electrode of W(50nm)/Ta-Pt(10nm) is proposed. The thermal expansion coefficient of W ($4.4x10^{-6}$℃$^{-1}$) is lower than that of Pt ($9.0x10^{-6}$ ℃$^{-1}$) and Ta ($6.6x10^{-6}$℃$^{-1}$) and is close to that of Si ($2.4x10^{-6}$℃$^{-1}$). Another benefit of using stack structure is that the resistivity of W ($5.3x10^{-6}$ ohm-cm) is much lower than the resistivity of alloys (> $300x10^{-6}$ohm-cm). In this structure, the Ta-Pt alloy determines the work function and the W layer serves as the main conducting material.

Fig.2-4 shows the C-V characteristics of W(50nm)/Ta-Pt(10nm)/HfO_2(5nm)/p-type Si structure after annealing at 600℃ and 800℃ in N_2 ambient for 30 minutes. The apparent kink in the curve of 600℃ annealed sample points to the insufficient passivation of interface states at the HfO_2/Si interface. The smaller kink and negligible hysteresis phenomenon of the 800℃ annealed sample imply that the stack structure is stable up to 800℃. The reduction of kink and hysteresis also confirms that thermal stress can be reduced by the stacked metal gate. The flatband voltage difference between 600 and 800℃ annealed devices may be attributed to the reduction of Q_{ss} and/or the change of Φ_m due to interaction between W and Ta-Pt or between Ta-Pt and HfO_2. A 900℃ annealing distorts the C-V characteristic. The stability of metal gate/high K dielectric system is under investigation.

2-4 Conclusions

This work explores the characteristics of the binary alloys Ta-Pt and Ta-Ti for gate electrode application. With a proper composition of high and low work function metals, the work function of the metal alloys can be modulated from 4.16eV to 5.05eV continuously. The resistivity of Pt-Ta alloy is high and thermal stress of thick Ta-Pt alloy may generate oxide charges. Therefore, stack structure with a low resistivity and low stress layer as main conducting layer and the proposed alloy layer as work function control layer, for example W/Ta-Pt, is preferred for actual application.

To implement metal gate into CMOS process is tough not only for alloy gates. Metal gates for NMOS and PMOS can be patterned separately [19]. Using metal ion implantation to form various alloys is another choice; it depends on the maturity of metal ion implantation technology. However, gate electrode with work function near mid-gap of Si should be used for FD-SOI. The proposed alloy system shows the advantage of precise work function control in this aspect.

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Table 2-1. Deposition conditions used in this work and atomic compositions of alloys analyzed with Rutherford backscattering spectroscopy (RBS)

Sample ID	Sputtering Power (W)			Atomic Ratio (%)		
	Ta	Pt	Ti	Ta	Pt	Ti
A1	50	0	50	63	0	37
A2	150	0	0	100	0	0
A3	100	30	0	74	26	0
A4	50	30	0	65	35	0
A5	30	30	0	58	42	0
A6	0	30	0	0	100	0

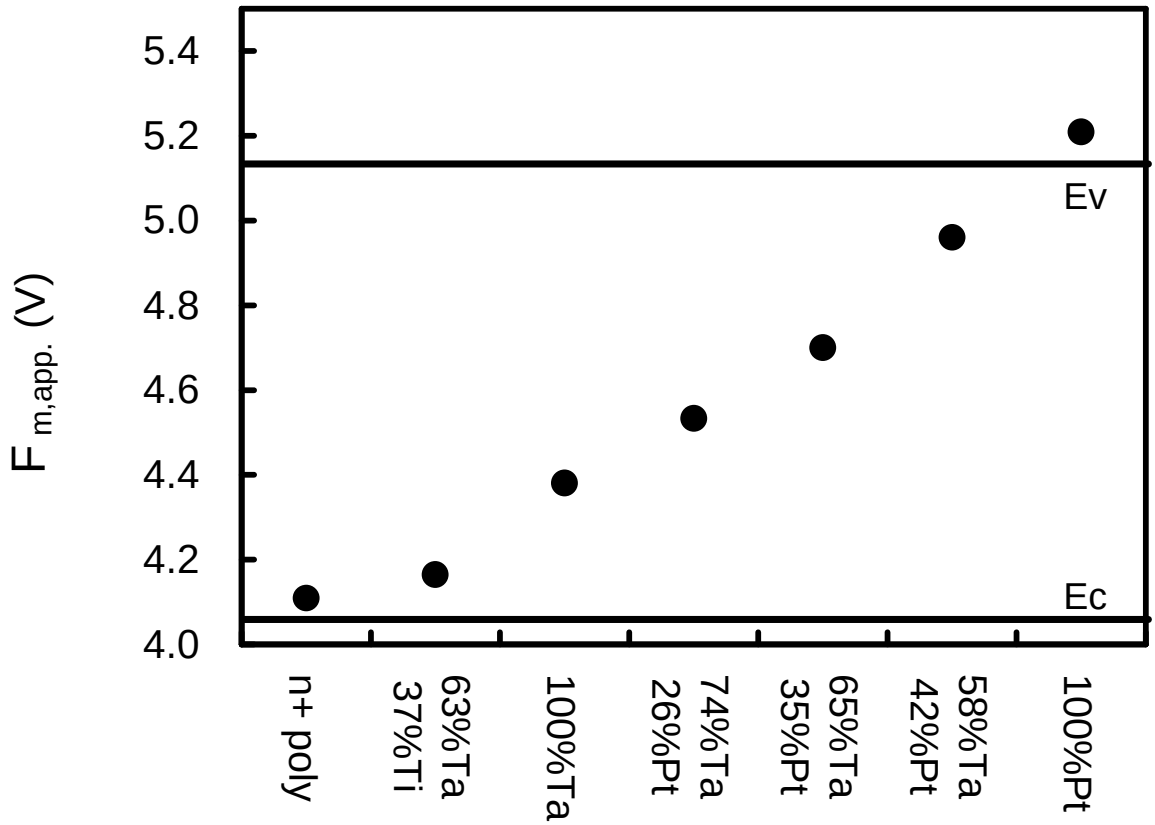

Fig.2-1. Extracted approximate work function ($\Phi_{m,app.}$) of 400℃ annealed samples.

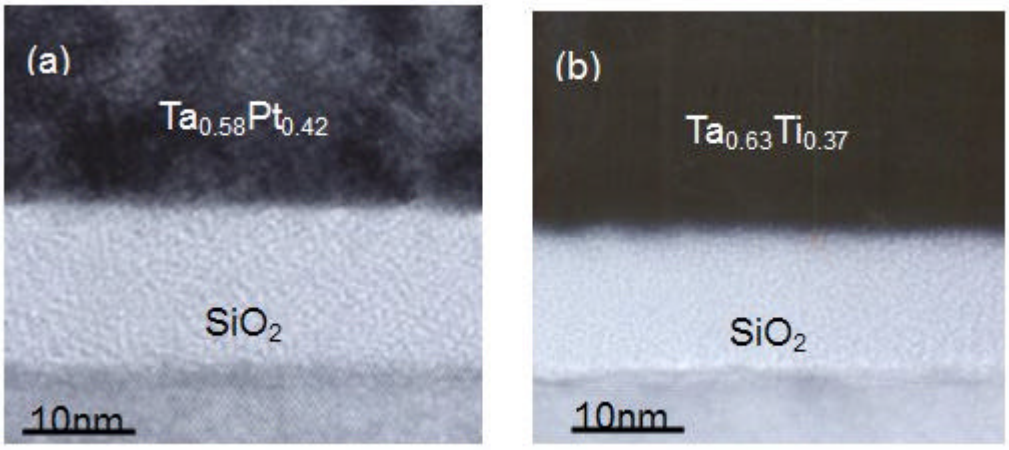

Fig.2-2. Cross-sectional TEM micrographs of (a) $Ta_{0.58}Pt_{0.42}/SiO_2$ structure and (b) $Ta_{0.63}Ti_{0.37}/SiO_2$ structure after annealing in N_2 ambient for 30 minutes at 600℃. No Interfacial reaction is observed.

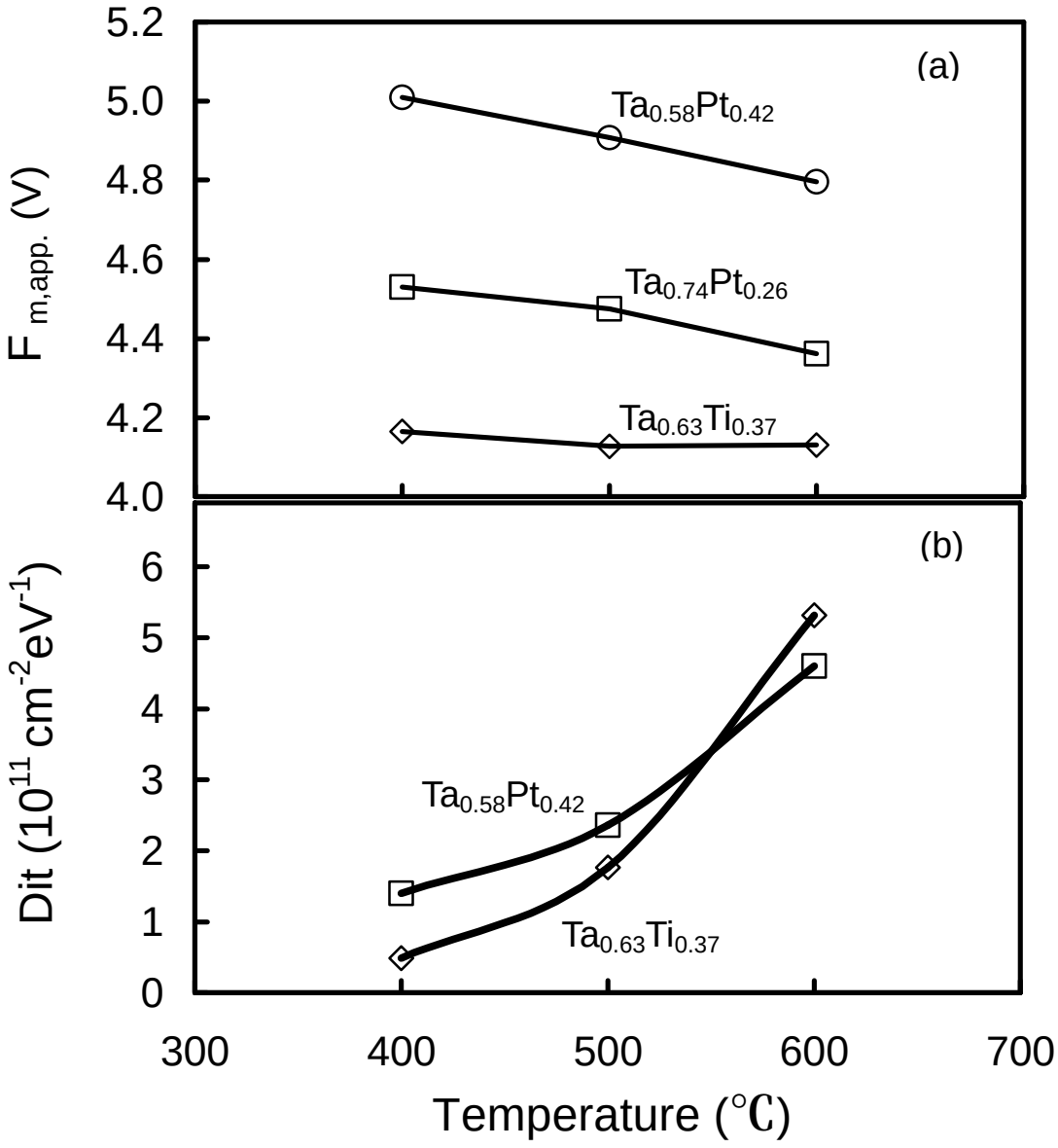

Fig.2-3. (a) Approximate work function ($\Phi_{m,app}$) and (b) interface state density (D_{it}) versus annealing temperatures.

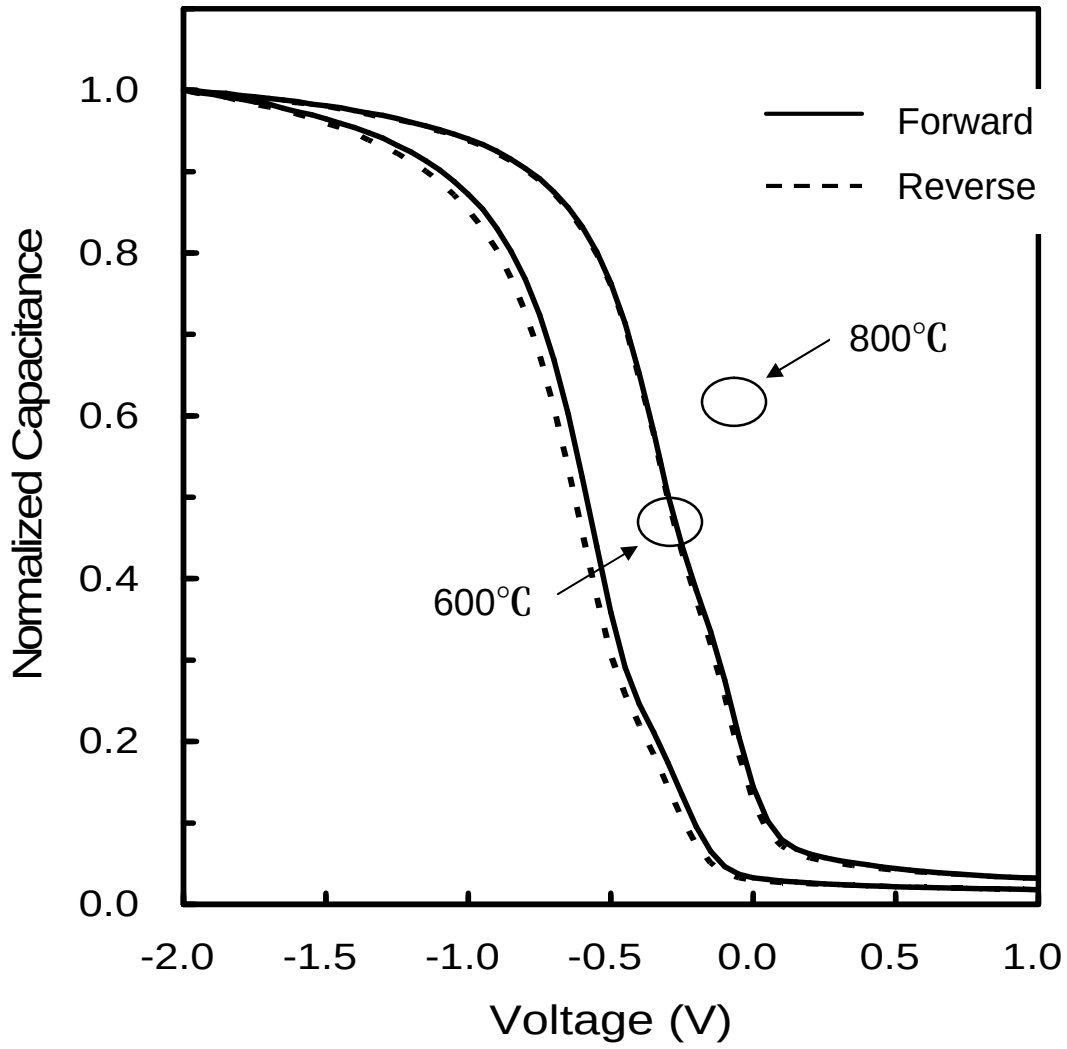

Fig.2-4. Capacitance-voltage characteristic of the $Ta_{0.58}Pt_{0.42}/HfO_2$/p-Si sample after annealing at 600℃ and 800℃ in N_2 ambient for 30 minutes.

Chapter 3
Process Stability of Alloy Gate

3-1 Introduction

Metal gates are currently proposed to replace the poly-Si gate beyond 65nm technology node[1] in order to solve the problems of poly-depletion and boron penetration [2-6]. However, before any metal gates can replace the poly-silicon gate, they must be able to be compatibly integrated into the process of MOSFET fabrication and should provide higher device performance than that of poly-silicon gate. To integrate the metal gate, there are two kinds of metal gate processes, the dummy gate process [7-10] (gate last process) and conventional gate process (gate first process) [11-13]. Compared with conventional processes, the dummy gate process has extra steps including the chemical-mechanical polishing (CMP) step and dummy-gate-removal so that the gate last process is more complicated [7-10]. Its main benefit is the lower temperature, which protects the thermal stability of metal gates since most metals may react with the gate dielectric at temperatures higher than 600°C. The temperature of the gate last process should be controlled to be lower than 500°C after the metal gate deposition. On the other hand, metal gates should withstand the high temperature of source/drain (S/D) activation process to be integrated with a relatively simple process of the conventional process [11-13]. The key factor for those metal gates is that they should be chemical inert as well as they should have the immunity to avoid dopant channeling during source/drain ion implantation [14, 15]. For device performance, metal gates should have proper work function (F_m) to obtain suitable threshold voltage for the n-type or p-type MOSFETs [16, 17]. The work function of metals must be 4.1-4.4eV for NMOSFETs and 4.8-5.1eV for NMOSFETs, respectively. In previous chapter, we showed how the work function of the binary metal alloys can be easily modulated to a suitable value for NMOSFETs or PMOSFETs by adjusting atomic ratios of the composition [18]. Moreover, a wide range of work functions should be available by the mixture of the two metal elements which contains a metal with much high work function, near the valence band of silicon, and a metal with quite low work function, near the conduction band of silicon, such as Ta-Pt alloys [18] or Ru-Ta alloys [19, 21]. In this work, we examine the thermal stability of the Ta-Pt alloys with tunable work function [18, 22, 23]. The work function effect of column III or V element impurity incorporation is also studied.

3-2 Experiments

Simple MOS capacitors with gate electrodes of Ta-Pt alloys were fabricated on p-type Si wafers. The beginning is the 6-inch p-type (100) oriented silicon wafers. After wafer cleaning, the gate oxide was thermally grown to 6nm thick in dry-oxygen atmosphere at 900 °C. After gate oxidation, the metal gates would be completed by lift-off process. Metal gate patterns were first defined with a conventional lithography process. Then, the alloys were deposited in a co-sputtering system to 55nm thick, and the sputtering power of Ta and Pt targets were set to DC 30 and RF 35 watts, or DC 20 and RF 40 watts. The wafers were split and than some samples were implanted with 5e15 cm^{-2} dosage of arsenic ions (As^+), phosphorous ions (P^+), or boron di-fluoride ions (BF_2^+). After implantation, metal gates were finished by the lift-off process. Then, all MOS capacitors were capped with 60nm thick silicon nitride films which were deposited in a plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C, in order to avoid out-gassing of impurities when the samples were annealed at high temperatures. Samples were annealed at temperatures between 400 and 800 °C in a rapidly thermal annealing (RTA) system for 30sec. Finally, the contact windows of gate electrodes were patterned by conventional lithography and wet etching process, and backside contacts were formed with an aluminum film deposited in a thermal evaporation system. The samples for the study of thermal stability was deposited with sputtering power of DC 100 watts and DC 30 watts for Ta and Pt targets, respectively, in order to form a Ta-rich alloy film, since Ta is more chemically reactive than Pt. Its annealing conditions of the higher thermal budget were from 400 °C to 800 °C in a horizontal furnace system for 30min. Table 1 lists the sample ID and conditions.

The X-ray photoelectron spectroscopy (XPS) was used to analysis the binding energy of Ta-Pt alloy. The Auger electron spectroscopy (AES) was used to detect the depth distribution of atomic composition of the alloy. The X-ray diffraction pattern was used to study the phase of the alloy. The secondary ion mass spectrometer (SIMS) was used to detect the distribution of implanted impurities before and after implantation. The flat band voltage (V_{fb}) was extracted from the C-V curves measured by Algient 4284 at 100 KHz. [24]

3-3 Results and Discussions

3-3-1 Thermal stability of the Ta-Pt alloy

The electron binding energies of oxygen (O) and tantalum (Ta) atoms were detected by

the XPS for the A1 samples with Ta-Pt (6nm)/SiO_2 (6nm)/Si structure. Figures 1(a) and 1(b) show the XPS spectra of O and Ta atoms, respectively. At the sample surface, the binding energy of 1s orbit of O atom is 531eV and that of $4f_{7/2}$ orbit of Ta atom shifts 1-2eV from that of the bulk Ta-Pt alloy and becomes 23eV, while the pure Ta would reveal $4f_{7/2}$ orbit signal at 21.5-22 eV. The large shift of Ta $4f_{7/2}$ orbit signal reflects a Ta-O bond. After short surface-sputtering periods of 100sec, 200sec, and so on, no obvious oxygen-related peaks are observed, and the peak of Ta atom is still at 23eV which comes from the Ta-Pt alloys. As seen in the 800°C samples, the binding energy of the bulk and interface region of alloy is all the same, and the lack of O 1s orbit signal indicates that the inner of Ta-Pt alloy is almost oxygen free. The Ta-O surface bond is attributed to the reaction of Ta atoms and the residual O_2 molecules in the annealing ambient. The same binding-energy signals of Ta atoms within the alloy for 400 and 800 °C annealed A1 samples are detected as shown in Fig. 2. For any the annealing temperatures, the same binding energy should imply that a stable chemical bond of the alloy. The atomic composition of the Ta-Pt alloy is analyzed by the AES. In Fig.3, AES depth profile shows that the atomic composition of both Ta and Pt of the 400 and 800 °C annealed samples are almost constant, except at the sample surface. The AES signals at the surface are affected by the surface oxidation. Figure 4 shows the X-ray diffraction pattern of the Ta-Pt alloy. The patterns of the samples are almost the same below 700°C, and present the phases of ß-Ta (200) and Pt (100). By 800°C, the phase of Pt (200) is revealed. Regardless of annealing temperatures, the all observed phases belong to tantalum hexagonal crystallite or platinum cubic crystallite. Overall, the same binding energy, uniform composition, and stable micro-crystallite reflect that the Ta-Pt alloy is a highly thermally stable alloy up to 800°C. Furthermore, the absence of the phases of metal oxides and binding energy shift of tantalum implies that the alloy is also chemically stable on the silicon dioxide films.

3-3-2 Work function effect of the impurity incorporation

The work function effect of III or V impurity incorporation of the alloy is investigated by the flat band voltage (V_{fb}) change. The V_{fb} is $V_{fb} = \Phi_{ms} - \frac{Q_{eff}}{C_{ox}}$, where F_{ms} is the work function difference between metal gate and silicon substrate. Q_{eff} and C_{ox} are effective oxide charges and oxide capacitance, respectively. The variation of V_{fb} can reflect the change of work function of metal gate as the amount of oxide charge is constant and the silicon substrate is the same for test samples, the samples fabricated with the same processes and materials assuming that Q_{eff} is also the same. Figure 5 shows the flat band voltage difference (? V_{fb})

versus implantation conditions for 500°C and 800°C annealed samples. The $?V_{fb}$ is the difference of flat band voltage between implanted samples and un-implanted samples. The fabrication processes of those are almost the same, except for the implantation process. In Fig.5 (a) almost all the $?V_{fb}$ of the A2 samples are located at -0.05V, except for the 800°C samples implanted with 25KeV BF_2^+. Under all the implantation conditions, the difference of $?V_{fb}$ is generally less than 0.05V. Furthermore, the difference of the $?V_{fb}$ of all the 500°C and 800°C samples with the same implantation condition is less than 0.02V. The $?V_{fb}$ is almost independent of the implantation condition and annealing temperature. Similarly, Figure 5(b) shows that the $?V_{fb}$ of A3 samples are located approximately at -0.1V for 500°C samples and at -0.05V for 800°C samples. For all of implantation conditions, the difference of the $?V_{fb}$ is generally less than 0.05V. The difference of the $?V_{fb}$ for all the 500°C and 800°C samples with the same implantation conditions is also about 0.05V. Figure 6 shows the impurity depth distribution both before and after annealing A3 samples implanted with 40KeV As^+ or 30KeV BF_2^+. In Fig. 6(a) the depth distribution of arsenic atoms of the before and after annealing A3 samples are almost the same. The abnormal peak signal of Ta comes form the SIMS detection error and it always occurs at the interface between metal gate and silicon dioxide. Compared with the Ta distribution, arsenic is free near the interface between metal gate and silicon dioxide. This presumes that the $?V_{fb}$ should not come from the work function change but mainly from oxide charges since the Ta-Pt alloy is free of impurities at the interface between the metal gate and silicon dioxide. Figure 6(b) shows that the boron impurities are distributed near the surface of the alloy before annealing. Subsequently, boron impurities are redistributed throughout the alloy film after 800°C annealing. In addition, the depth distributions both before and after annealing P^+ implanted samples are also detected and are similar to those of BF_2^+ implanted samples. Although the impurities of boron or phosphorus can be diffused throughout the alloy films at 800°C, the $?V_{fb}$ of both A2 samples and A3 samples are still small. This confirms that the work function of the alloys incorporated with impurities of boron or phosphorus should be almost constant. The C-V characteristics of 800°C A3 samples are shown in Fig. 7. The C-V curves of the As^+ and P^+ implanted samples are smoother than those of the BF_2^+ implanted and un-implanted samples. This confirms that the $?V_{fb}$ should be due to the oxide charge, which might be caused by the sputtering damage and thermal stress. The oxide charges difference are presumably caused by the thermal stress difference between implanted samples and un-implanted samples, since the alloy is thermally stable at 800°C and the implantation process is the main difference. Considering the dosage of implantation impurity, the amount of dosage is 5E15 cm^{-2}, such that the concentration of

impurity could be 8.3E20 cm^{-3} if the distribution of impurities is uniform. The impurity concentration can only cause a ? V_{fb} less than 0.1V, which should be mostly caused by oxide charges. Moreover, the dosage for implantation process of MOSFET fabrication would generally be less than 5E15 cm^{-2} so that the work function variation of the alloy gate affected by the impurities should be much less than 0.1V and could be neglected. In other words, this implies that the alloys are immune to impurities due to implantation.

3-4 Conclusions

The Ta-Pt alloy with tunable work function is a potentially suitable material for metal gates due to its thermal stability and resistance to the impurities. It could be integrated in the conventional MOSFET process, and the work function should not be changed by the incorporation of the implantation impurities of arsenic ions, boron ions and phosphorus ions. Therefore, the control of threshold voltage of the alloy-gate MOSFET could be easier, and not be disturbed by the S/D implantation process.

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Table 3-1. Sample ID and conditions

Sample ID	A1	A2		A3	
Ta target power	DC 100W	DC 30W		DC 20W	
Pt target power	DC 30W	RF 35W		RF 40W	
Implantation	No	Yes	No	Yes	No

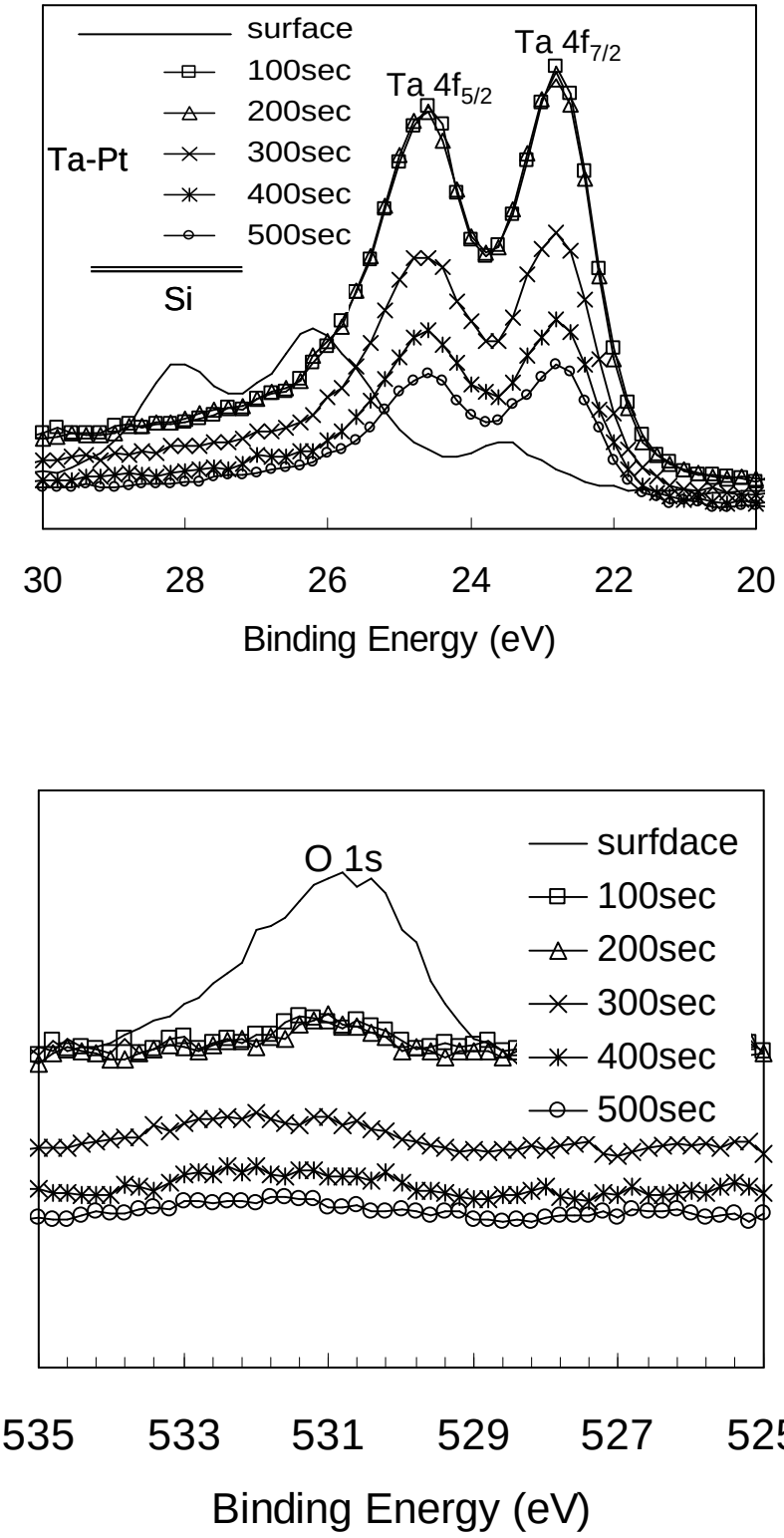


Fig.3-1. The binding energy of (a) O atoms and (b) Ta atoms of the 800 °C annealed samples detected by the XPS after argon (Ar) surface sputtering for various times.

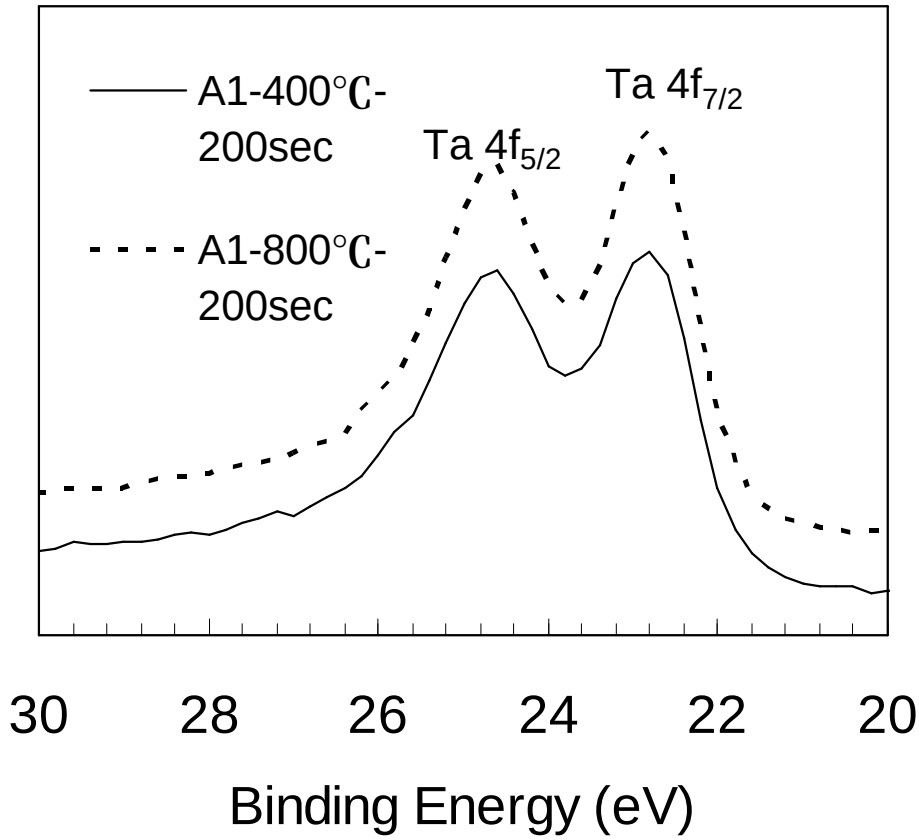


Fig.3-2. The binding energy of Ta atoms of the 400 °C and 800 °C annealed A1 samples detected by XPS after Ar surface sputtering for 200sec.

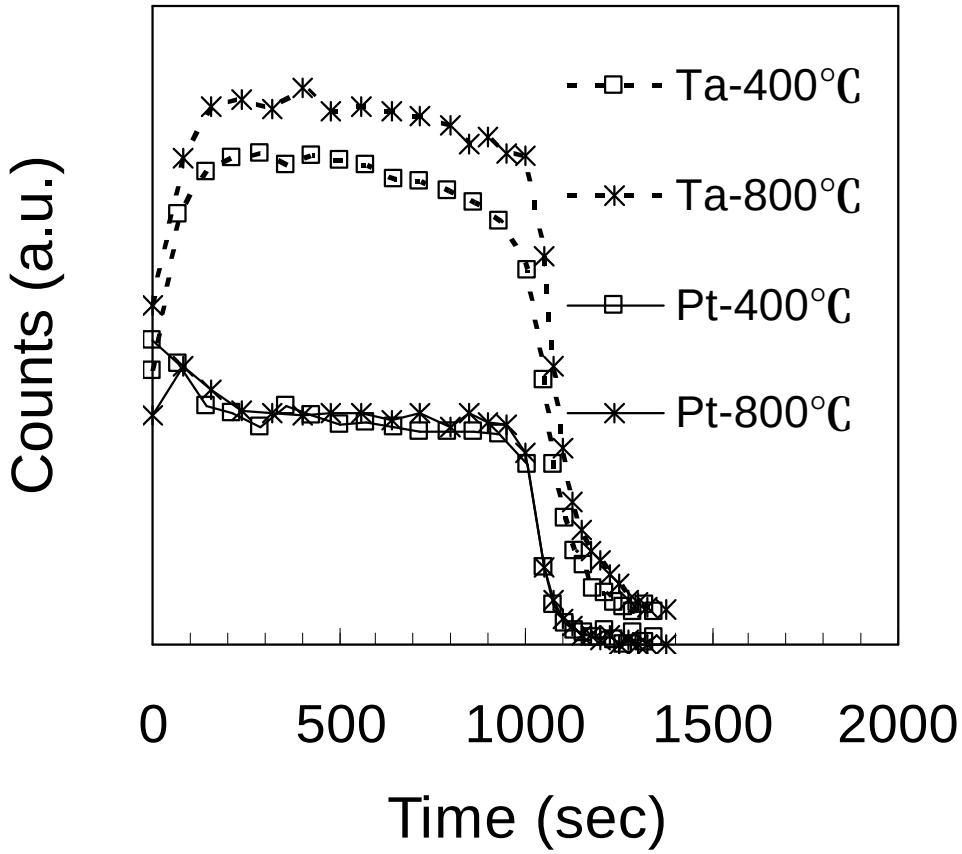


Fig.3-3. Depth distribution of the compositions of the 400 °C and 800 °C annealed A1 samples detected by AES.

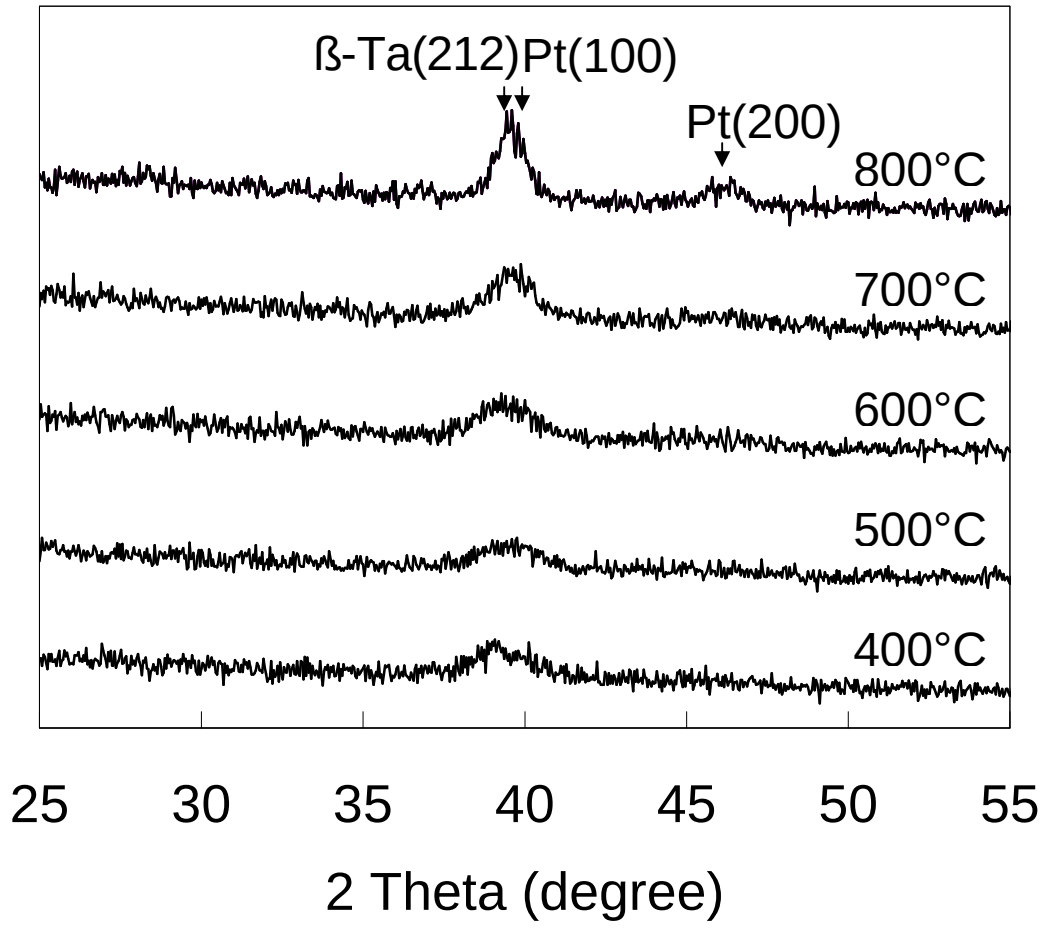


Fig.3-4. X-ray diffraction pattern of the A1 samples after 400°C, 500°C, 600°C, 700°C, and 800°C annealing.

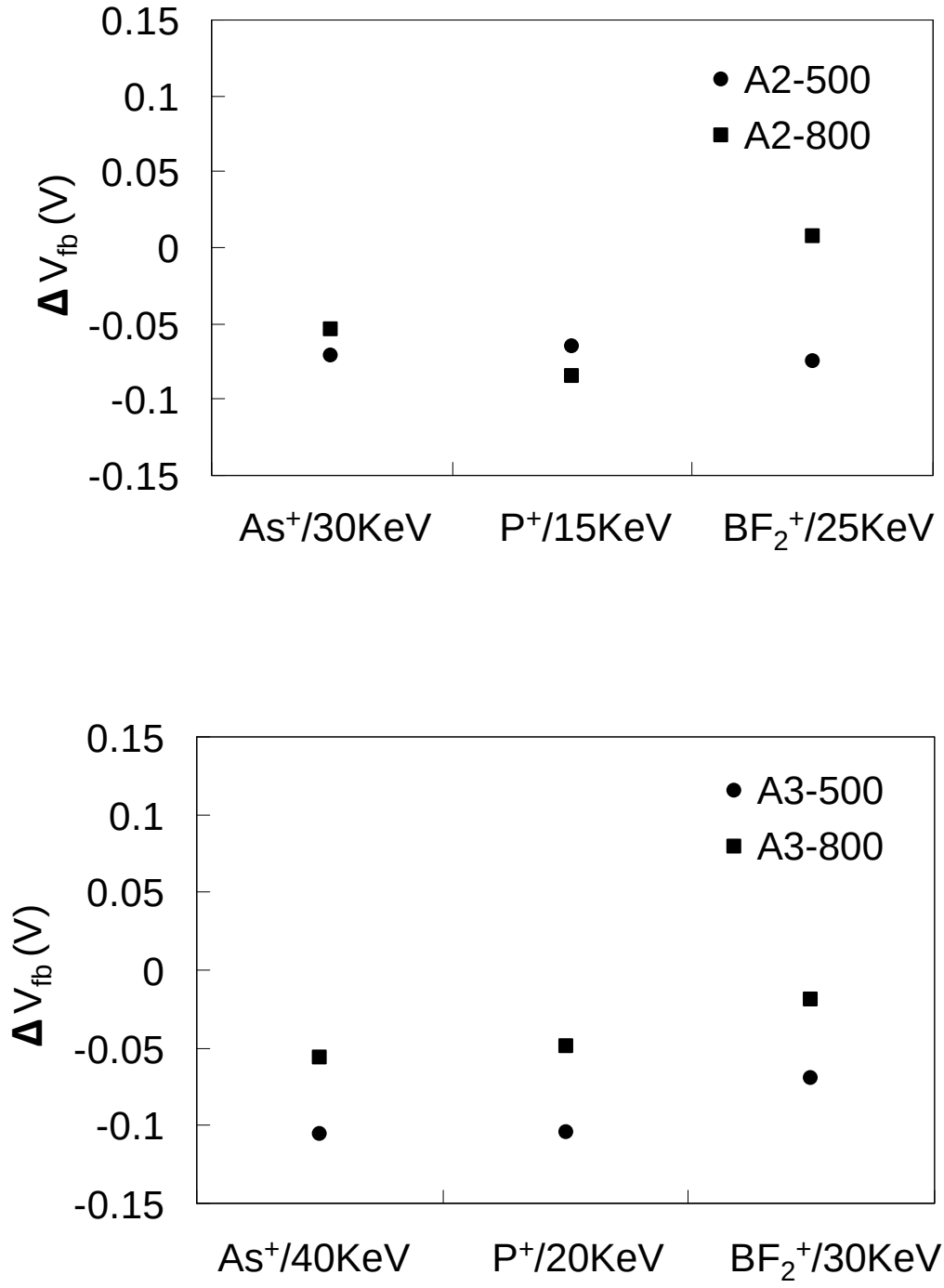
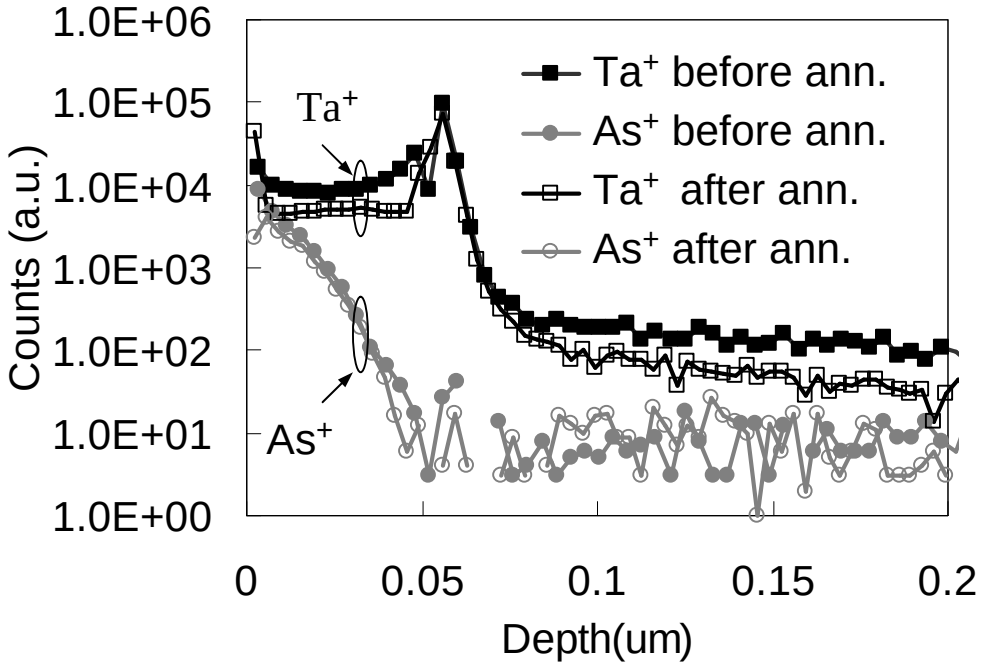


Fig.3-5. The flat-band voltage shift (? V_{fb}) of (a) A2 samples; (b) A3 samples with various implantation conditions after 500°C and 800°C annealing. The ? V_{fb} value is the difference between flat-band voltage of the un-implanted and implanted samples.



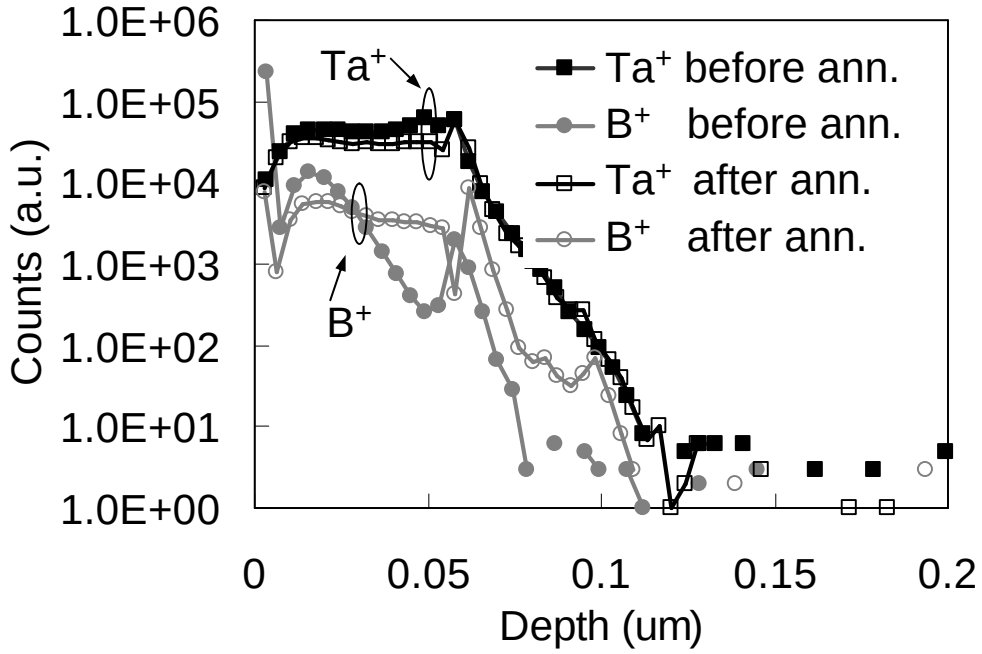


Fig.3-6. The depth distribution before and after 800°C annealing (a) arsenic ; (b) boron of A3 sample detected by SIMS. The energy of implantation values are 50 KeV and 30 KeV for As^+ and BF_2^+, respectively and both dosages are 5E15 cm^{-2}.

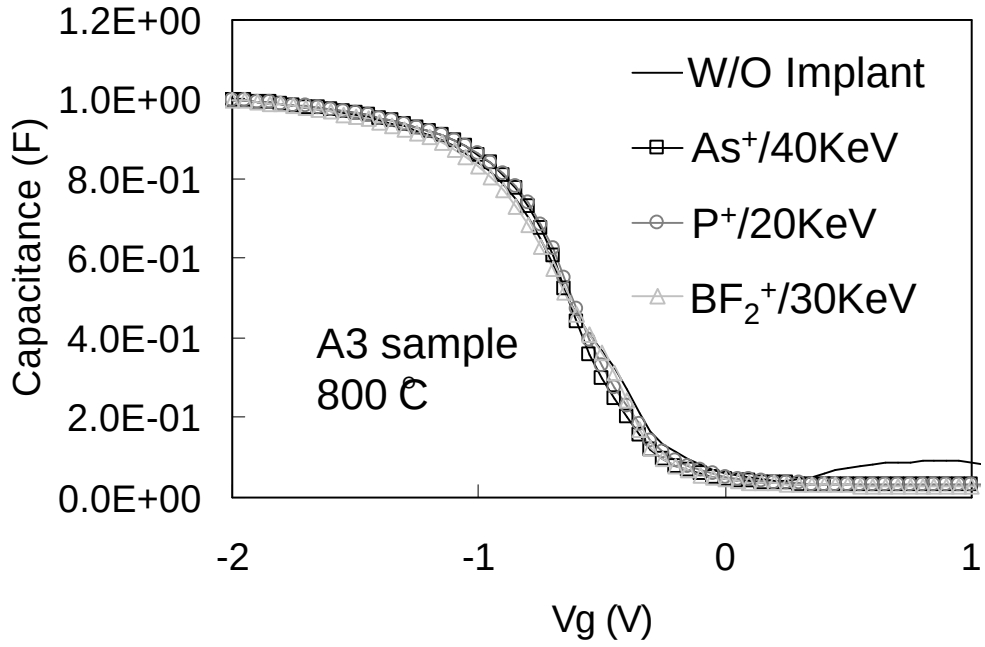


Fig.3-7. C-V characteristic of 800°C annealed A3 samples with and without implantation process.

Chapter 4
Metal Nitride Gate Technology – MoN

4-1 Introduction

Molybdenum nitride (MoN_x) is a material with rigid, inert and corrosion-resistant characteristics [1-5]. This material also has good thermal stability. Such characteristics of MoN_x are very attractive to the applications of semiconductor industry. The work-function of Mo is about 4.6V and possesses large modulation ability (4.2-4.9V) on different dielectrics. Due to the work-function of 4.8V for Mo on SiO_2, this metal can be the metal gate material of PMOS and its work function could be modulated by changing the nitrogen content in MoN_x. Finally, the threshold voltage could also be adjusted by work function modulation.

In this chapter, we discuss the work function modulation and thermal stability of MoN_x with different ratio of nitrogen, and study physical mechanism of MoN_x work-function modulation by physical analysis. Besides, the phenomenon of sputter damage during process would be investigated later.

4-2 Results and Discussion

4-2-1 Physical characteristics of MoN_x

The atomic ratio of MoN_x could be detected by RBS. Fig.4-1 shows the RBS spectrums of MoN_x with three different N/Mo ratios. In order to clearly distinguish the signals of C, N, and Mo, carbon substrate was used as the sample substrate. Resolution of atomic ratio from RBS is about 0.05. Theoretic values of N/Mo atomic ratios for MoN-1, MoN-2, and MoN-3 are 0.85, 1.0, and 1.45, respectively. MoN-0 stands for the pure metal of Mo.

Fig.4-2(a)-(c) were grazing-angle XRD spectrums of MoN-1, MoN-2 and MoN-3 after annealing with various temperature. After 400℃annealing, spectrum of MoN-1 showed peaks of MoN(200) and MoO_3(110). The peak intensity of MoN(200) strongly increased with the annealing temperature, but that of MoO_3(110) relatively decreased. Besides, there was no change of phase and orientation for MoN-1 as the annealing temperature increased. Compared MoN-1 with MoN-2 after 400℃ annealing, peak intensity of MoN(200) become weaker with higher nitrogen ratio. The increase of nitrogen decreased the extent of crystallization and some micro amorphous structure occurred. The binding energy of Mo-N increased and

crystallization enhanced after 600℃ annealing, so MoN(200) peak appeared clearly. For MoN-3 whose nitrogen ration was 20/20, the diffraction peak of MoN(200) come out apparently until 800℃ annealing. The MoO_3(110) peak at $2q = 23.34°$ was signal of surface oxidation during sputtering. Its intensity was very weak and increased slightly with the nitrogen ratio.

The stress of MoN_x after annealing was about 1.2GPa tensile (Fig.4-3). And after the adhesion test of MoN_x film, the crack of Si substrate indicated that MoN_x film had superior adhesion with SiO_2 and HfO_2 dielectrics.

4-2-2 Electrical Analysis of MoN_x

A. Sheet-Resistance Measurement

Fig.4-4(a) was the sheet resistance of as-deposit MoN_x films with different nitrogen content. And Fig.4-4(b) was the sheet resistance with different nitrogen contents and various RTA temperature from 400℃ to 800℃. The resistivity was normalized to the value at 400℃. From Fig.4-4(a) resistance increased apparently as the ratio of Ar/N_2 was larger than 20/10 owing to the apparent increase of nitrogen content in MON_x. And Fig.4-4(b) showed that resistivity decreased with the annealing temperature below 600℃. From XRD data, this could be due to the enhancement of crystallization caused by the increase of annealing temperature. As annealing temperature was higher than 800℃, resistivity abruptly increased without other bonds production and color change. Further study is needed for he fact that samples with over saturated nitrogen showed high resistivity after 700℃ annealing.

B. Sputtering Damage Analysis

As shown in Fig.4-5(a), films deposited with higher power showed larger SiO_2 dielectric leakage current. K. Nakajima described that high energy metal atom during sputtering would bump into the dielectric and caused sputter damage [6]. Compared with the I-V curve [Fig.4-5(b)], it seems that film with higher sputtering power shows severe sputter damage. We deposited films with three different powers upon two kinds of dielectric and investigate films by ICP-MS to find the suitable sputtering power.

Fig.4-6 shows the results of ICP-MS analysis. At sputtering power of 100W the atomic concentration of Mo near SiO_2 surface is close to $10^{20}(atom/cm^3)$ with bombardment depth larger than 2nm. Atomic concentration of oxide surface decreases as sputtering power

decreases. Because the atomic resolution of Mo for ICP-MS is 0.2ppb [$3x10^{17}$(atom/cm^3)], the measured concentration below the resolution is considered lower Mo concentration. The detected concentration is below the resolution at the power of 25W and this means no sputter damage existed on the SiO_2 surface. For HfO_2 dielectric, the surface atomic concentration of Mo is below the resolution. So sputter damage doesn't exist on HfO_2 films. This ability of anti-sputter damage could be due to that HfO_2 has higher density and mass than SiO_2.

Sputtering process would cause damage of SiO_2 in traditional process, and increase leakage current and surface trap charge. But HfO_2 dielectric used in the next generation has the ability of anti-sputter damage. So it's worthy to discuss that if sputtering process could be taken into new transistor process. Of course, further reliability analysis is still needed to be investigated.

C. C-V characteristics and thermal stability of MoN_x

Fig.4-7 (a)-(d) are C-V curves of MoN-0、MoN-1、MoN-2 and MoN-3 deposited on 40nm SiO_2 versus various different annealing temperature. Each C-V curve was averaged by measuring at least 10 capacitances. MoN-0 which was capacitance with pure Mo metal gate was very stable and not affected by annealing temperature (Fig.4-7). Slight distortion in accumulation mode was observed for MoN-1 which annealing below 600℃ and this was probably due to the increase of sputter damage induced interface trap. After 600℃ annealing, these interface traps were recovered. Then the measured CV curve was more normal.

The CV curves of MoN-2 after 400℃ and 500℃ annealing had slight flat-band voltage shift of about 0.1V. From XRD spectrums, this could be due to the different crystallization extent of MoN_x. The flat-band voltage shift was only about 40mV when annealing temperature was higher than 500℃. This was due to that the crystallization reached stable. The slight distortion like MoN-1 was happened when annealing temperature was lower than 600℃, and this situation could be improved by high temperature annealing. The CV curve of MoN-3 showed that the shift of CV curve was not obvious as increasing annealing temperature. According to XRD analysis results, it would have obviously crystallization as annealing temperature was up to 800℃.

Fig.4-8 showed the flat-band voltage shifts compared with that of 400℃ versus different temperatures. All V_{fb} shifts are small except that of MoN-2. CV curves of MoN_x films deposited on HfO_2 were shown in Fig.4-9(a)-(d). There was no apparent shift observed. The distortion of slight increase at accumulation mode might be the larger interfacial trap density

between HfO_2 and SiO_2. Fig.4-10 was the plot of flat-band voltage shifts compared with that of 400℃. The V_{fb} shift of MoN_x on HfO_2 was very stable with annealing temperature (Fig.4-10). From above we could know that MoN_x film has a good thermal stability whether on SiO_2 or on HfO_2 dielectrics.

D. Work-Function Modulation of MoN_x

For the sample of 500℃ annealing, the curve of average V_{fb} versus capacitance effective thickness (CET) with various SiO_2 thickness was shown in Fig.4-11 and Fig.4-12 was curve of V_{fb} versus CET with various SiO_2 thickness for HfO_2/SiO_2 structure. From Fig.4-11, the slopes of MoN-0, MoN-1, MoN-2 and MoN-3 are nearly parallel and conform to constant total charge. When ratio of nitrogen flow rate increases, CV curves shift rightward and V_{fb} shift upward. And it seems to get saturate when the ratio is over 20/10, thus V_{fb} of MoN-3 is a bit higher than that of MoN-2. The slopes of CV curve for MoN-2 and MoN-3 from Fig.4-12 are different from two others. H. Kattelus stated that nitrogen could release the stress of MoN, lower interfacial trap density and get larger slope [7]. The shift of CV curves seems to get affected by saturation of nitrogen and tends to a constant value finally. Compared Fig.4-11 with Fig.4-12, the latter get 0.3V higher V_{fb} than the former.

The work function could be extracted from V_{fb} of different oxide thickness. Fig.4-13 and Fig.4-14 are figures of work function versus different thickness of SiO_2 and HfO_2/SiO_2 with different annealing temperature, respectively. The V_{fb} of each thickness of the same annealing temperature was taken the average of several values. From Fig.4-13, the work functions of MoN-0, MoN-1, MoN-2 and MoN-3 at 500℃ annealing were 4.6V, 4.97V, 5.03V and 5.11V respectively. The work function increases with the ratio of nitrogen flow rate, and finally saturates to a constant value until the ratio of flow rate larger than 20/10. The modulation of work function changes from 4.97V to 5.11V as the ratio of N/Mo is from 0.85 to 1.45. Range of modulation is 0.14V. Besides, work function slightly increases about 40mV with annealing temperature. This is due to the higher crystallization structure of MoN_x from the prior results of XRD and CV analysis.

For structure of HfO_2/SiO_2 stack, work functions of MoN-0, MoN-1, MoN-2 and MoN-3 have a value about 4.89V, 5.31V, 5.41V and 5.37V respectively. These values are higher than those of SiO_2. The work function tends to a constant value as nitrogen saturates. The modulation range is 0.1V which is from 5.31V to 5.41V as the ratio of N/Mo ranges from 0.85 to 1.45.

It's worthy to discuss that the work function of MoN_x on HfO_2 is 0.3V higher than that on SiO_2. The Fermi level pinning caused by dipole layer screening effect of High-κ materials like HfO_2 limits metal work function to the mid-gap of Si. Then work function of metal gate on P substrate should reduce. But our results didn't fit the fact. From the comparison of MoN-0 and MoN-3, the difference was independent of the kinds of oxide dielectric. So MoN on HfO_2 dielectric should have no problem about Fermi level pinning.

$$f_{ms}' = f_{ms} - \frac{1}{e_{ox}} EOT1 * Q_{it,High-k} \qquad (4\text{-}1)$$

The difference of 0.3V might come from the methods of work function extraction. The assumptions are HfO_2/SiO_2 interfacial trap density of $5*10^{12}cm^{-2}$ and very thin HfO_2 thickness. But actually the trap density is higher than that of our assumption. According to Eq 4-1, R. Jha presented that $Q_{it\ High-?}$ is negative when $Q_{it\ SiO2}$ is positive [8]. When work function is -0.3V and ? value is 5, the value of $Q_{it\ High-?}$ equals $1.65*10^{13}cm^{-2}$, higher than the value of our assumption.

4-3 Summary and Conclusions

We investigated characteristics of MoN_x like thermal stability and work function modulation with different ratio of nitrogen. Then we understood the physical mechanism of work function modulation by physical analysis. According to the analysis of RBS, the ratios of N/Mo of MoN_x are 0.85, 1.0 and 1.45. Several important characteristics are described below:

1. The main phase and orientation of MoN-1, MoN-2 and MoN-3 is MoN(200). As the raise of N/Mo ratio, amorphous phase occurs and resistivity becomes higher. The phase and orientation remains with the increase of annealing temperature, and crystallization becomes enhance obviously.
2. High-? HfO_2 with metal gate has highly resistance to sputter damage and doesn't react with MoN_x.
3. MoN_x film shows good thermal stability on SiO_2 or HfO_2.
4. Work function increases with ratio of nitrogen flow rate. Until the ratio of N/Mo is larger than 0.5, MoN_x would tend to saturate and its work function tend to a constant value. The range of work function modulation is about 0.1V with the N/Mo ratio range from 0.85 to 1.45. Besides, the work function increases slightly about 40mV as the annealing temperature increases.

The modulation range of work function can be up to 0.4V from pure Mo to MoN of N/Mo ratio 1.57 and this would be useful for threshold voltage adjustment. In aspect of process temperature, the nitrogen can't be too much and saturates in order to avoid the affect of thermal stability. The over high sheet resistance seems to be the common problem of nitride and this could be the limiting condition for metal nitride to be the candidate of metal gate. This situation of high resistivity could be solved by stack another layer of low resistance metal upon metal nitride to reduce the sheet resistance.

Besides, Fermi level pinning effect was found for the metal gate on HfO_2 dielectric and moved the Fermi level toward the mid-gap of Si. Then Fermi level would be pinned there. This effect caused that the needed value of work function would be larger than theoretical value. But from our work (Fig.4-13 and Fig.4-14), difference of work functions between MoN-0 and MoN-3 on SiO_2 and HfO_2 doesn't get affected by oxide layer. So Fermi level pinning effect seems not happen. This situation should be worthy to notice.

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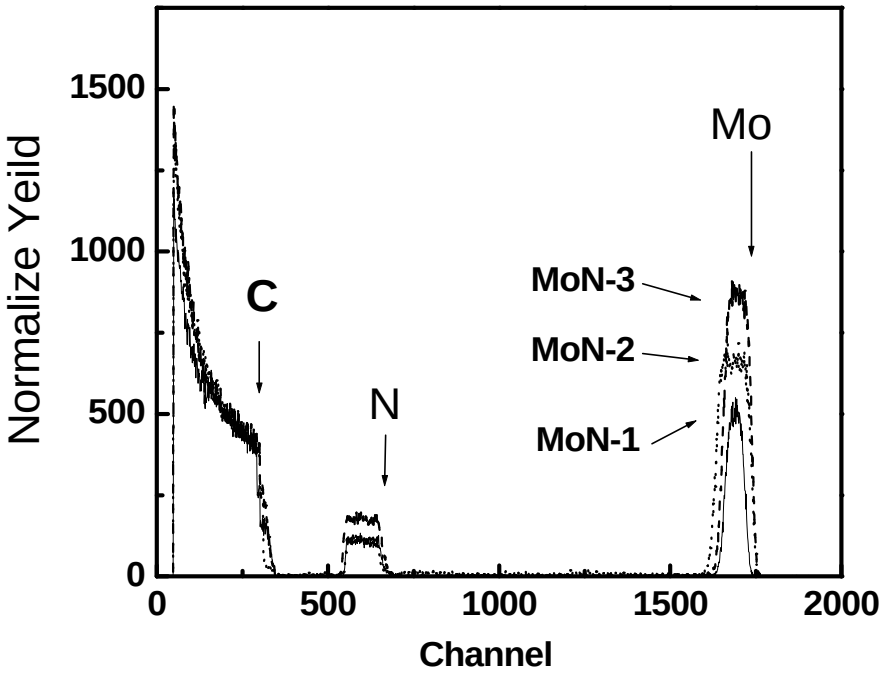
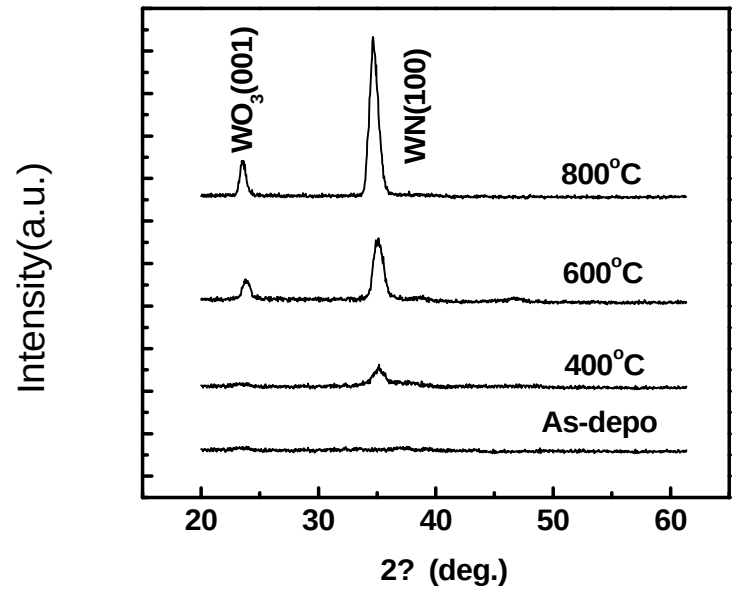
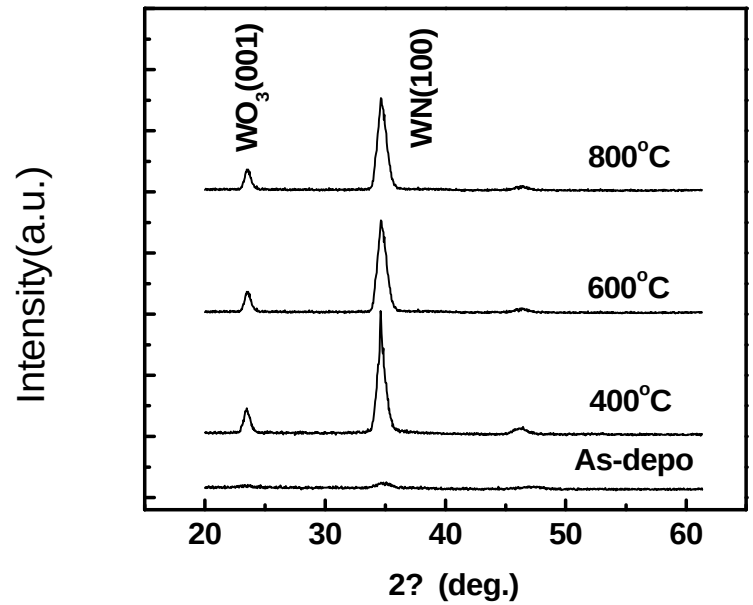


Fig.4-1. RBS spectrum of MoN_x on carbon substrate.

Ratio of Ar/N_2 flow rate: MoN-1=20/5, MoN-2=20/10, MoN-3=20/20

Ratio of N/Mo: MoN-1=0.85, MoN-2=1.0, MoN-3=1.45


Intensity(a.u.)
WO3(001)
WN(100)
800°C
600°C
400°C
As-depo
20
30
40
50
60
2? (deg.)


Intensity(a.u.)
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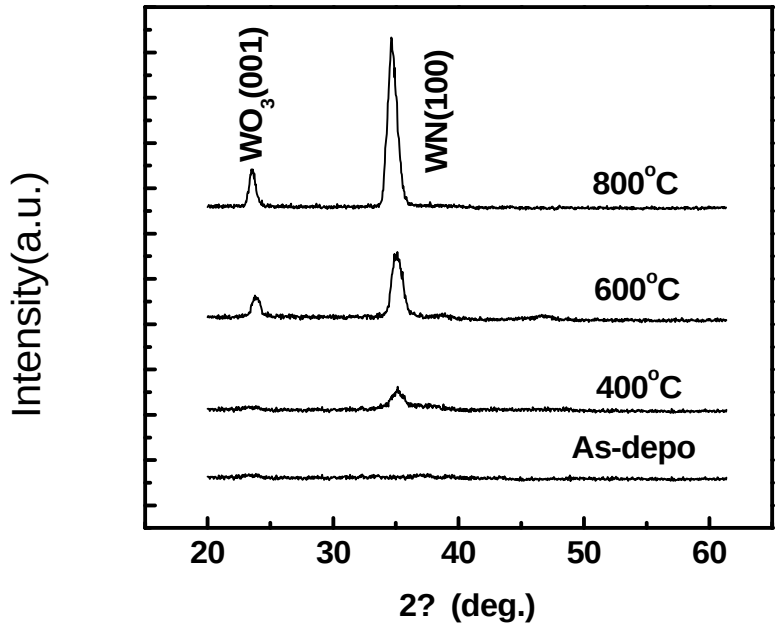


Fig.4-2. (a) XRD spectrum of MoN-1 with different annealing temperature. (b) XRD spectrum of MoN-2 with different annealing temperature. (c) XRD spectrum of MoN-3 with different annealing temperature

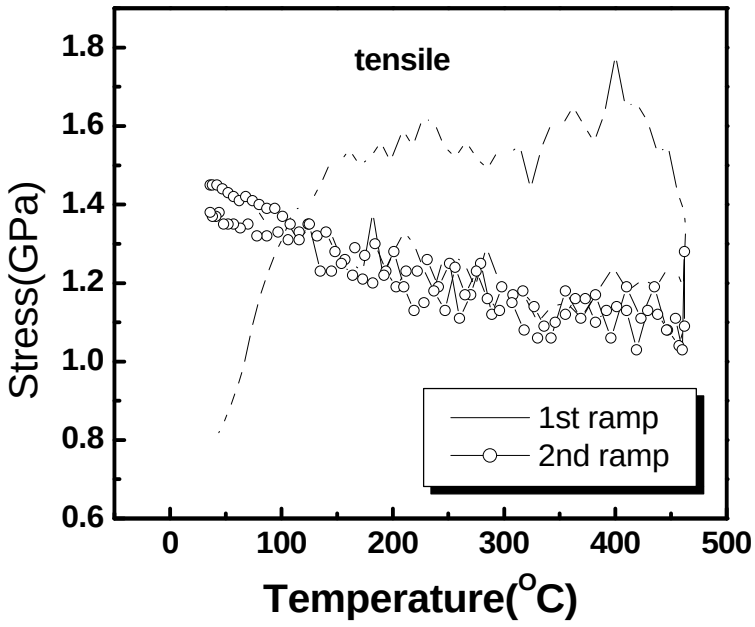
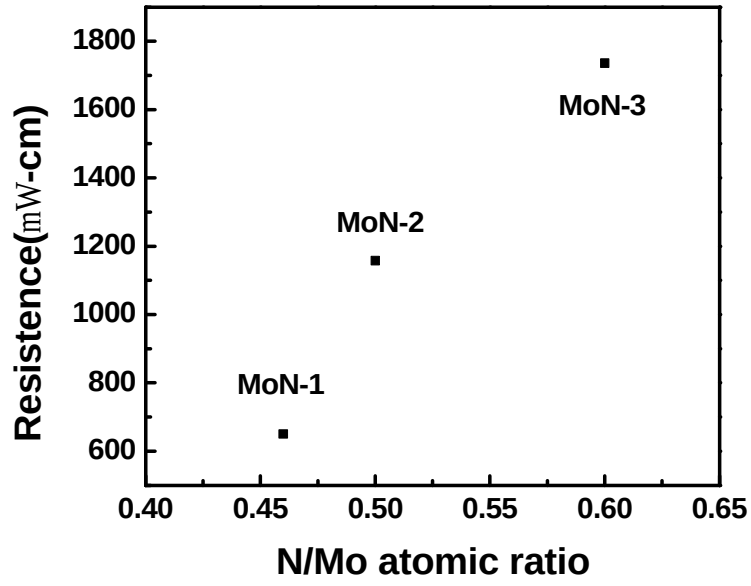


Fig.4-3. Film stress of MoN-2 versus temperature.



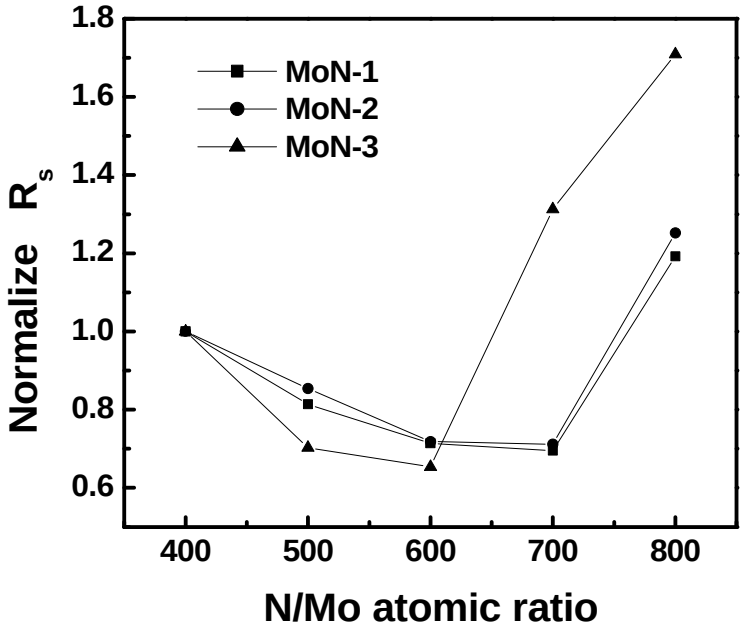
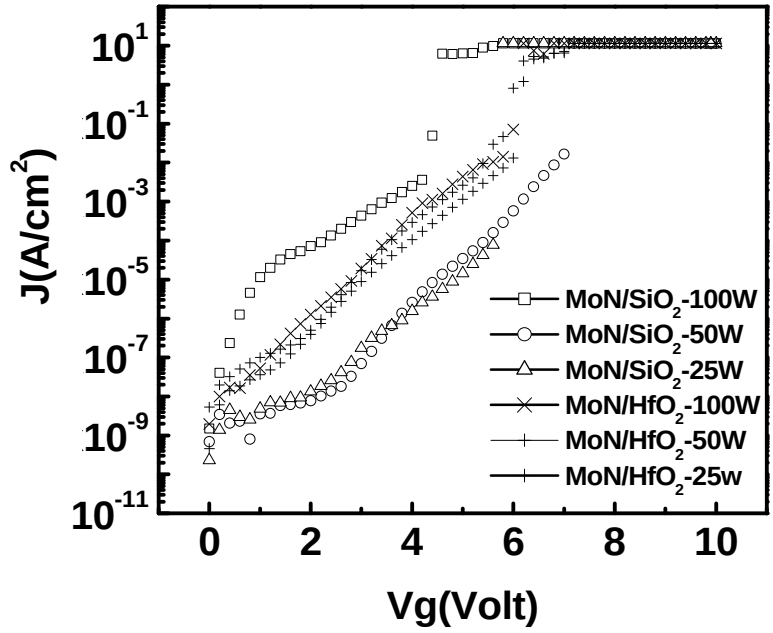


Fig.4-4. (a) Sheet resistance of as-deposit 60nm MoN_x film and (b) sheet resistance of the 60nm MoN_x after annealing at different temperatures.



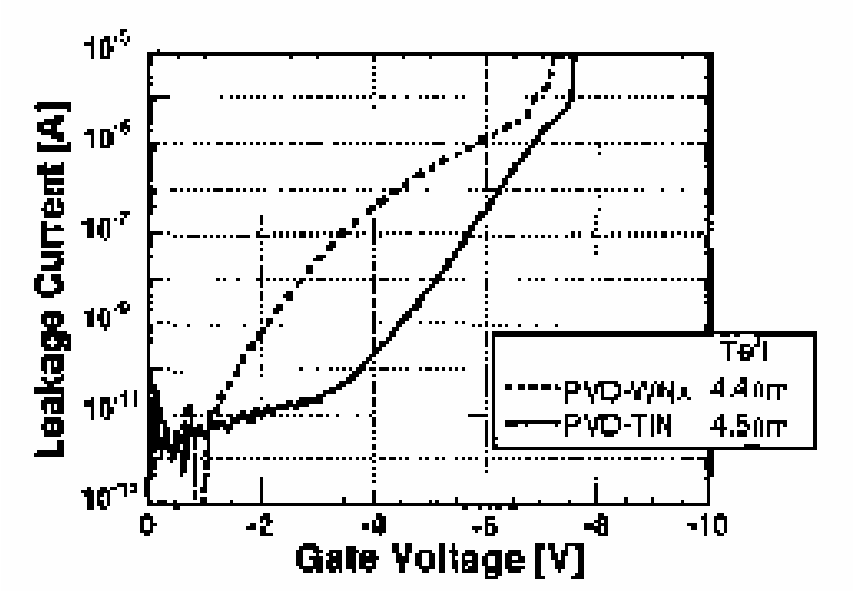
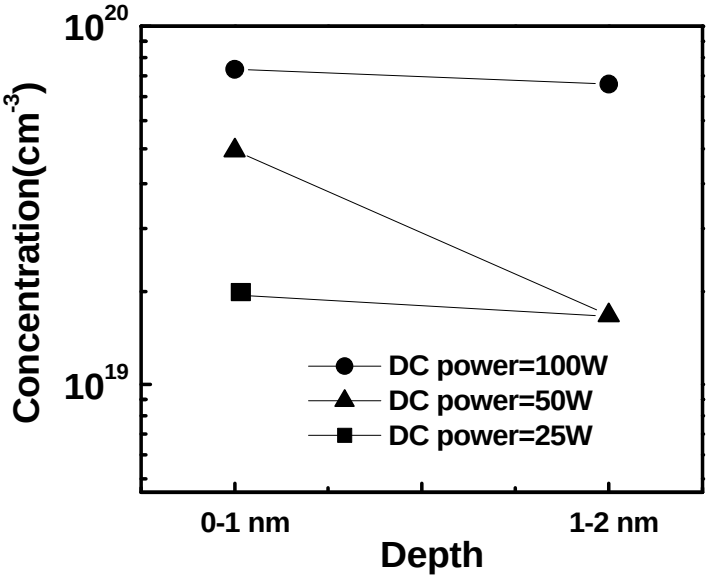


Fig.4-5. (a) I-V curve of different sample structures of our work and (b) I-V curve of sputter damage from literatures.



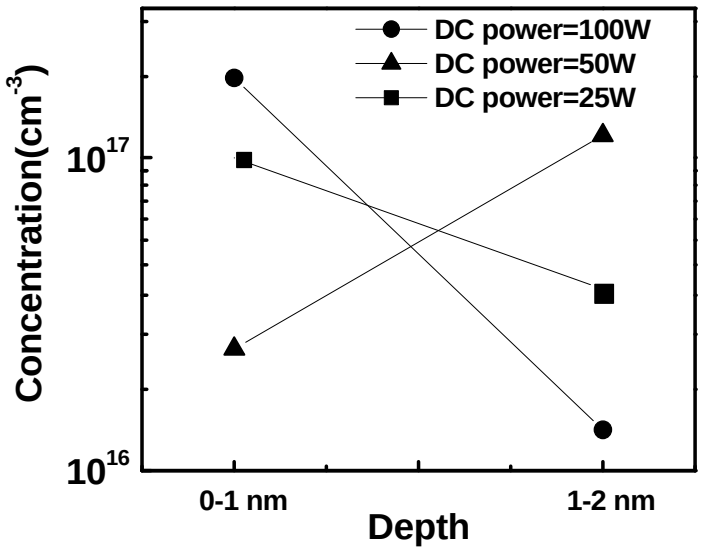


Fig.4-6. (a) ICP-MS plot of MoN/SiO_2 structure. The surface concentration of $10^{20}(cm^{-3})$ means that sputter damage exists. (b) ICP-MS plot of MoN/HfO_2 structure. The surface concentration is below the resolution value. This means that sputter damage doesn't exist. The resolution of ICP-MS is $3*10^{17}(cm^{-3})$.

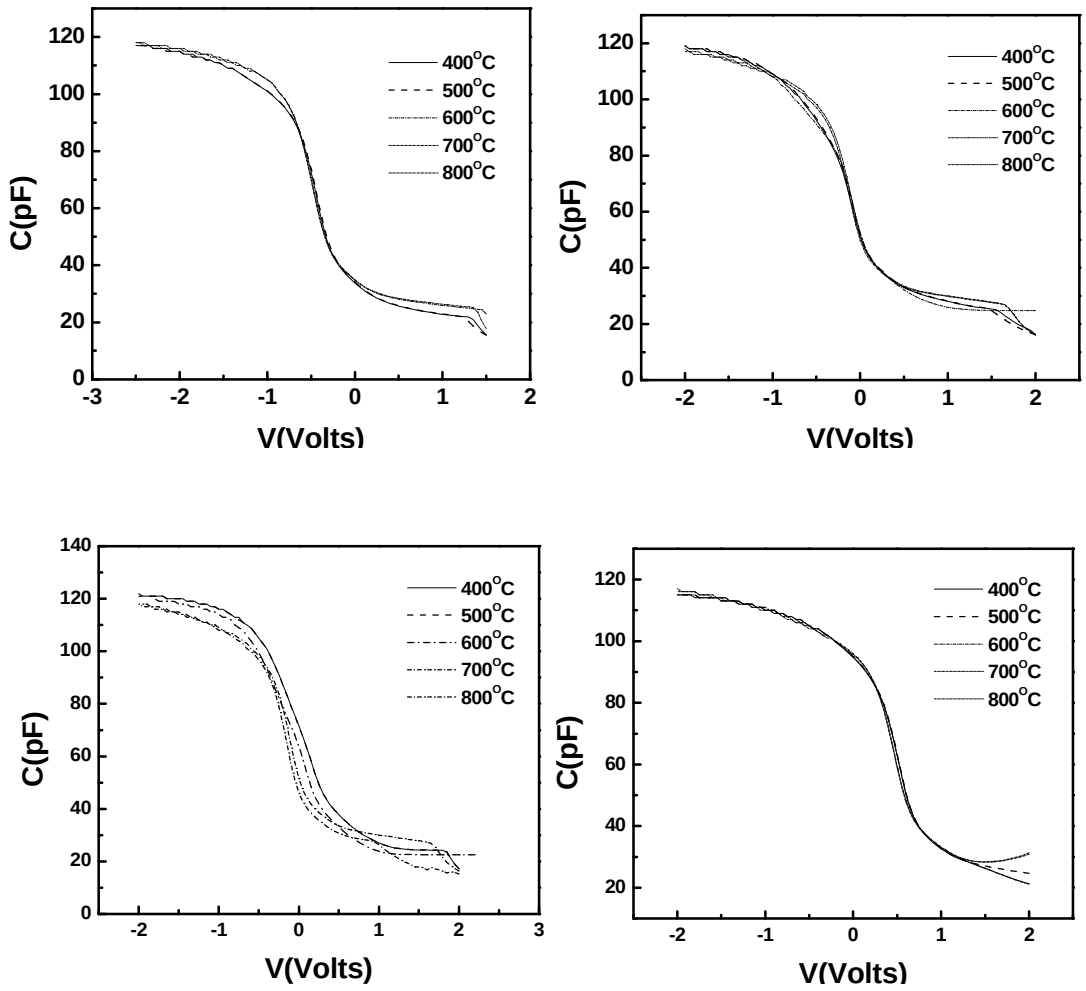


Fig.4-7. CV curves of MoN_x/SiO_2 versus various annealing temperatures.
(a)MoN-0; (b)MoN-1; (c)MoN-2; (d)MoN-3.

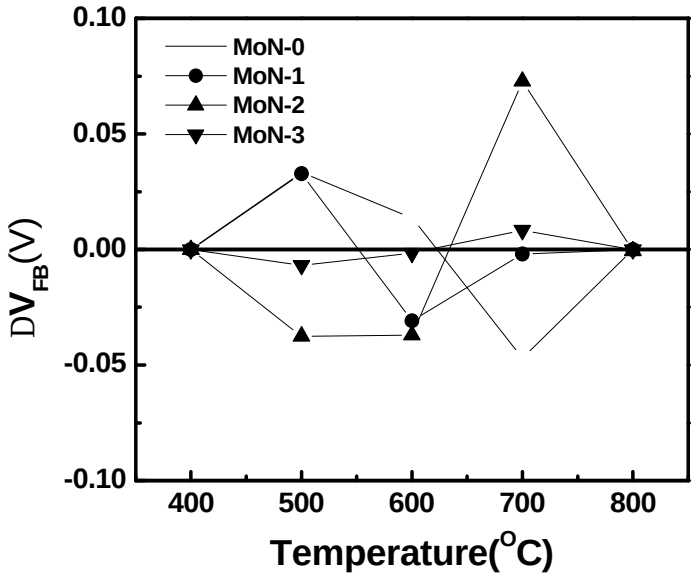


Fig.4-8. Flat band difference of MoN/SiO_2 versus different annealing temperatures

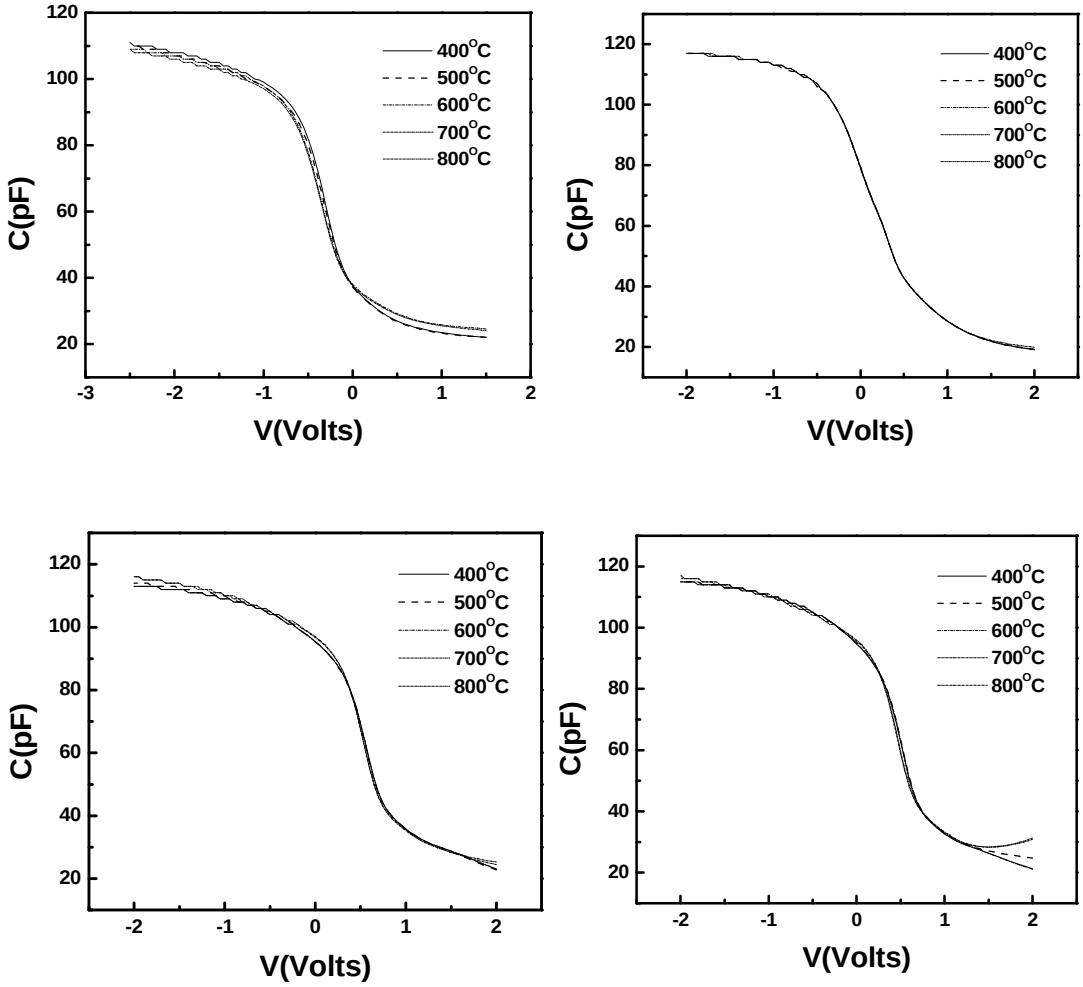


Fig.4-9. CV curves of Mo/ HfO_2(5nm)/SiO_2 (40nm) versus different annealing temperatures. (a)MoN-0; (b)MoN-1; (c)MoN-2; (d)MoN-3.

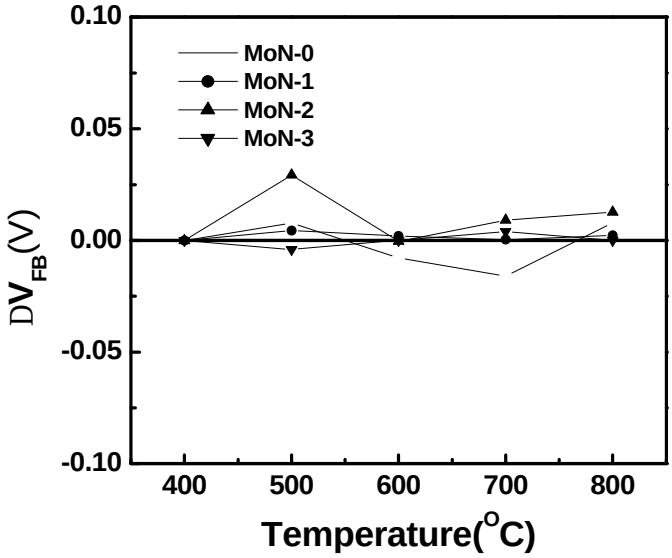


Fig.4-10. Flat band difference of MoN_x/ HfO_2(5nm)/SiO_2(40nm) versus different annealing temperatures.

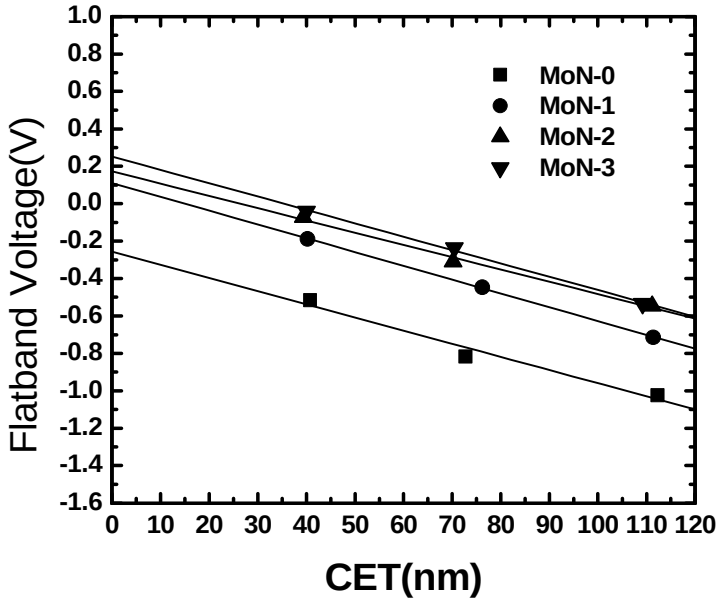


Fig.4-11. MoN_x/SiO_2 flat band voltage of different thickness.

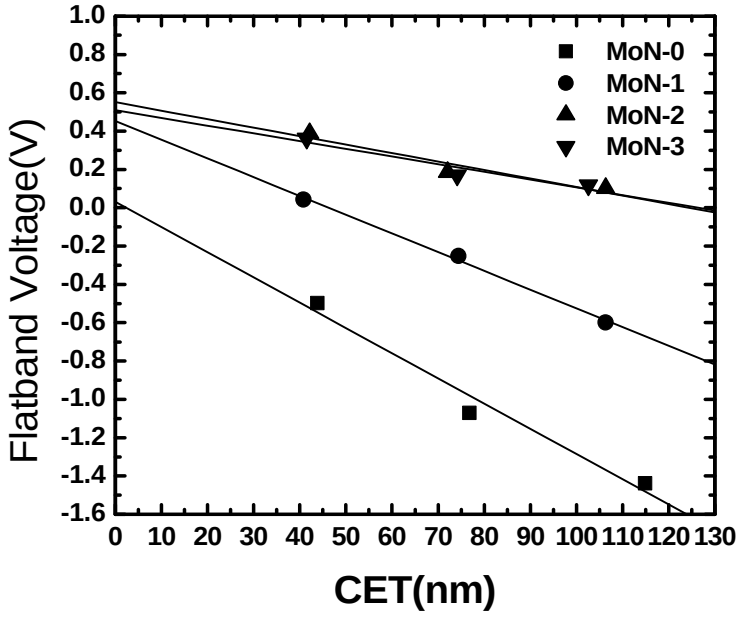


Fig.4-12. MoN_x/ HfO_2(5nm)/SiO_2 flat band voltage of different thickness.

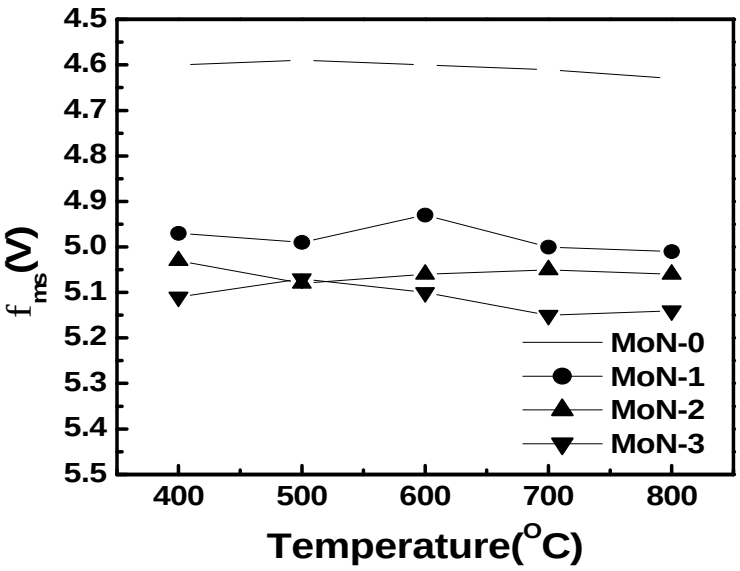


Fig.4-13. MoN_x/ SiO_2 Work function of MoN_x versus temperature.

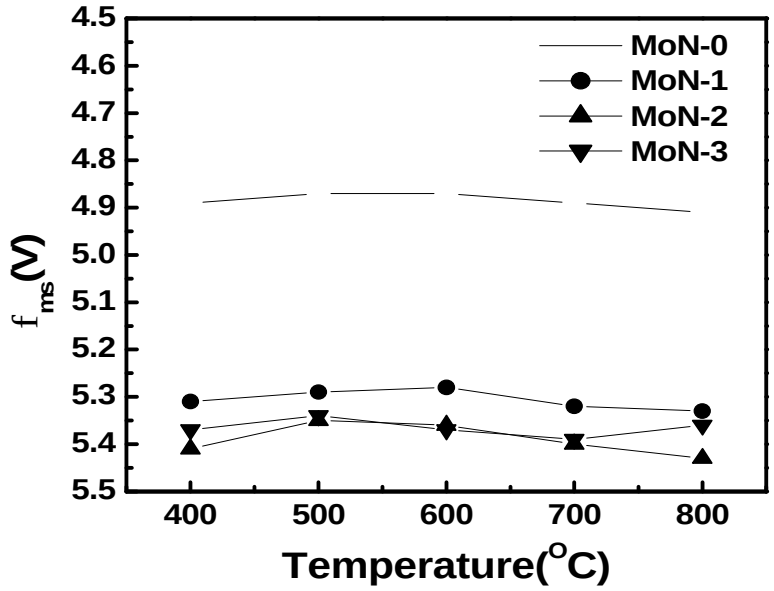


Fig.4-14. MoN_x/ HfO_2(5nm)/SiO_2 work function of MoN_x versus temperature.

Chapter 5
Metal Nitride Gate Technology - WN

5-1 Introduction

For the candidates of metal gate material, WN_x is also another potential material [1]. The characteristics of WN_x contains being tough, chemical inert and corrosion-resistant. WN_x has the characteristics of superior thermal stability, high melting point and work function near mid-gap about 4.55-4.75V. In this work, nitrogen was incorporated during sputtering and work function WN_x could be adjusted by adjusting nitrogen content.

In this chapter we discuss the work function modulation and thermal stability of WN_x with various nitrogen ratios and study the change of phase and orientation of WN_x after annealing. Further, we hope to explain the physical mechanism of work function modulation. The effective work function, thermal stability and adhesion of WN_x on HfO_2 dielectric are also topics of this work. Besides, outgas effect of WN_x was also found.

5-2 Results and Discussion

5-2-1 Physical Characteristics of WN_x

The atomic ratio of WN_x could be detected by RBS. Fig.5-1 shows the RBS spectrums of WN_x with three different N/W ratios. In order to clearly distinguish the signals of C, N, and Mo, carbon substrate was used as the sample substrate. Resolution of atomic ratio from RBS is about 0.05. Theoretic values of N/W atomic ratios for WN-1, WN-2, and WN-3 are 0.8, 1.26, and 1.57, respectively. MoN-0 stands for the pure metal of tungsten.

Fig.4-2 (a)-(c) were grazing- angle XRD spectrums of WN-1, WN-2 and WN-3 after annealing with various temperature. WN-1 without annealing showed unapparent diffraction peak of WN(100). This weak X-ray diffraction signal meant that the film didn’t have long-term crystal arrange After 400℃ annealing, the signals from XRD remained unchanged, and peak of WN(100) showed very obviously until the annealing temperature reached 600℃. This revealed that amorphous WN(100) come regular arrange of crystal space. Besides, obviously enhanced WO_3(001) and very weak WO_3(002) peak were found at 2?=23.14？and 47.26？respectively. These peaks might be due to the trace of oxygen atom in chamber during sputtering. T. G. Shen had mentioned that oxygen in WN_x would move to surface and form

tungsten oxide [2].

Peak intensity of WN(100) and WO_3(001) remained unchanged after 800℃ annealing. For WN-2 without annealing, peak of WN(100) is similar to WN-1. After 400℃ annealing, WN(100) peak was obvious. From RBS spectrums, we could know that it could be due to that N/W ratio of 1.26 for WN-2 is larger than that of 0.8 for WN-1. More nitrogen atoms could be supplied to bonding with tungsten. As the annealing temperature reached 600℃, WN(100) peak intensity become slightly higher and 2?(=35.24？) was also a little smaller than that of WN-1 (2?=35.84？). The situation of lattice constant expansion could happen [3].

N/W ratio should be about 1 for WN-1 but the ratio the ratio becomes 1.26 for WN-2. We supposed that too much nitrogen filled between lattices and caused the expansion of lattice constant. Similarly WN(100) peak remained unchanged as the annealing temperature was up to 800℃. From Fig.4-2(c) WN(100) signal was hardly detected for WN-3 without annealing , and this meant the weak W-N bond. According to the research of K. J. Huber, much nitrogen atoms among WN_x would cause the increase of W-N bonding energy, so it would be difficult to form WN crystal [4].

WN(100) peak was weaker after 400℃ annealing. For the same reason, the peak of WN(100) after 600℃ annealing was smaller than that peak for WN-2. The intensity would be the same as that of WN-2 until annealing temperature of 800℃.

From the XRD analysis above, we can find that overdose of nitrogen was filled the site outside the lattice. The bonding of WN could also be affected by nitrogen concentration and annealing temperature. The intensity of WN and WO_3 peaks remained constant when the annealing temperature reached 800℃. This means that oxidation didn’t happen during annealing. This situation is different from that of MoN_x.

WN_x without annealing shows compressive stress (Fig.4-3) and this compressive stress of WN_x could decrease slowly to the value of -0.2Gpa. So the annealing process could release the compressive stress and this is helpful to decrease the density of interfacial trap charge.

In the adhesion test, the results are the same as those of MoN_x. The crack of Si substrate indicated that WN_x film had superior adhesion with SiO_2 and HfO_2 dielectrics.

5-2-2 Outgas Effect of WN_x

Rapid thermal anneal (RTA) and furnace thermal anneal are two common annealing processes. When we annealed WN_x with RTA, there were bubbles found on the surface of WN_x film. Fig.5-4 was SEM photos of bubbles and the bubbles were getting more with the

increasing annealing temperature. Although mist might be the cause of bubbles, the sputtering films were deposited at high vacuum and so mist couldn't exist.

When annealing temperature got higher, the range of regular crystal for WN_x became wider from XRD analysis. We assumed that these bubbles could be nitrogen come from WN_x during annealing. And the metal films could crack due to the rapid outgassing rate of nitrogen.

TDS was used to detect the components of released gas from WN_x. From Fig.5-5(a) the background ion current of nitrogen was about 10^{-11}(A) in Ar environment. After the temperature was raised to 800℃ and maintained for 10minutes, the ion current of nitrogen enhanced with the temperature while that of oxygen and water unchanged with temperature.(Fig.5-5(b)) So we found out that the cause of bubbles was the nitrogen released from WN_x. We also found that there were no cracks for WN_x films with furnace annealing from the SEM photos. This could be due to that nitrogen could slowly diffuse out the sample when the temperature rising was slowly. While the rising rate of temperature was too fast, the released nitrogen couldn't have enough time to diffuse out the sample and then formed the bubbles. Thus in the proceeding experiments, we performed furnace annealing for WN_x instead of RTA for MoN_x in order to avoid the bubbles.

5-2-3 Electrical Characteristics of WNx

A. Sheet Resistance Measurement

Fig.5-6(a) shows the sheet resistance of as-deposit WN_x films with various nitrogen contents. And Fig.5-6 (b) is sheet resistance with different nitrogen content and various annealing temperature from 400℃ to 800℃. The resistivity is normalized by that of 400℃.

Resistivity of all the samples without annealing from Fig.5-6(a) is very high and it's due to that high-resist (1000-4500 $m\Omega - cm$) phase WN(100) was the main phase of un-annealing WN_x [4]. Resistivity increases with the increase of nitrogen atoms filled among the lattice. When the annealing temperature was below 600℃, crystallization enhanced with the increase of annealing temperature, then resistivity had the trend of decrease. As the annealing temperature was higher than 600℃, nitrogen was released from W_XN and reisistivity lowers to a constant value finally.

B. C-V Curves and Thermal Stability of WN

Fig.5-7 is C-V curves of WN-0、WN-1、WN-2 and WN-3 deposited on 30nm SiO_2

versus various different annealing temperatures. Each C-V curve was measured and averaged by at least 10 capacitances. Fig.5.8 is the plot of flat-band voltage derived from the CV curves of Fig.5-7 versus temperature. The flat-band voltage is normalized to that of 400℃. WN-0 sample which is the pure tungsten metal was very stable with the annealing temperature. The deviation of CV curve for WN-1 is about between 0.1V from 400℃ to 800℃ annealing. Slightly distortion was found at 400℃and 500℃ annealing for WN-2 and WN-3, and this could be due to much nitrogen induced expansion of lattice constant.

Flat band voltage shift was related to the concentration of nitrogen. We could divide the flat-band voltage shifts of Fig.5-8 into two groups with WN-0~1 and WN-2~3. And this shift was improved after 600℃ annealing. Besides, CV shifted to the right and this meant negative charge existed in the interface as anneal temperature increased. This effect conflicted with the fact that the charge induced by the stress should be positive charge and the compressive stress would decrease after annealing. We supposed that Si-N bond formed in the interface of SiO_2 and Si, caused negative charge and shifted the CV curve to the right. And this effect would decrease by the separate out of nitrogen with high enough annealing temperature.

Fig.5-9 and Fig.5-10 are CV curves and V_{fb} shifts of WN_x deposited on HfO_2. WN-0 was very stable while the deviations of other samples increased with the increase of nitrogen atoms. The distortion improved after high temperature annealing. From CV data, we knew that the deviation range of WN_x on HfO_2 was smaller and this might be due to the fact that HfO_2 is harder to bond with nitrogen.

C. Work-Function Modulation of WN

For the sample of 600℃ annealing, the curve of average V_{fb} versus capacitance effective thickness (CET) with various SiO_2 thickness was shown in Fig.5-11. Fig.5-12 was the same curve with various thickness of HfO_2/SiO_2 structure. From Fig.5-11, V_{fb} of WN-1 with W/N ratio of 20/5 moved upward about 0.5V than that of WN-0. And V_{fb} moved toward downward as the ratio of nitrogen increased. The trend of HfO_2/SiO_2 structure in Fig.5-12 is almost the same as that of SiO_2 structure.

We extracted the work function of WN_x from V_{fb} and plotted work functions versus various annealing temperature with SiO_2 (Fig.5-13). And Fig.5-13 was the same plot with the structure of HfO_2/SiO_2 stack. At the annealing temperature of 600℃, the work functions of WN-0~3 were about 4.6V, 5.11V, 5.03V and 4.96V respectively, and these values could be divided into two groups . First group was the range of 0.51V from WN-0 to WN-1. That meant an obvious difference of work function exists between pure tungsten metal to WN_x.

The other group was the range from WN-1 to WN-3. This group showed the trend of decreasing work functions with the increase of nitrogen ratio.

From XRD spectrum of 600℃, when the diffraction peak of WN(100) was stronger, the distance to that of WN-0 got longer. Stronger peak of WN(100) stood for the more complete structure of WN_x film. When the film structure was not complete enough, the work function would be relatively small. Peak of WN-1 showed the strongest intensity and the largest deviation. This might be that there was not so much nitrogen to hinder from bonding. The range of modulation was only 0.15V which was from 5.11V to 4.96V with N/W ratio of 0.8 to 1.57 respectively. Besides, work function of 800℃ annealing compared to that of 400℃ increased slightly. According to data of XRD and CV curves, this could be due to the complete structure of WN_x. At high annealing temperature, the outgassing of nitrogen and completeness of bond caused the difference of N/W ratios between all the WN samples to get smaller. And the modulation range of nitrogen got smaller, too.

At the annealing temperature of 600℃, the work functions of WN-0~3 with HfO_2/SiO_2 structure were 4.77V, 5.14V, 5.08V and 4.92V respectively. These values were larger than those of SiO_2 dielectric. For the deviation of work function, it increased only 0.37V which value was 0.14V lower that of SiO_2. Without taking Fermi Pinning effect into consideration, the work function was irrelevant to the dielectric. So the modulation range of WN_x on HfO_2 dielectric was smaller than that on SiO_2 dielectric. This meant that problem of work function limiting exists for WN_x on HfO_2 dielectric. This case is different from the situation of MoN_x. From WN-1 to WN-3, the ratios of nitrogen flow rate increases, and the work function decreases. The modulation range is 0.22V which is from 4.92V to 5.14V with N/W ratio from 0.8 to 1.57.

From the work function modulation of MoN_x, we discovered that high density interfacial trap between HfO_2/SiO_2 interface induced the work function of MoN_x on HfO_2 dielectric 0.3V to be higher than that on SiO_2 dielectric. Because the dielectric for MoN_x and WN_x was deposited at the same time, the interface trap should be the same. But work function of WN_x on HfO_2 was only 0.1V higher than that on SiO_2. This could be proven that due to the effect of Fermi Level Pinning. And the real position of limited Fermi level still was needed to further study.

5-3 Summary and Conclusions

This chapter discussed the thermal stability and work function modulation of WN_x with

various N/W ratios. Physical analysis was also used to instigate the physical mechanism of work function modulation of WN_x. According to the RBS spectrums, the ratios of N/W are 0.8, 1.26 and 1.57. And several important characteristics were described below:

1. The main phase and orientation of WN-1, WN-2 and WN-3 is WN(100). Effect of lattice constant expansion was found in WN-2 and WN-3. As the increasing annealing temperature, the phase and orientation didn't change, diffraction peak enhanced, and the structure of WN became more complete.
2. At the annealing temperature of 400℃, WN(100) peak of WN-2 was the most obvious peak. Over-high dose of nitrogen would increase the bonding energy of W-N, and this made the WN(100) peak intensity of WN-3 is the second highest. At the annealing temperature of 600℃, the peak signal of WN-1 is the highest because there was no over-saturate nitrogen atoms to block the bonding.
3. Nitrogen between WNx would separate out during RTA from the analysis of TDS. This was because RTA would cause the nitrogen to separate out too quickly and caused the film to crack. This effect could be avoided when replacing RTA with furnace annealing.
4. Thermal stability of WN_x on SiO_2 could be affected by content of nitrogen atoms and annealing temperature. But thermal stability of WN_x on HfO_2 is better that that on SiO_2.
5. The work function modulation of WN_x by increasing nitrogen ratio is divided into two stages. First stage is from pure metal tungsten to tungsten nitride and second stage is affected by the ratio of nitrogen atoms.
6. At 600℃ annealing, the work function decreases as the ratio of nitrogen flow rate increases, and this is because the incomplete structure caused by high dose of nitrogen atoms. The modulation range of work function is about 0.2V as the ratio of N/W is from 0.8 to 0.57. And the work function increases slightly with the annealing temperature.

The range of work function modulation can be 0.4V~0.5V from pure tungsten metal to WN_x with the N/W ratio of 1.57. This modulation range has finite effect for the adjustment of threshold voltage. For the process temperature, the content of nitrogen atoms can't be over saturate too much. Otherwise, the thermal stability would be affected. Over high sheet

resistance seems to be the common problem of nitride which to be the candidate of metal gate, and this could be solved by stack a layer of low resistance metal upon nitride.

Besides, the work function of WN_x on HfO_2 is only 0.1V higher than that on SiO_2. This effect confirmed that Fermi pinning effect occurred. It’s a problem worthy to notice and make further research for it.

References

[1]. G. Wei, “ Trandition Metal Nitride Functional Coatings”, JOM. September 2001.Y. G. shen, Y. W. Mai, “effect of oxygen on residual stress and structural properties of tungsten nitride films grown by reactive magnetron sputtering”, MSE, B76(2000), p. 107-115.

[2]. P. C. Jiang, “Preparation of W-N thin film and its characteristics as gate electrode”, NCKU MSE 2002.

[3]. K. J. Huber and C. R. Aita, “Resistivity changes and phase evolution in W-N films sputter deposited in Ne-N2 and Ar-N2 discharges” J. Vac. Scl. Technol. A 6 (2), May/Jun 1988.

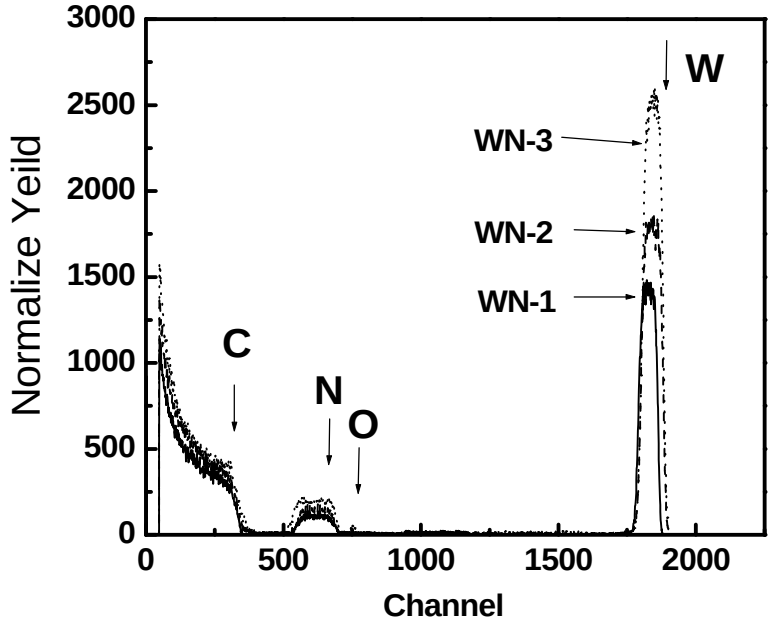
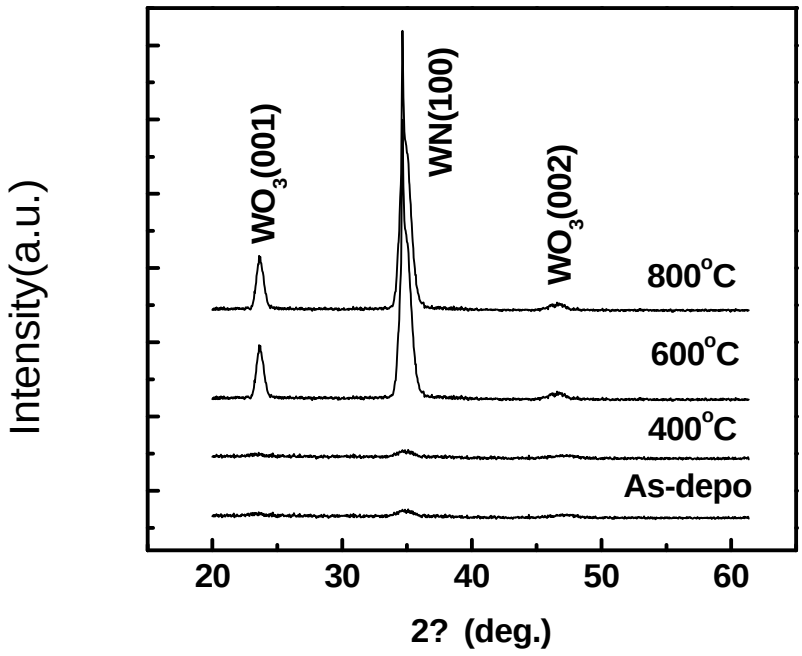


Fig.5-1. RBS spectrum of WN_x on carbon substrate.

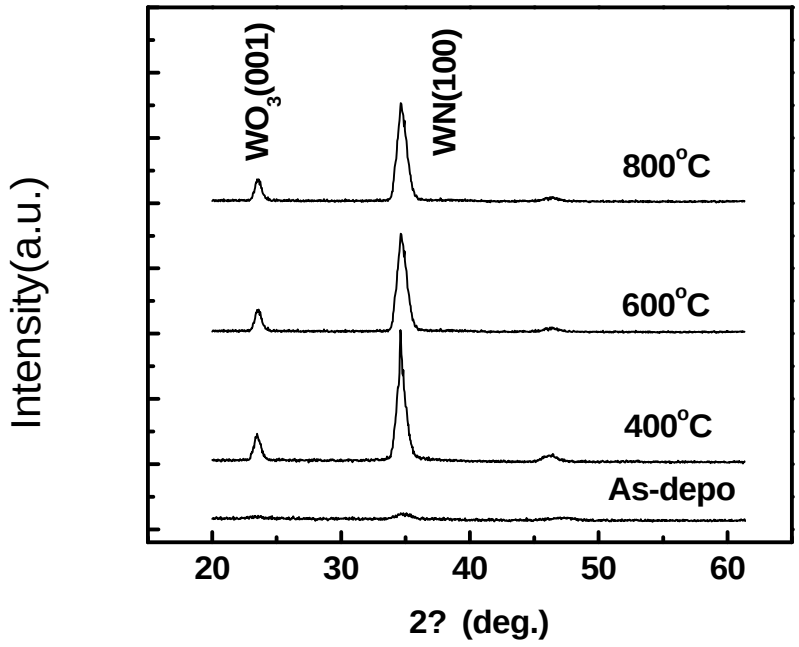
Ratio of Ar/N_2 flow rate: WN-1=20/5, WN-2=20/10, WN-3=20/20

Ratio of N/W: WN-1=0.8, WN-2=1.26, WN-3=1.57

(a)


Intensity(a.u.)
WO3(001)
WN(100)
WO3(002)
800°C
600°C
400°C
As-depo
20
30
40
50
60
2? (deg.)

(b)


Intensity(a.u.)
WO3(001)
WN(100)
800°C
600°C
400°C
As-depo
20
30
40
50
60
2? (deg.)

(c)

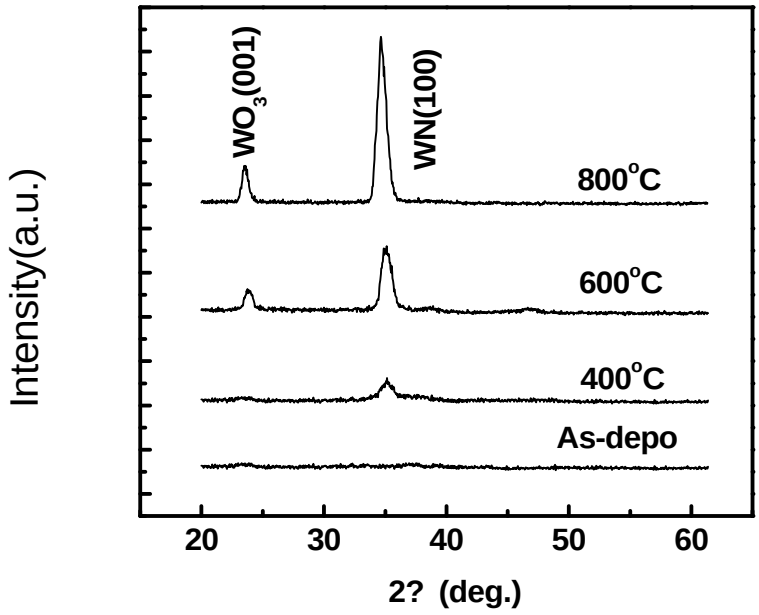


Fig.5-2. (a) XRD spectrums of WN-1 with various annealing temperature, (b) XRD spectrums of WN-2 with various annealing temperature, and (c) XRD spectrums of WN-3 with various annealing temperature.

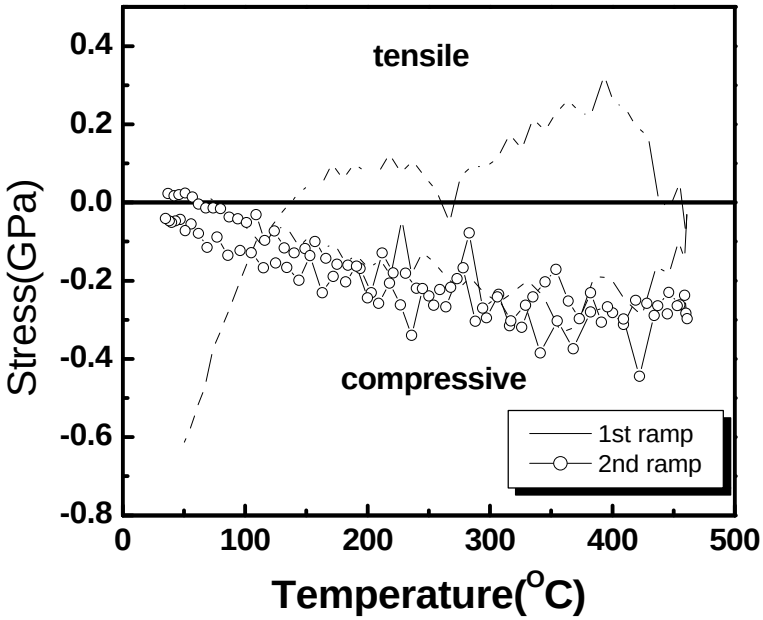


Fig.5-3. Film stress of WN-2 versus annealing temperature

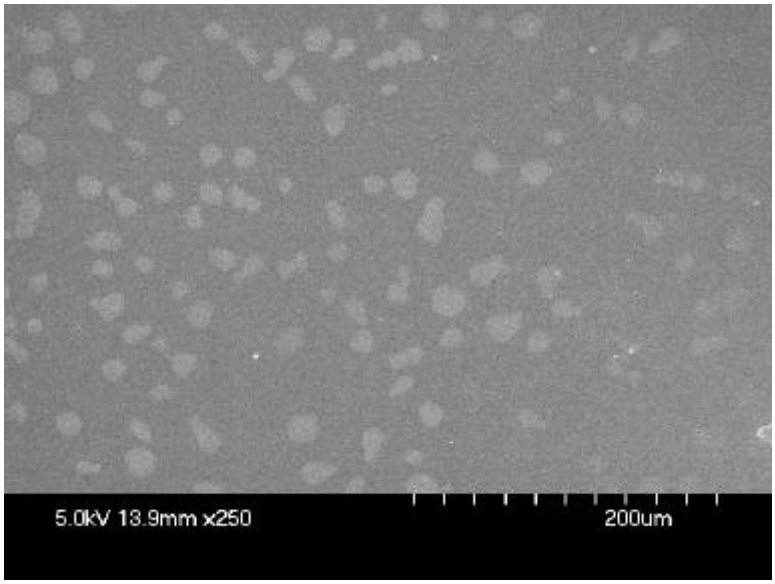
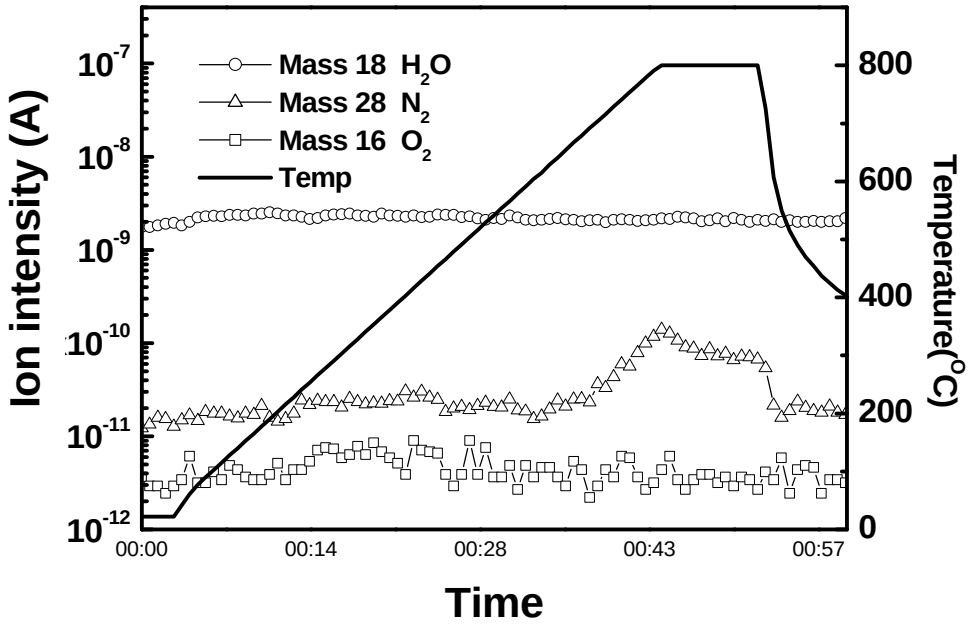


Fig.5-4. SEM photo of cracked metal surface.

(a)



(b)

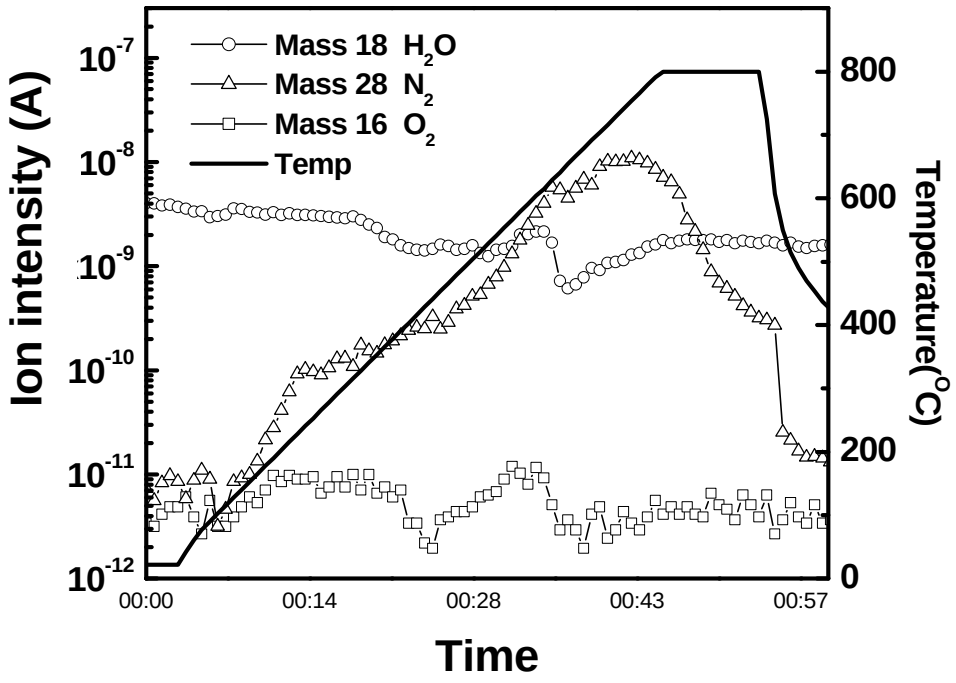
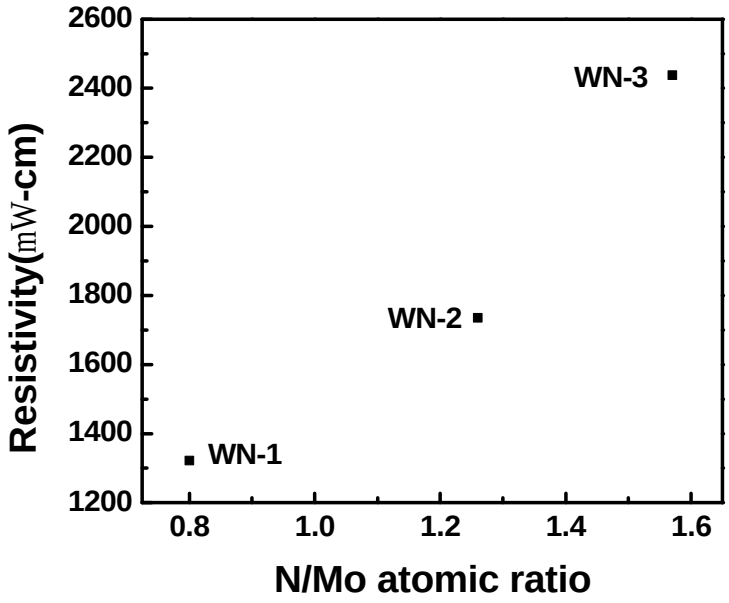


Fig.5-5. (a) background ion current of various gases in Ar environment, and (b) background ion current of sample at 800℃ annealing for 10 minutes in Ar environment.

(a)



(b)

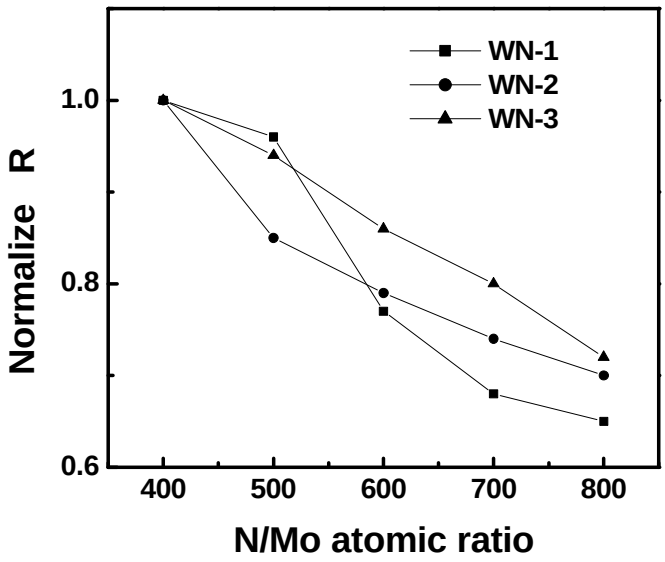


Fig.5-6. (a) Sheet resistance of 60nm as-deposit WN_x films and (b) sheet resistance of 60nm WN_x after annealing at different temperatures. The sheet resistance is normalized to that of 400℃.

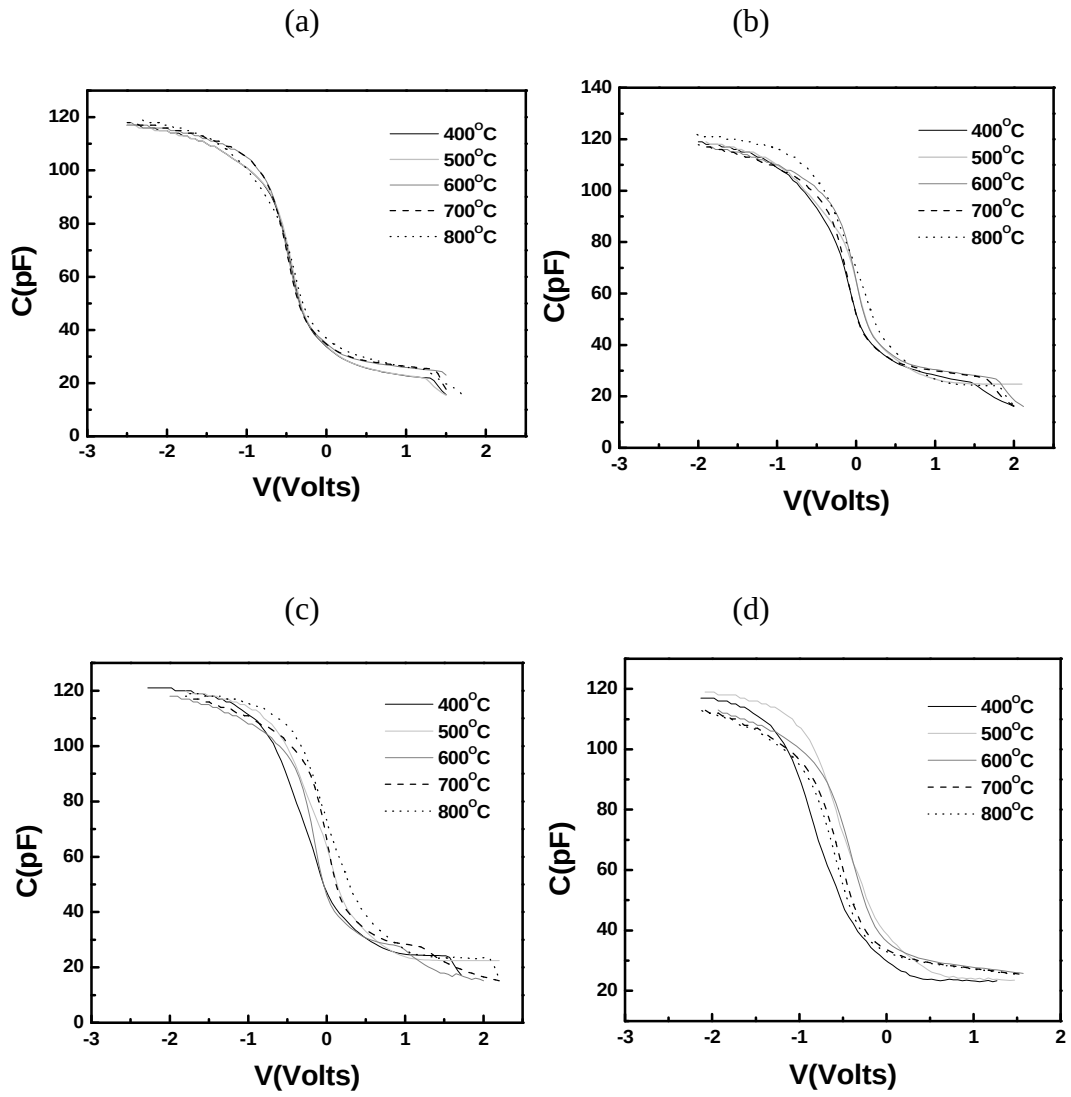


Fig.5-7. CV curves of WN_x/SiO_2 with different annealing temperatures.
(a)WN-0; (b)WN-1; (c)WN-2; (d)WN-3.

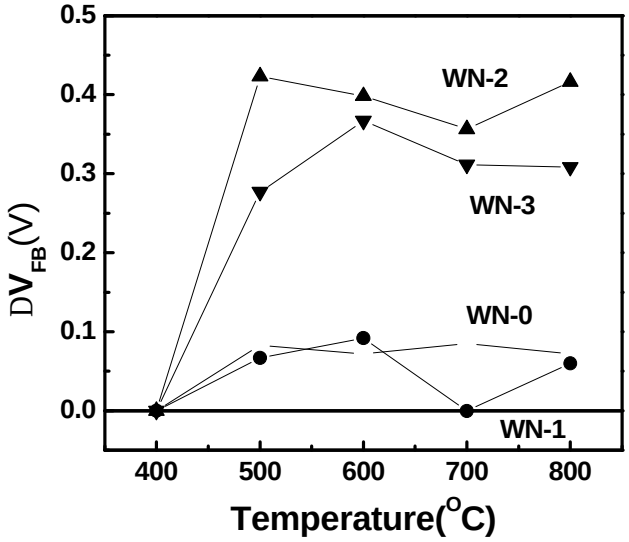


Fig.5-8. Flat-band voltage shift of WN_x/SiO_2 with different annealing temperatures.

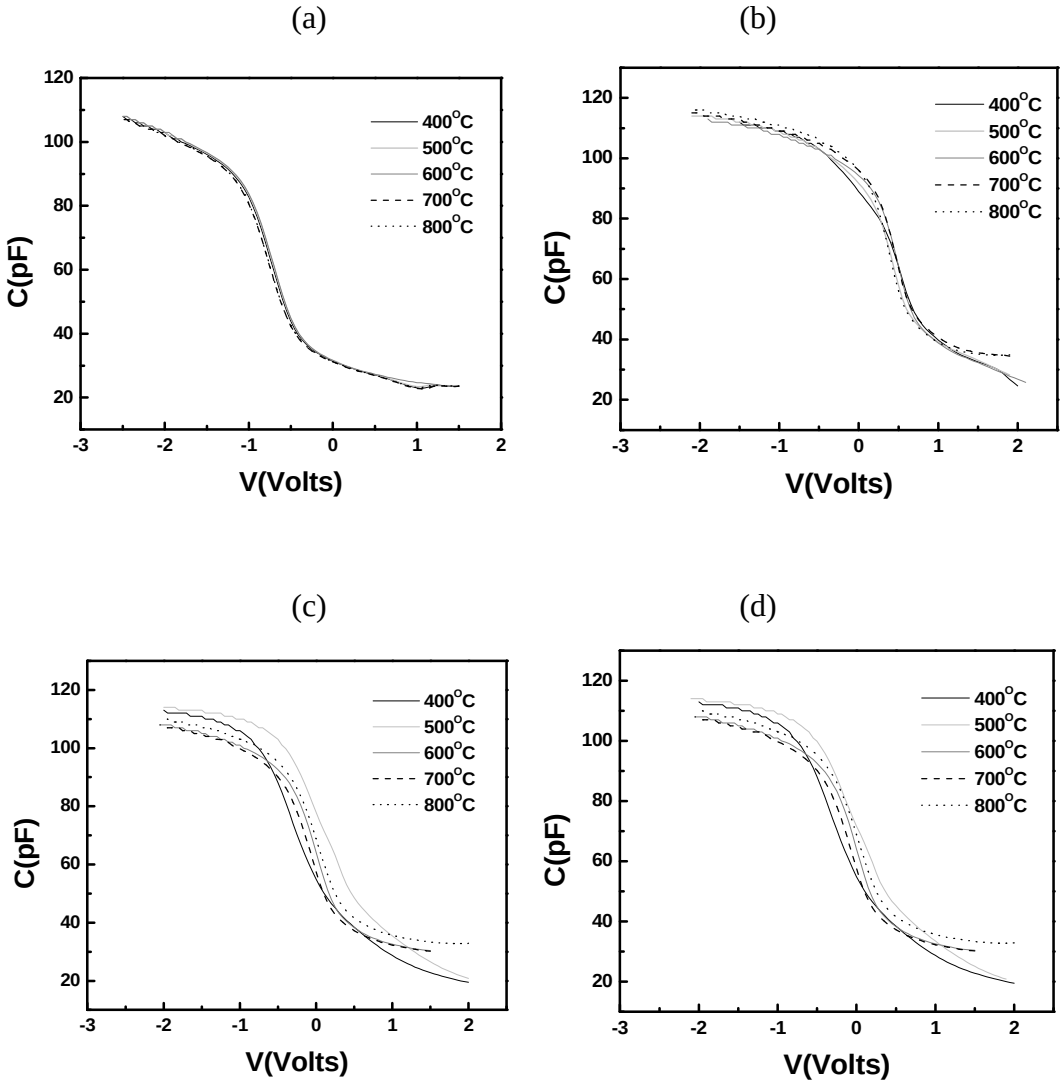


Fig.5-9. CV curves of $WN_x/HfO_2/SiO_2$ with different annealing temperatures.
(a)WN-0; (b)WN-1; (c)WN-2; (d)WN-3.

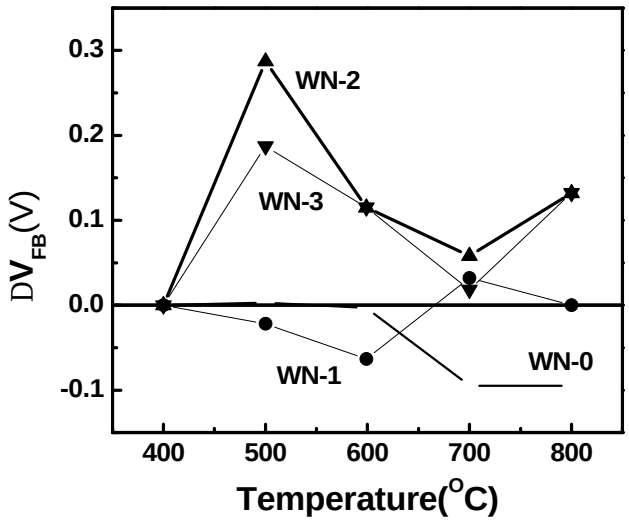


Fig.5-10. Flat-band voltage shift of $WN_x/HfO_2/SiO_2$ with different annealing temperatures.

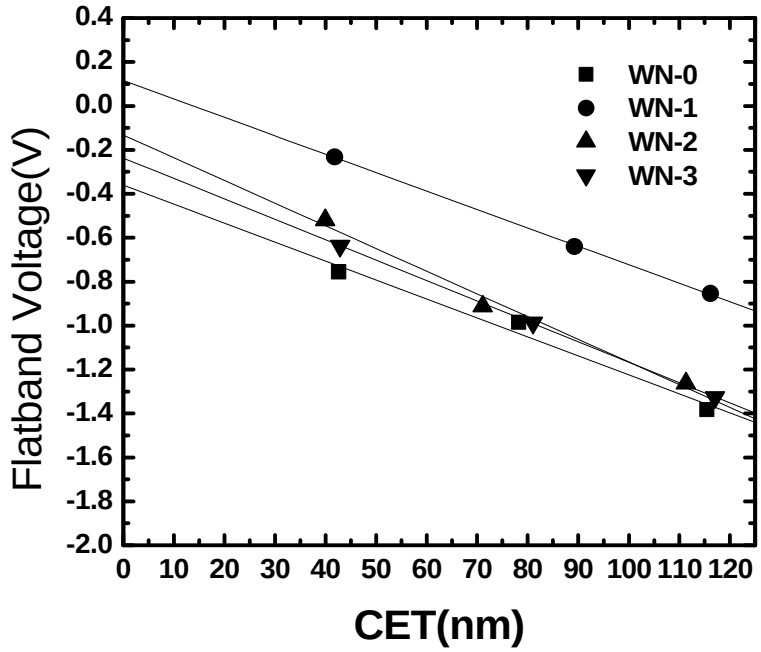


Fig.5-11. Flat-band voltage shift of WN_x/SiO_2 versus CET.

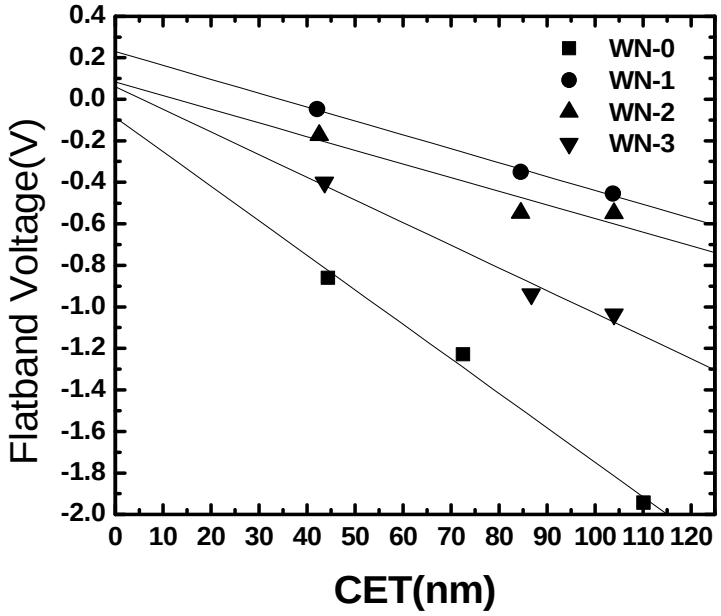


Fig.5-12. Flat-band voltage shift of WN_x/HfO_2(5nm)/SiO_2(40nm) versus CET.

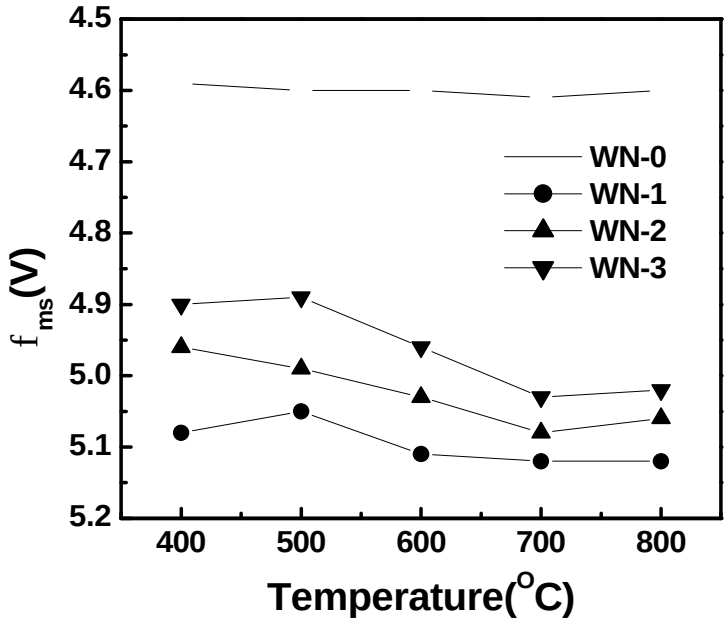


Fig.5-13. Work function of WN_x/SiO_2(40nm) versus annealing temperature.

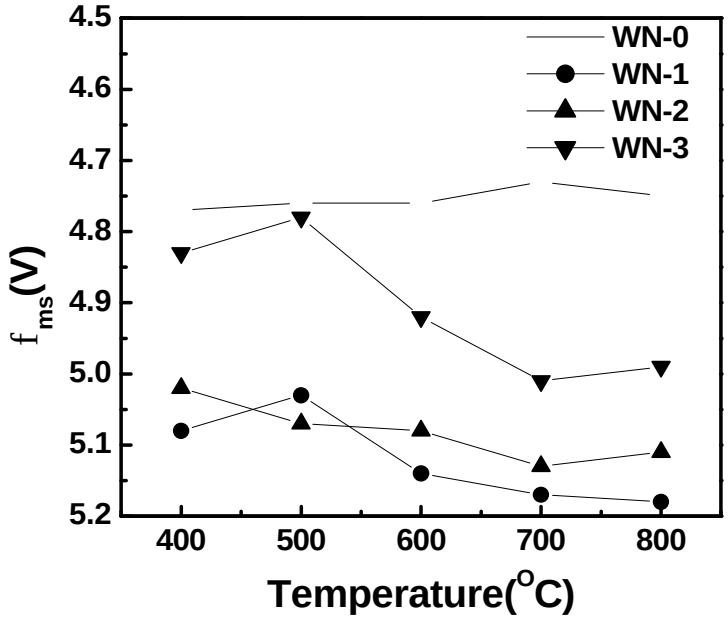


Fig.5-14. Work function of WN_x/HfO_2(5nm)/SiO_2(40nm) versus annealing temperature.

Chapter 6
Formation of Interfacial Layer during Reactive Sputtering of Hafnium Oxide

6-1 Introduction

Silicon dioxide (SiO_2) have been used as gate dielectric of CMOS devices for several decades because of its superior properties such as low interface state density, large energy bandgap (8.9eV), low leakage current, and good thermal stability for Si substrate and poly-Si gate. As device dimensions scale down, the thickness of SiO_2 must be reduced to keep sufficient current driving capability. But when the thickness of SiO_2 was below 3.5nm, direct tunneling current increases 100 times for every 0.4~0.5 nm decrease of thickness [1]. This high gate leakage current would increase standby power consumption and induce loss of inversion layer charges. According to the 2001 ITRS roadmap, the effective oxide thickness (EOT, a number which converts thickness of dielectric thickness into thickness of SiO_2) will reach 1.8nm and the maximum gate current should be lower than $2mA/cm^2$ for low power application in 2005 [2]. The simulated leakage current of 1.8nm SiO_2 was about $1A/cm^2$ and couldn't meet the specified gate leakage current.

In order to reduce gate current caused by direct tunneling, the physically thickness of dielectrics must increase such that the EOT can scale down continuously. New gate dielectrics with dielectric constant (K) higher than SiO_2 must be developed. Oxynitride (SiON), with K in the range of 5~7, has been extensively studied and was found to exhibit more controllable oxidation rate, lower interface state generation, improved resistance against dopant diffusion, higher dielectric integrity, lower stress induced leakage current, and lower charge trapping characteristics [3-5]. It has been thought as an alternative dielectric for the next generation. But it is unclear if oxynitride will meet future leakage current target because its dielectric constant is not high enough. Several alternative high dielectric constant (high-k) materials with dielectric constant higher than SiON have been studied to overcome the challenge of gate dielectric scale down.

The most commonly reported high-k materials are HfO_2, ZrO_2, Ta_2O_5, TiO_2, Al_2O_3, and La_2O_3, etc [6-12]. Among these candidates, HfO_2 attracted much more attention from recent researches. The reported dielectric constant of HfO_2 is about 25~30 [6, 7]. This magnitude of

K-value is higher than that of Si_3N_4 (~7) and Al_2O_3 (8~11.5) [6, 7]. At the same time, it is not too high to induce sever FIBL effect [13]. The energy bandgap of HfO_2 is about 5.68eV, which is higher than that of the other high-K materials [14]. Band alignment determines the barrier height for electron and hole tunneling from gate or Si substrate. The calculated band offsets of HfO_2 for electron and hole is 1.5ev and 3.4eV, respectively [14]. This band alignment is acceptable and better than other high-K materials such as Ta_2O_5 [14]. The free energy of reaction with Si is about 47.6 Kcal/mole at 727℃, which is also higher than that of TiO_2 and Ta_2O_5. Therefore, HfO_2 is a more stable material on Si substrate as compared to TiO_2 and Ta_2O_5 [15]. Among the elements in the IVA group of the periodic table (Ti, Zr, Hf), Hf has the highest heat of formation (271 kcal/mole) [16]. Unlike other silicides, the silicide of Hf can be easily oxidized [17]. That means that Hf is easy to be oxidized to form HfO_2 and the oxide of Hf is usually stable on Si substrate. Unlike ZrO_2, HfO_2 shows a good thermodynamic stability with poly-Si. It had been reported that HfO_2 would not react with poly-Si at temperatures as high as 1000℃ [18].

Several deposition techniques have been employed to prepare HfO_2 film. They are physical vapor deposition (PVD) [19, 20], chemical vapor deposition (CVD) [21, 22], atomic layer deposition (ALD) [23, 24], and jet vapor deposition (JVD) [25, 26]. Among these deposition techniques, PVD has advantages of simple process, high purity, and low cost-of-ownership. However, unusually thick interfacial layer (IL) was observed in some literatures [27]. Fig.6-1 shows the calculated impact of interfacial layer on the effective k-value of the HfO_2/IL stack assuming the k-value of HfO_2 is 27. A 10% SiO_2-like interfacial layer results in a more than 30% degradation of effective k-value. To take the advantages of high K value of HfO_2 thoroughly, the interfacial layer must be reduced as possible.

In this chapter, we focused on the formation of interfacial layer using PVD method. Various deposition schemes were employed to form HfO_2 film. Detailed experimental procedure is described in the next section. Experimental results are presented and discussed in section 6-3. The formation mechanism of interfacial layer and the guidelines for minimizing interfacial layer are proposed at last.

6-2 Experimental Procedure

Simple metal-insulator-silicon (MIS) structures were fabricated to study the effective oxide thickness (EOT) and interfacial layer at HfO_2 /Si interface. The main process flow is briefly listed in Fig.6-2. The starting material is 6-inches (100)-oriented p-type wafer. After

standard RCA clean, wafers were immersed in dilute HF solution to remove chemical oxide. Wafers were then loaded into the chamber of a reactively DC sputtering system. During film deposition, substrate temperature was held at 100℃. Either HfO_2 or Hf film was deposited by sputtering from a Hf target. The base pressure of the sputtering chamber before deposition was pumped down to $2x10^{-8}$ Torr and the pressure during deposition was kept at $2x10^{-3}$ Torr. When Hf was deposited, the gas and flow rate is Ar and 120 sccm, respectively. For HfO_2 deposition, the gas mixture and flow rate is Ar/O_2 and 30sccm/10sccm, respectively. The deposition power was kept at 100W. The deposition rate of HfO_2 and Hf is different for different power and gas ratio. For the deposition condition used in this work, the deposition rate of HfO_2 and Hf is about 0.6nm/min and 9.6nm/min, respectively. The thickness ratio of the HfO_2/Hf stack was split into two categories. One is fixing the bottom Hf thickness at 1 nm and varying the top HfO_2 thickness from 3 to 9 nm. The other is fixing the top HfO_2 thickness at 7nm and varying the bottom Hf thickness from 0 to 5 nm. The deposited film structures and sample ID are listed in Table 6-1.

Post-deposition-annealing (PDA) was performed in a rapid thermal annealing (RTA) system at 600℃ for 30sec in N_2 ambient. Since oxygen can penetrate through both Hf and HfO_2 films, the deposited Hf layer was converted into HfO_2 during PDA by reacting with residual oxygen in annealing ambient [16, 28, 29]. Platinum is used as gate electrode due to its inert property. Pt was deposited in an e-beam evaporation system through a shadow mask after PDA. The area of the capacitor is $3.63x10^{-3}$ cm^2. Then a backside metallization process completed the sample fabrication. Metal-Insulator-Metal (MIM) sample was also fabricated to identify the actual dielectric constant of the deposited HfO_2 layer. TiN is used as gate electrode of the MIM sample.

The thickness of deposited film was measured with N&K analyzer. The surface roughness was measured with atomic force microscope (AFM). For electrical analysis, high frequency capacitance-voltage (HFCV) characteristic was measured at 100 kHz with a precision impedance meter of model Agilent 4284A. Effective dielectric constant is then calculated from the measured capacitance at accumulation mode and optically measured dielectric thickness. For material analysis, transmission electron microscopy (TEM) was used to determine the exact thickness and identify the interface situation between HfO_2 and Si substrate. The dielectric constant of HfO_2 can be calculated from the MIM sample. Then, the dielectric constant of the interfacial layer can be determined according to the actual thickness of each layer and the dielectric constant of HfO_2 from MIM sample. The composition of the

interfacial layer was further identified with Energy Dispersive Microscopy (EDS) in a TEM system.

6-3 Result and Discussion

The uniformity, defined as the range of thickness divided by 2 times of the average thickness, of as-deposited film thickness measured with N&K analyzer is between 4% and 5% for both Hf and HfO_2 films at all thickness. Fig.6-3 shows that the surface roughness of 2 nm thick Hf film measured by AFM is 0.253nm, which is very close to that of original Si surface and is much smaller than the thickness of deposited film. The continuity of films was further characterized with plane-view SEM inspection, no pin holes and agglomeration phenomenon were observed. All of these results confirm the homogeneity of the deposited films.

Fig.6-4 shows the HFCV curve of the sample H73. The curve looks normal but the calculated effective K-value is only 8.5, which is much lower than the typical K-value of HfO_2 film. To check if the deposited film is normal, TiN/Hf/HfO_2/Hf/TiN structure was prepared. The thickness of dielectric is 12.5 nm from the cross-sectional TEM inspection. The exact K-value of HfO_2 film was calculated to be 27.9 and this value is consistent with the reported K-value of HfO_2, 20~30. To understand why the effective K-value of sample H73 is so low, high resolution TEM was employed to inspect the actual sample structure. Fig.6-5 shows the cross sectional TEM micrograph of sample H73. Because of the poor adhesion between Pt and HfO_2, the Pt layer peeled-off during sample preparation. A thick interfacial layer of 3.2 nm thick between HfO_2 and Si substrate is clearly observed. This observation is consistent with that reported previously [27]. Because HfO_2 was deposited immediately after HF-dip step, there should not be such an unusual thick native oxide on the Si surface. In fact, the native oxide thickness measured on Si wafer just after HF dip process by N&K analyzer is less than 0.3 nm.

The interfacial layer may be either silicon dioxide or Hf-silicate. To clarify what material it is, the K-value of the interfacial layer was estimated using the thickness of interfacial layer and the thickness of HfO_2 layer measured from Fig.6-5, and the dielectric constant of HfO_2 is assumed to be 27.9. The estimated K value of the interfacial layer is 3.8, which indicates that the interfacial layer is SiO_2-liked material. The composition of the interfacial layer was analyzed with EDS. The signal intensity of Hf within HfO_2 layer is much stronger than that within interfacial layer, while the signal intensity of oxygen keeps similar. This result confirms that the interfacial layer is SiO_2-like material but not Hf-silicate.

Since the sample shown in Fig.6-5 did not experience PDA, the thick interfacial oxide must be grown during the HfO_2 deposition period. It should be noted that the PDA process used in this work only produce a SiO_2 layer thinner than 0.5 nm on bare Si. Even if the sample experienced PDA, the 3.2nm thick SiO_2-liked IL can not be attributed to the PDA process.

Up to now, a fact can be sure is that the thick oxide layer is formed during the reactive sputter process. Why reactive sputter introduces such a thick oxide layer? The temperature during sputtering is only 100℃ and the content of oxygen is much lower than that in typical oxidation furnace. The partial pressure of oxygen during sputtering is kept at 0.5 mTorr and the deposition time is shorter than 15 min. So it is impossible that this thick SiO_2 layer comes from the oxidation of the Si substrate by reacting with oxygen molecule under such a low thermal budget and short period of time.

In order to investigate the origin of interfacial SiO_2, optical emission spectroscopy (OES) was employed to detect the chemical state in sputter chamber during film deposition. Fig.6-6 shows the OES spectrums for various gas conditions. Only O-radical instead of O_2-radical is detected in the sputtering chamber, while in typical O_2 plasma system, O_2-radical is the main radical detected [28]. Based on the observation, an O-radicals enhanced oxidation model is proposed to explain the thick interfacial oxide layer. The injected oxygen molecules are excited into ions and radicals. The oxygen related species in the plasma system may include O-ion, O_2-ion, O-radical, O_2-radical, etc. O_2-radicals may collide with the other particles and decompose into O-radicals and/or O-ions. Some O-radicals and O_2-radicals diffuse randomly to Si surface and form an interfacial oxide layer at the initial deposition stage. Ions are accelerated toward target and after bombarding the target, all of the O_2-ions decompose into O-ions or O-radicals. Some reflected O-radicals move toward wafers with high energy. Because O-radical has small radius and is highly reactive, it penetrates through the HfO_2/Hf stack rapidly and during the penetration, it not only oxidized the bottom Hf layer but also reacts with the Si substrate to form SiO_2. Therefore, a very thick SiO_2 layer is formed during the reactive sputtering process. The oxidation due to the other O-contained species can not be ruled out totally. Since O-radical has the highest activity and the intensity of O-radical is much higher than the other species, it is believed that O-radicals play the major role.

Based on the mechanism of formation of thick interfacial SiO_2, a series of HfO_2/Hf stack structures are examined to reveal the efficiency of the bottom Hf layer on the reduction of interfacial SiO_2. Fig.6-7(a) and (b) show the effective K value as a function of thickness of bottom Hf layer and of thickness of upper HfO_2 layer, respectively. For the same thickness of

top HfO_2 layer, thicker Hf layer results in higher effective K value. On the other hand, for the same thickness of bottom Hf layer, thicker HfO_2 layer results in lower effective K value. Because the final thickness of dielectric is different for different sample, the improvement of effective K value may be due to the reduction of interfacial oxide layer or simply due to the decrease of the thickness percentage of the interfacial oxide layer. Fig.6-8(a), (b), and (c) show the cross-sectional TEM micrographs of samples with HfO_2/Hf stack of 7nm/1nm (sample H71), 7nm/5nm (sample H75), and 3nm/1nm (sample H31), respectively. The interfacial layer thickness depends on the HfO_2/Hf stack structure. The correlation between interfacial layer thickness and bottom Hf thickness with the same upper HfO_2 thickness is shown in Fig.6-9. By increasing the bottom Hf thickness to 5 nm, the thickness of interfacial oxide layer can be reduced to 1.3 nm, which is the same as that observed in the sample with only Hf layer (H03). This phenomenon implies that a 5 nm thick Hf is necessary to block the diffusion of O-radicals during reactive sputtering of HfO_2. The origin of the 1-1.5 nm thick interfacial oxide layer is postulated to the surviving oxygen in the chamber or the traced oxygen impurity in Ar gas.

Correlation between interfacial layer thickness and upper HfO_2 thickness is shown in Fig.6-10. Similar interfacial SiO_2 thickness of about 3-4 nm was observed. This result indicates that the growth of interfacial oxide layer occurs at the early stage of HfO_2 deposition. With the increase of HfO_2 thickness, oxidation is blocked.

6-4 Conclusions

In this work, the formation of interfacial SiO_2 layer at HfO_2/Si interface was studied comprehensively. It is observed that using physical vapor deposition technique, it is difficult to totally eliminate the formation of interfacial SiO_2 layer. During reactive sputtering deposition of HfO_2 layer, an interfacial SiO_2 layer thicker than 3 nm would be grown. Such an unusual thick SiO_2 layer is formed due to the enhanced oxidation of O-radicals generated in the sputtering chamber. Adoption of two-step deposition method, the thickness of interfacial SiO_2 layer can be reduced only if the bottom Hf layer is thicker than 5 nm. However, the reduction of effective oxide thickness would be limited. Re-oxidation of Hf film sounds a better choice. A 1.0-1.5 nm thick interfacial SiO_2 layer is still observed. This implies that the traced oxygen in the sputtering chamber plays critical role on the formation of interfacial layer. To conclude, reactive sputtering is not a good method to prepare HfO_2 layer with negligible interfacial SiO_2 layer. Re-oxidation of Hf film is a better choice, but the oxygen content in the

sputtering chamber must be well controlled.

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Table 6-1. Sample ID and film structures used in this work.

Sample ID	H70	H71	H73	H75	H31	H51	H71	H91	H03
HfO_2 (nm)	7	7	7	7	3	5	7	9	0
Hf (nm)	0	1	3	5	1	1	1	1	3

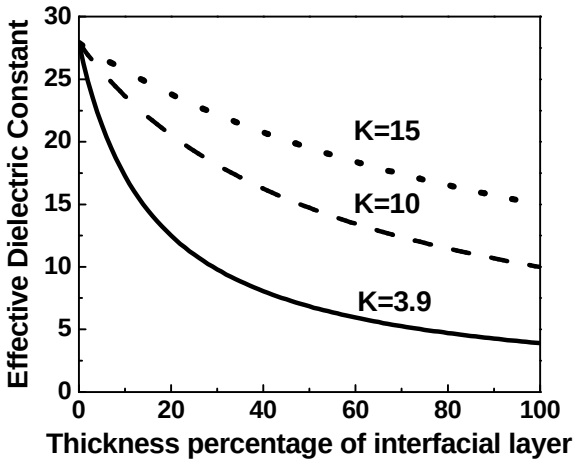


Fig.6-1. Effective dielectric constant of HfO_2/interfacial layer stack structure versus the thickness of interfacial layer with the dielectric constant of interfacial layer as parameter. The dielectric constant of HfO_2 is assumed to be 27.

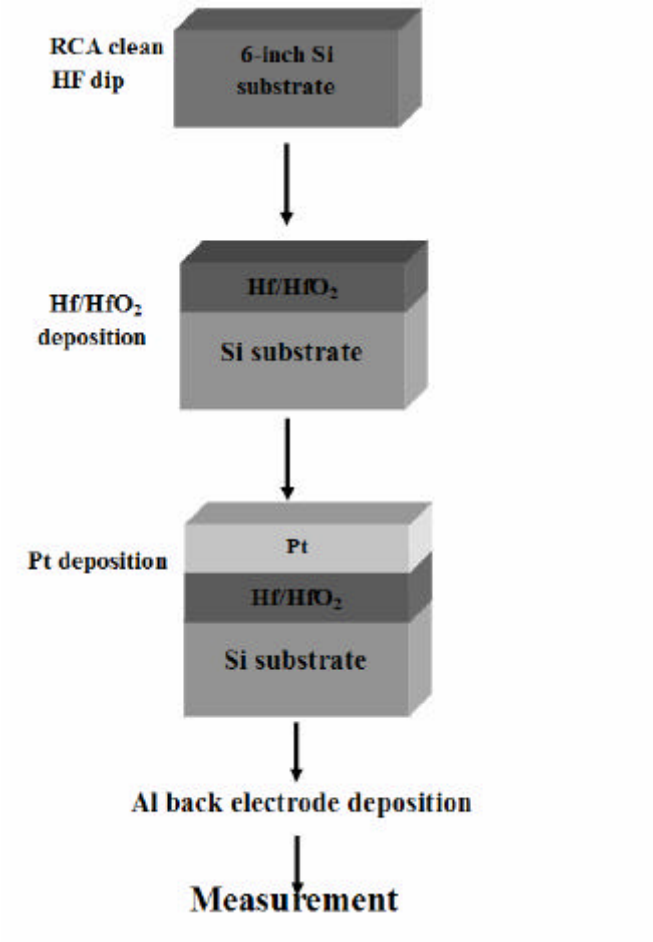


Fig.6-2. Schematic drawing of main process flow used in this work.

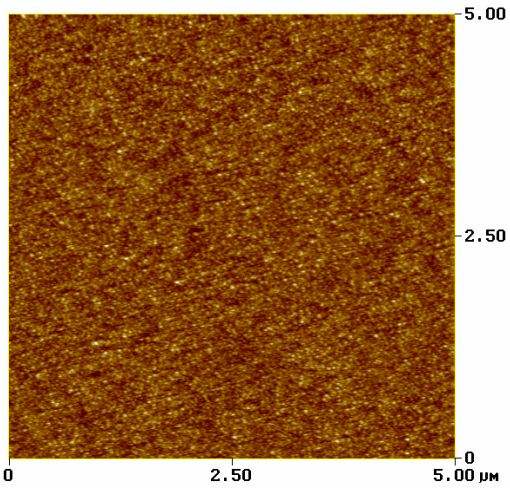


Fig.6-3. Atomic force microscopic image of 2 nm thick Hf film. The root-mean-square roughness is only 0.253nm.

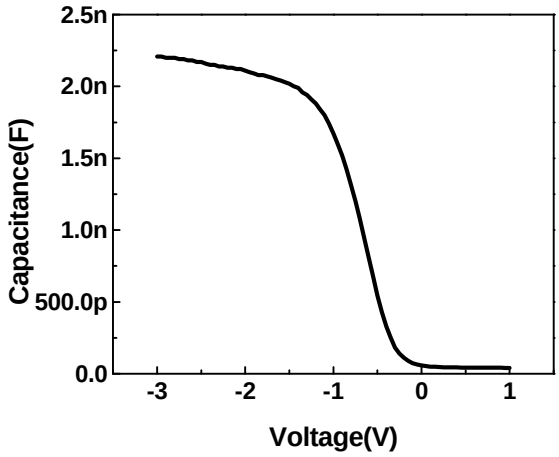


Fig.6-4. High frequency capacitance-voltage curve of sample H73. The curve looks normal but the calculated effective K-value is only 8.5.

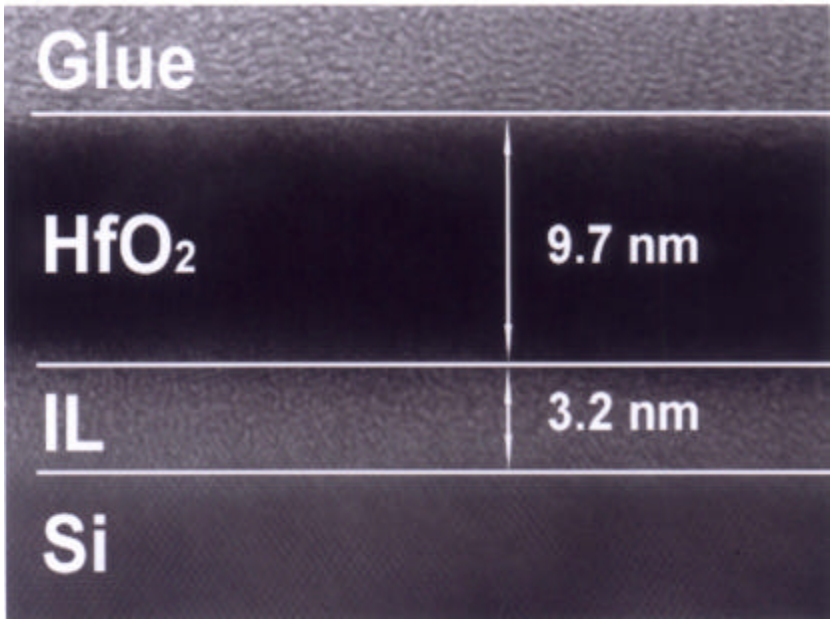


Fig.6-5. Cross-sectional TEM micrograph of sample H73. A thick interfacial layer of 3.2 nm thick between HfO_2 and Si substrate is clearly observed.

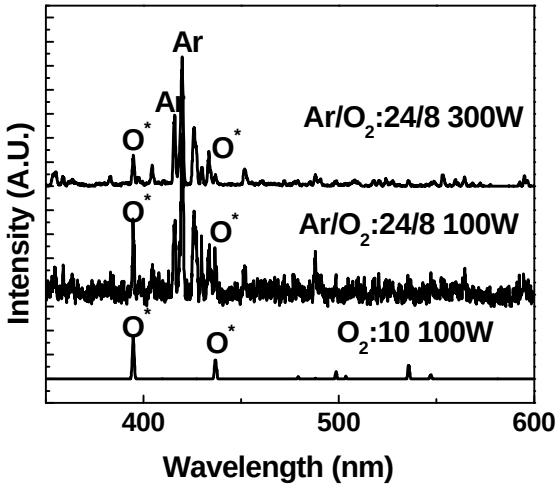
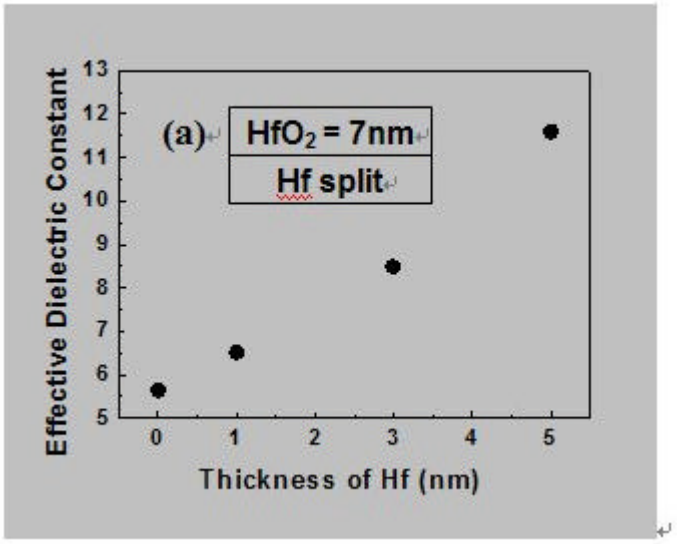


Fig.6-6. Optical-emission-spectrums of various gas mixtures in the sputtering chamber. Strong O-radical signals are detected in all cases.

(a)



(b)

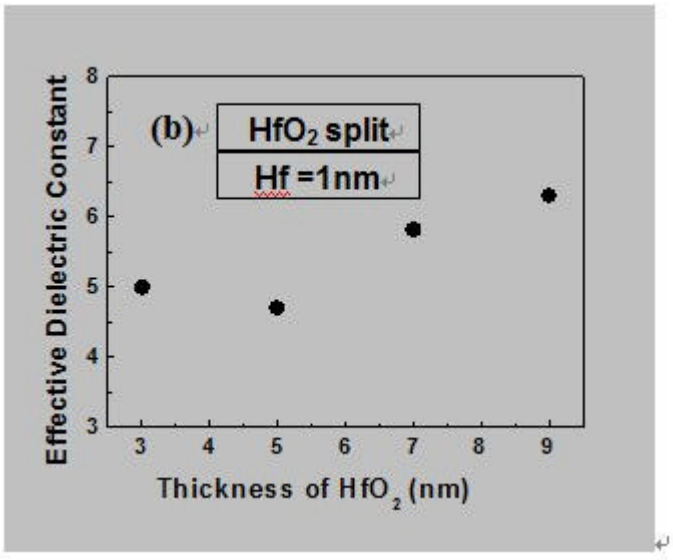


Fig.6-7. Effective dielectric constant as a function of the thickness of (a) bottom Hf layer and (b) upper HfO_2 layer.

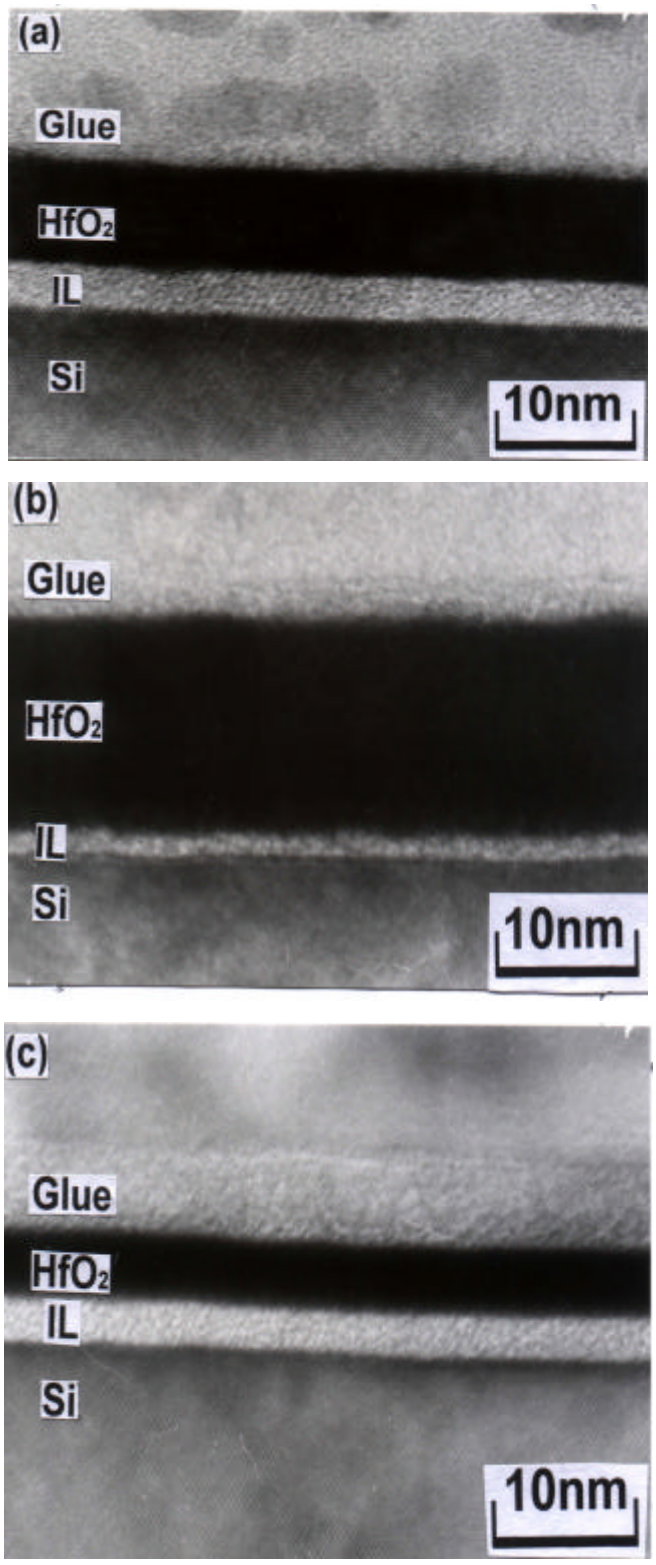


Fig.6-8. Cross-sectional TEM micrographs of samples (a) H71, (b) H75, and (c) H31.

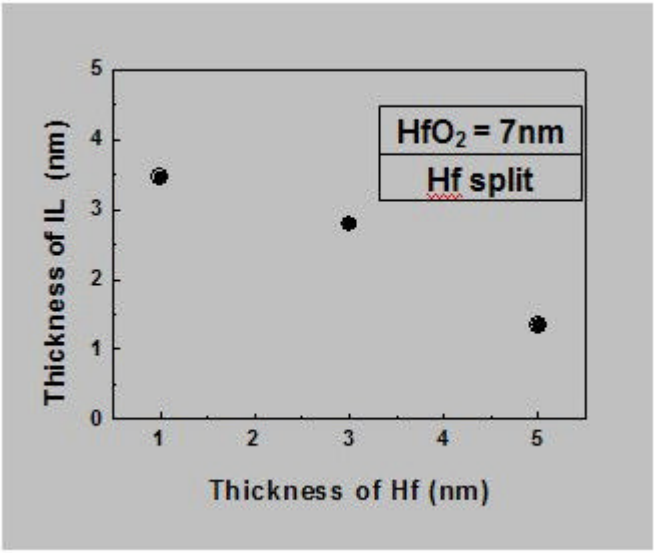


Fig.6-9. Interfacial SiO_2 layer thickness as a function of bottom Hf thickness with the same upper HfO_2 thickness.

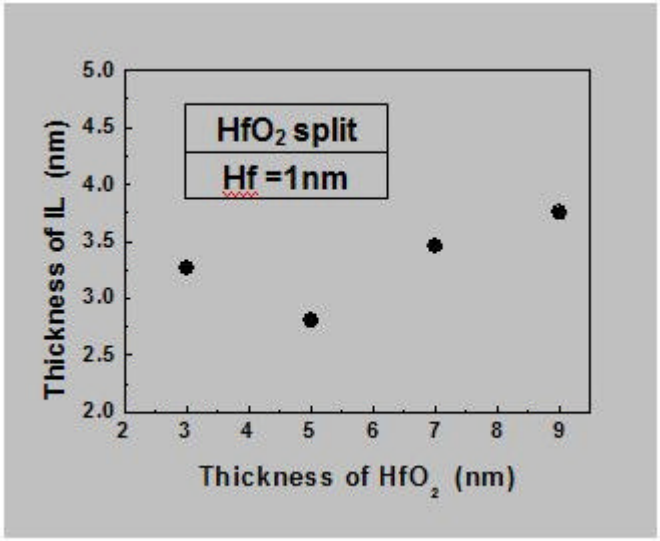


Fig.6-10. Interfacial SiO_2 layer thickness as a function of upper HfO_2 thickness with the same bottom Hf thickness.

Chapter 7
Electrical Characteristics of HfO_2 Film Prepared by MOCVD

7-1 Introduction

As the dimensions of complementary metal oxide semiconductor (CMOS) devices are scaled into the nanometer regime, the equivalent oxide thickness (EOT) of the gate dielectric decreases steadily to thinner than 1nm [1]. Its leakage current under normal operation bias falls into the direct tunneling regime [2]. High-k materials are employed to increase the physical thickness of the gate insulator while maintaining the same EOT and gate capacitance, thus reduces significantly the tunneling leakage current. Although many high-k materials are proposed to replace silicon dioxide as gate insulator, HfO_2 is the most promising one for its excellent advantages, such as a suitable dielectric constant (~25), high band-gap energy (~ 5.9eV), suitable tunneling barrier height for both electron and hole (>1eV), and thermal compatibility with contemporary CMOS process [3-8].

As mentioned in previous chapter, many methods had been employed to deposit high-k materials, such as physical vapor deposition (PVD) [6], metal-organic chemical vapor deposition (MOCVD) [8], atomic layer deposition (ALD) [8], and jet vapor deposition (JVD) [9]. The advantages and disadvantages of PVD and MOCVD are listed in Table7-2. Although PVD is a simple technique for depositing new materials for evaluation in an academic organization, it may cause damage to the electrical devices and is not preferred by industries because of poor step coverage and thickness uniformity [6].

In this chapter, we used MOCVD system to deposit HfO_2 film. For MOCVD system, it is known that precursors play a crucial role in determining process parameters, such as deposition temperature, vapor pressure, and contamination issues etc. In this thesis, the precursor is provided by the Axitron Co. and the details can not be disclosed at this moment. Different gate electrode, such as Al, Ta-Pt, Pt and poly-Si, were employed to investigate the effect of gate electrode on HfO_2. Different gas injection sequences, oxygen first and hafnium first, were study to simulate the two-step deposition method in PVD system and to reveal their effects on film properties. Different deposition temperatures, various oxygen flow rate, and various reaction gas, were needed to investigate the thin film electrical and material properties. Different surface treatment methods are also studied. Capacitance-voltage (C-V) and

current-voltage (I-V) characteristics are measured to evaluate the film electrical properties. Material and micro-structure analysis will be conducted in the next chapter.

7-2 Experimental Procedures

7-2-1 Metal / Insulator / Silicon (MIS-C) Sample Preparation

MIS capacitors were fabricated on p-type (100)-oriented silicon wafers with 8~10 Ω-cm nominal resistivity. After standard RCA clean process, three surface treatment methods were performed prior to film deposition. They are dilute HF-dip (HF-treatment), NH_3-annealing (NH_3-treatment) and rapid thermal oxidation (RTO-treatment). The HF-treatment is to immerse wafers into a 100:1 diluted HF solution after RCA clean and then spin dry without rinse in DI water. NH_3-treatment is to anneal wafers in pure NH_3 ambient at 800℃ for 60 minutes in a LPCVD system after RCA clean. Ellipsometry measurement indicates that a 1 nm thick silicon nitride layer is grown during this treatment. After NH_3-treatment, some wafers were annealed in N_2O ambient at 600℃ or 800℃ for 30sec prior to film deposition to improve the interface property between the nitride layer and silicon. The RTO-treatment is to grow a thin oxide layer on Si surface in a rapid thermal oxidation system at 800℃ for 30sec in pure O_2 ambient and then anneal in nitrogen ambient at 1000℃ for 30sec in the same chamber.

After surface treatment, wafers were put immediately into a MOCVD system for HfO_2 deposition. Three different deposition temperatures, 345℃, 400℃ and 500℃, were used to study the temperature effects. The reaction gases are O_2 and N_2O with various flow rates. The thickness of HfO_2 was set to 6 nm in most cases, which is controlled by the pulse number. The deposition rate was extracted by depositing thick HfO_2 film and measuring thickness with n&k analyzer. Because the system is designed for 200 mm wafers, a quarts carrier is adapted so that our 150mm wafers can be handled. Just prior to deposition, wafers were heated in O_2 ambient for 10min at the deposition temperature for thermal equilibrium and to replace the surface hydrogen termination with oxygen. The monolayer is expected to reduce the interface state density, which affects the electrical property significantly.

After film deposition, post-deposition annealing (PDA) was performed on all of the samples to investigate its impact on material properties and electrical characteristics of HfO_2. Most of the wafers were annealed at 600℃, 750℃, and 1000℃ for 30sec in nitrogen ambient . Some of them were annealed at 600℃, 800℃, 900℃, and 1000℃ for 30sec in

nitrogen or oxygen ambient. The deposition and annealing conditions are summarized in Table 7-3.

Pt-gated and Al-gated capacitors were formed in an e-beam evaporating system through a shadow mask after PDA. Pt has stable and inert chemical properties, but its adhesion with oxide is poor. Al is the most common electrode and is easy preparation in simple thermal evaporator system. A recently reported alloy gate electrode, Ta-Pt, was also prepared for comparison. After gate electrode deposition, 500nm thick Al was deposited at wafer backside as electrode for all samples to make good conductive contact to measurement system. The process flow of this MIS structure is illustrated in Fig.7-5.

7-2-2 Poly-Si / Insulator / Silicon (MIS-C) Sample Preparation

Since poly-Si is still the commonly used gate electrode in standard CMOS process, the MIS capacitor with poly-Si gate was also fabricated. The side-benefit of poly-Si gate is the gate patterning can be performed with conventional photolithography and etching techniques. The gate edge effect can be eliminated if suitable isolation technology is employed.

Typical LOCOS isolation structure was used for the poly-Si gate capacitor. After isolation process, HfO_2 was deposited at 400℃ and 500℃ with various O_2 and N_2O gas flow ratio following different surface treatments. All of these samples were annealed in N_2 ambient at 600℃ for 30sec after deposition. Un-doped Poly-Si of 200 nm thick was immediately deposited after the PDA process. Gate electrode patterns were defined by the conventional photolithography and the plasma etching techniques. The poly-Si gate was doped by ion-implantation of As^+ ions at 20 keV to a does of $3x10^{15}$ cm^{-2} followed by an activation annealing in N_2 RTA for 30sec at 900℃ or 1000℃. Finally, a 500 nm thick Al was deposited at wafer backside to make good conductive contact to measurement system.

7-2-3 Analysis Techniques

For electrical analysis, a precision impedance meter of model Agilent 4284 was used for C-V measurement and a semiconductor parameter analyzer of model Agilent 4156C was used for I-V measurement. High frequency C-V measurement was performed at 100 kHz, with a small ac signal of V_{rms}=30mV. In general, the bias voltage is swept from inversion mode to accumulation mode. In some case, forward and backward sweeps were performed to monitor the hysteresis phenomenon. Due to the high leakage current of most of the thin gate dielectric, parallel circuit model was employed. The capacitance-equivalent-thickness (CET) of gate

dielectric was calculated from the capacitance at accumulation mode and the calibrated gate area.

For material analysis, cross-sectional Transmission Electron Microscopy (TEM) inspection, atomic force microscopy (AFM), X-Ray Diffraction (XRD), transmission electron diffraction (TED), and X-ray photoelectron spectroscopy (XPS) were employed. Detailed analysis conditions and results will be discussed in the next chapter.

7-3 Electrical Results

Fig.7-6 is a schematic drawing indicating the relationship between measured effective oxide thickness and physical parameters. The effective oxide thickness (EOT) is defined as the physical thickness of gate dielectric divided by the ratio of dielectric constant of the dielectric material to the dielectric constant of SiO_2 (3.9). The CET_{acc} and CET_{inv} is the capacitance equivalent thickness of gate dielectric calculated from the measured gate capacitance at accumulation mode and inversion mode, respectively. The CET_{acc} consists of the EOT and the equivalent thickness of accumulation layer due to quantum effect (T_{qm}) [10]. The CET_{inv} consists of the EOT, T_{qm} and the equivalent thickness of gate depletion layer (T_{pd}) [10].

7-3-1 Effect of Gate Electrode

Before studying the effect of deposition parameters on the HfO_2 film properties, suitable gate electrode must be selected. It had been reported that metals show good adhesion to dielectric might form an interfacial layer between metal and dielectric [11]. It was also reported that an AlO_x-like interfacial layer may form at the Al/HfO_2 interface, while no interfacial layer was observed between Pt and HfO_2 [11]. Fig.7-7 shows the C-V characteristics of Al gate MIS-C and Ta-Pt gate MIS-C, where Ta-Pt is a newly reported gate materials [12]. The dielectric was 14nm thick HfO_2 deposited on HF-treated Si substrate followed by a N_2 RTA at 600℃ for 30sec. The flatband voltage difference is attributed to the work function difference between Al (4.1eV) and Ta-Pt (4.6eV) [12]. The capacitance at accumulation mode of Ta-Pt gate MIS-C is higher than that of Al gate MIS-C. After conversion, the CET of Ta-Pt gate and Al gate is 4.76nm and 7.04nm or the effective dielectric constant (?) is 11.47 and 7.76, respectively. This result indicates that the interfacial layer of the Al-gate device is thicker than that of the Ta-Pt gate device. Since the process before gate electrode deposition is identical and no further thermal treatment was performed after metal deposition, the interfacial layer thickness at HfO_2/Si interface must be identical for

both samples. It is thus postulates that as reported previously, an interfacial layer forms at the Al/HfO_2 interface.

It is known that the heat of formation of Al_2O_3 is 399 Kcal/mol, which is larger than that of HfO_2, 271 Kcal/mol [11]. It is reasonable that the AlO_x-like interfacial layer could form during Al evaporation. Due to the inert chemical property of Ta-Pt alloy, no interfacial layer would form between Ta-Pt and HfO_2. It is suggested that metals with heat of formation of metal oxides higher than that of HfO_2 is not likely to be used as gate electrode.

Fig7-8 shows the C-V characteristics of poly-Si gate and Pt-gate devices with 8 nm thick HfO_2 films deposited on NH_3-treated wafers followed by a 600℃ PDA in N_2 ambient for 30 sec. The CET values of poly-Si gate devices are larger than that of the Pt gate devices. This can not be explained by the poly-gate depletion effect because the CET is measured at accumulation mode. The only reasonable explanation is that an additional low dielectric constant interfacial layer formed at the poly-Si/HfO_2 interface during poly-Si deposition and dopant activation processes. The CET value increases with the increase of activation temperature supports the explanation.

Both Ta-Pt and Pt exhibit inert chemical properties and are suitable for studying HfO_2 properties. The deposition of Ta-Pt is more complicate than that of Pt. So, Pt is employed in the remaining part of the thesis. It should be noted that the adhesion of Pt to HfO_2 is poor so that it is difficult to form good gate contact. Besides, the lightly doped Si substrate adds additional series resistance to the device. As the leakage current of gate dielectric is not negligible, the measured capacitance using simple parallel circuit is lower than the actual capacitance due to the contribution of the series resistance [13-14]. In this thesis, 100 kHz was employed and no equivalent circuit correction was performed.

7-3-2 Effect of Gas Sequence

In the MOCVD system, precursor provides the hafnium atoms and O_2 gas provides oxygen atoms. The effect of gas injection sequence is examined in this subsection. The case of Hf-precursor being injected at first is called Hf-first and the case of O_2 being injected at first is called O_2-first. Fig.7-9(a) and (b) show the C-V characteristics and current density at -1V, respectively, of samples with HfO_2 deposited at 400℃ and 450℃. The O_2 flow rate is 300sccm and the deposition pressure is 3mbar. No PDA was performed in this experiment.

Even though the Hf-first scheme results in larger accumulation capacitance, which is attributed to thinner interfacial layer, it results in much higher leakage current than the O_2-first scheme. It is postulated that Hf is too heavy to migrate on silicon surface to form HfO_2 at the

initial stage of these two deposition schemes so that Hf may react with Si or Hf-rich thin film may be formed to lead to larger leakage current. Although the O_2-first scheme results in larger CET, which accounts or thicker interfacial layer, this scheme is still recommended due to the much lower leakage current. The reduction of interfacial layer thickness is rendered to surface treatment.

7-3-3 Effect of Surface Treatment

In order to improve the interface properties between HfO_2 and Si interface, some surface treatment methods were employed prior to HfO_2 deposited. In this subsection, HF-treatment, NH_3-treatment, and RTO-treatment were performed and compared. The C-V characteristics of MIS-C with different surface treatment are shown in Fig.7-10, where the HfO_2 film was deposited at the condition of T=400℃, O_2 flow rate=300sccm, and pressure=3 mbar. No PDA was performed. The C-V curves of NH_3-treatment sample and RTO-treatment sample show less distortion than that of HF-treatment sample. This result indicates that the previous two treatments result in less interface states. From the shape of the distorted C-V curves, the interface states are attributed to donor-like interface states. Although the NH_3-treatment sample has higher accumulation capacitance than the RTO-treatment samples, the NH_3-treatment sample shows more sever hysteresis phenomenon than the RTO-treatment sample due to higher tensile stress between the SiN_x and silicon substrate [15]. It should be note that the RTO-treatment sample shows negligible hysteresis phenomenon. The major drawback is low accumulation capacitance which compiles thicker interfacial layer.

Fig.7-11(a) and (b) show the current density versus PDA temperatures in N_2 and O_2 ambient, respectively. The RTO-treatment samples show the lowest leakage current and the HF-treatment samples show the highest leakage current among the three different surface treatment methods. It is postulated that the RTO-treatment forms a high quality interfacial layer, which results in low accumulation capacitance together with low leakage current. The HF-treatment samples should have similar interfacial layer thickness as the RTO-treatment samples because of the same accumulation capacitance. However, the poor quality of interfacial layer results in the highest leakage current among the three treatment methods.

In Fig.7-11(a), it is observed that the leakage current increases with the increase of PDA temperature from room temperature to 800℃. This phenomenon is consistent with the published results and is explained by the crystallization of the HfO_2 film [16]. As the PDA temperature is higher than 800℃, the leakage current decreases. It is quite possible to be due to the increase of interfacial layer thickness because the accumulation capacitance decreases

greatly. Micro-structural analysis will be shown and discussed in the next chapter. The temperature beyond which the leakage current decreases with PDA in O_2 ambient reduces to 700℃. This result implies that the interfacial layer growth in O_2 ambient is much faster than that in N_2 ambient.

Similar results can be observed on poly-Si gate devices. Fig.7-12 compares the leakage current of HfO_2 deposited at 400℃ and 500℃ followed by a 600℃ PDA in N_2 ambient. The O_2 flow rate is 500sccm and the deposition pressure is 5mbar. The magnitude of leakage current is still in the sequence of RTO-treatment < NH3-treatment < HF-treatment. Another interesting phenomenon is that the leakage current of 500℃ deposited samples is lower than that of 400℃ deposited samples by a factor of 5 orders of magnitude. Furthermore, the effect of surface treatment becomes less pronounced as the HfO_2 film is deposited at 500℃. The effect of deposition temperature will be investigated in the next subsection and the mechanism will be proposed in chapter 4.

Based on the results shown from Fig.7-10 to Fig.7-12, a tradeoff between interface quality and CET exists. One possible method to improve the interface quality of the NH_3 treatment sample is adding a N_2O annealing after NH_3-treatment to convert the interfacial layer from nitride to oxy-nitride. Fig.7-13 shows the magnitude of hysteresis of NH_3-treatment samples wafer with post treatment annealing (PTA) at 600℃ and 800℃ in N_2O ambient for 30sec. The HfO_2 film was deposited at 400℃ with O_2/N_2O gas flow ratio rate of 250sccm/250sccm and pressure of 5 mbar. It is observed that an 800℃ PTA reduces the hysteresis phenomenon effectively. For the samples without PTA, high temperature PDA can still reduce the hysteresis effectively. It is summarized that by converting the interfacial layer from nitride-liked layer to another type interfacial layer such as oxide-liked layer, the hysteresis phenomenon can be reduced. The high hysteresis of samples with 600℃ PTA and 750℃ PDA cannot be explained now. It might be due to some process errors.

Fig.7-14 shows the leakage current density and CET of the samples with PTA. Although PDA can improve hysteresis phenomenon and reduce leakage current, the cost is the increase of CET, which is unacceptable for nano-scaled CMOS devices. Better surface treatment method must be developed. Before that, NH_3-treatment was employed in the following subsections to study the HfO_2 film properties.

7-3-4 Effect of Deposition Temperature and Ambient

As has been shown in Fig 7-12, HfO_2 deposited at higher temperature shows lower

leakage current. In this subsection, the effect of deposition temperature and deposition ambient was investigated systematically. About 6 nm thick HfO_2 film was deposited at temperatures of 345℃, 400℃, and 500℃ in pure O_2 ambient (500sccm), O_2/N_2O mixed ambient (250/250sccm), and pure N_2O ambient (500sccm) on NH_3-treatment wafers. The deposition pressure was kept at 5 mbar.

Fig.7-15 shows the current density at -1V and CET versus deposition temperatures at different deposition ambient before PDA. The CET of HfO_2 deposited at T=500℃ in pure N_2O ambient is not shown in this figure because the leakage current is too large to measure correct C-V curve. The CET values of all deposition conditions are similar. However, the effect of deposition ambient on leakage current is significantly different with increasing deposition temperature, especially at high deposition temperature. In oxygen-contained deposition ambient, the leakage current decreases with the increase of deposition temperature, while in pure N_2O ambient the trend is reversed. Although the CET values are similar, the leakage current of HfO_2 film deposited in pure oxygen ambient is lower than that deposited in O_2/N_2O mixed ambient, especially at high deposition temperature. Adding N_2O gas reduces the deposition rate at all temperatures. Pure N_2O ambient has the lowest deposition rate but the highest leakage current.

Fig.7-16 and 7-17 show the current density and CET values, respectively, of HfO_2 films deposited at different temperatures and ambient on NH_3-treatment samples versus PDA temperatures. For HfO_2 films deposited in pure O_2 ambient (Fig.7-16(a)) at 345 and 400 ℃, the leakage current increase with the increase of PDA temperature at first and then decreases with the increase of PDA temperature. This trend is similar to that shown in Fig.7-12. However, for HfO_2 film deposited at 500 ℃, the leakage current decreases with the increase of PDA temperature monotonically. This is a quite different trend that has never been reported. On the other hand, the CET values decrease slightly after 600 ℃ PDA and then increases with the increase of PDA temperature as shown in Fig.7-17(a). The mechanism of the change of CET values will be explored in the next chapter. What important to be highlighted here is that the CET values of HfO_2 film deposited at different temperature are similar while the leakage current has orders of magnitude difference. Thus, another mechanism other than interfacial layer thickness must be proposed to explain this phenomenon.

For HfO_2 films deposited in O_2/N_2O mixed ambient (Fig.7-16(b)), convex shaped leakage current versus PDA temperature was observed at all of the three deposition temperatures. The leakage current is higher even if the CET is similar or larger than that of

films deposited in pure O_2 ambient, especially for the 500 ℃ deposited films. The HfO_2 film deposited in pure N_2O ambient shows even higher leakage current in Fig.7-16(c). To summarize, higher deposition temperature and purer O_2 ambient is benefit to the leakage current performance. The mechanism is not related to the interfacial layer thickness.

Fig.7-18 compares the electrical properties of HfO_2 films deposited at 500℃ with O_2 flow rate of 500 sccm on NH_3-treated and HF-treated wafers. The HF-treatment results in thicker CET but similar leakage current density. Again, the leakage current is dominated by the HfO_2 film itself.

7-3-5 Effect of O_2 Flow Rate

From the above results, HfO_2 deposited at higher temperature in pure oxygen ambient has better electrical properties. In this subsection, the effect of O_2 flow rate was examined. Fig.7-19(a) and (b) show the C-V characteristics and the leakage current at –1V versus PDA temperature, respectively, of the HfO_2 films deposited at 500℃ with different O_2 flow rates on HF-treated wafers. The film deposited with low O_2 flow rate shows severely distorted C-V characteristic. The leakage current density of samples deposited with high O_2 flow rate is lower than that with low O_2 flow, too. The deposition temperature plays the same role at low O_2 flow rate as at high flow rate. Fig.7-20 shows the leakage current at -1V versus PDA temperature. The deposition parameters are the same as those used in Fig.7-15 except that the deposition ambient is pure O_2 at flow arte of 300 sccm. The lower the deposition temperature is, the higher the leakage current density is. These results indicate that higher O_2 flow rate, i.e. sufficient O_2 supply in reaction ambient, and higher deposition temperature, i.e. sufficient decomposition of Hf-precursor, are necessary to deposit high quality HfO_2.

7-4 Summary

In this chapter, electrical characteristics of HfO_2 films deposited at various deposition conditions were investigated. Several important phenomena were observed and summarized as follows.

1. Metals with heat of formation of metal oxides higher than that of HfO_2 is not preferred to be used as gate electrode. For example, Al will react with HfO_2 to form Al_2O_3 interfacial layer during Al deposition and poly-Si may react with HfO_2 during dopant activation annealing. Both Pt and Ta-Pt alloy have inert chemical properties and can be used as gate electrode to study the characteristics of HfO_2 film.

2. The gas injection sequence affects the formation of interfacial layer at HfO_2/Si interface. In comparison with the Hf-first scheme, the O_2-first scheme results in thicker CET, which accounts for thicker interfacial layer. However, this scheme is still recommended due to the much lower leakage current. To reduce CET to meet the requirement of sub-65nm devices, suitable surface treatment and post deposition processes must be developed.
3. Surface treatment affects the growth of interfacial layer and thus affects the electrical properties. The magnitude of leakage current is in the sequence of RTO-treatment < NH_3-treatment < HF-treatment. NH_3-treatment results in the thinnest CET among the three surface treatment methods. However, the hysteresis phenomenon of NH_3-treatment sample is severer than that of the RTO-treatment samples apparently.
4. Post surface treatment annealing in N_2O ambient or post deposition annealing in N_2 or O_2 ambient can improve the hysteresis problem but the cost is the increase of CET. Within the experimental conditions in this chapter, it is suggest that in terms of the best interface properties and the lowest leakage current density, RTO-treatment is the best choice. However, to achieve the thinnest CET, NH_3-treatment becomes the most promising method.
5. Higher deposition temperature and purer O_2 ambient is benefit to the leakage current performance under the same CET. By adding N_2O gas, the deposition rate is reduced and the leakage current is increased. As the deposition temperature increases to 500℃, the surface treatment and post deposition annealing temperature play minor role on the leakage current.
6. Higher O_2 flow rate supply more sufficient O_2 in reaction chamber is also important deposit high quality HfO_2.
7. According to the above results, the best deposition conditions are recommended as : surface treatment:NH_3-treatment, deposition temperature:500℃, deposition ambient:pure O_2 ambient, O_2 flow rate:500sccm, bas pressure:5mbar.

The leakage current density and the corresponding CET value published in literature are summarized in Fig.7-21 [16-21]. The specifications for high performance application, low standby power application as well as DRAM application are also indicated in the figure [16-21]. The best results of this work are indicated as the red rectangle. Although CET value in this work is not low enough, the leakage current is lower than the published results at the similar CET range. The thinnest CET obtained in this chapter is around 2.5nm, which is too

thick for sub-65nm devices. Reduce the as-deposited HfO_2 thickness and improve surface treatment are expected to further reduce the CET to around 1nm. In this chapter, only the measured electrical properties are presented. In the next chapter, detailed micro-structure analysis will be performed to explain the mechanisms.

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Table 7-1. Material properties of HfO_2, ZrO_2, and Al_2O_3 [22].

Aspect	Property		
	HfO_2	ZrO_2	Al_2O_3
Band-gap(eV)	5.68	5.16	8.3
Barrier height to Si(eV)	1.6	1.5	2.9
Dielectric constant	25~40	~25	8~10
Dielectric strength (MV /cm)	2~4.5		>1.0
Heat of formation (Kcal/mol)	271	261.9	399
ΔG for reduction (Si+Mox→M+SiOx)	47.648	42.326	64.39
Thermal expansion coefficient ($10^{16}K^{-1}$)	5.3	7.01	6.7
Lattice constant (Å) (5.43 Å for Si)	5.11	5.1	4.7~5.2
Self diffusion coefficient @ 900℃	$2.8227x10^{-17}$	$6.0009x10^{-10}$	$1.5048x10^{-7}$

Table 7-2. Comparison of Deposition Techniques: MOCVD, Sputtering & ALCVD

MOCVD
Adv.: * Commercial used * Good conformality * Excellent control of dielectric composition
Disadv: * C, H, OH impurities contamination * Precursor

Sputtering
Adv: * Good for evaluating new materials
Disadv: * Poor conformality, especially for high aspect ratio * Purity of target is a concern * Plasma induces damage is a concern

ALCVD
Adv: * Dielectric thickness control * Excellent step coverage * Dielectric composition control
Disadv: * Chlorine-based precursor caused chamber corrosion * Air and moisture sensitive precursor.

Table 7-3. Experimental split conditions of MIS.

.**Methods of surface treatment:**	
HF last	HF solution with HF / H_2O = 1/100
NH_3	800℃ 60min in LPCVD
$NH_3 + N_2O$	800℃ 60min (LPCVD) + 600℃ or 800℃ 30sec (RTA)
RTO	800℃ 30sec O_2 ambient + 1000℃ 30sec N_2 ambient

Thin film deposition conditions:	
Temperature	345℃ , 400℃ and 500℃
Pressure	1.5mbarr, 3mbarr and 5mbarr
Reaction gas	O_2, N_2O and O_2 / N_2O mixed gas
Reaction gas flow rate	300sccm and 500sccm

Gate electrodes:	
Aluminum	Thermal evaporation (500nm)
Pt	E-beam evaporation (100nm)
Poly-Si	LPCVD (200nm) with 20keV 3E15 As implantation
Ta-Pt	Co-Sputter (100nm)

Post deposition annealing:	
N_2 ambient	As-dep., 600℃, 750℃ and 1000℃ for 30sec
O_2 ambient	As-dep., 600℃, 750℃ and 1000℃ for 30sec

? = Not a solid at 1000K

¦ = Radioactive

(1) = Failed reaction Si + MO_x → M + SiO_2

(2) = Failed reaction Si + MO_x → MSi_x + SiO_2

(3) = Failed reaction Si + MO_x → M + MSi_xO_y

? H																	? He
Li	Be											? B	? C	? N	? O	? F	? Ne
(1) Na	Mg											Al	Si	? P	? S	? Cl	? Ar
? K	Ca	Sc	(2) Ti	(1) V	(1) Cr	(1) Mn	(1) Fe	(1) Co	(1) Ni	(1) Cu	(1) Zn	(1) Ga	(1) Ge	? As	? Se	? Br	? Kr
? Rb	Sr	Y	Zr	(1) Nb	(1) Mo	¦ Tc	(1) Ru	(1) Rh	(1) Pd	? Ag	(1) Cd	(1) In	(1) Sn	(1) Sb	(1) Te	? I	? Xe
? Cs	(3) Ba	£	Hf	(1) Ta	(1) W	(1) Re	(1) Os	(1) Ir	? Pt	? Au	? Hg	? Ti	(1) Pb	(1) Bi	¦ Po	¦ At	¦ Rn
¦ Fr	¦ Ra	¥	¦ Rl	¦ Ha	¦ Sa	¦ Ns	¦ Hs	¦ Mt									

La	Ce	Pr	Nd	¦ Pm	(1) Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
¦ Ac	¦ Th	¦ Pa	¦ U	¦ Np	¦ Pu	¦ Am	¦ Cm	¦ Bk	¦ Cf	¦ Es	¦ Fm	¦ Md	¦ No	¦ Lr

Fig.7-1. Metal oxides thermodynamically stability in direct contact with silicon [23].

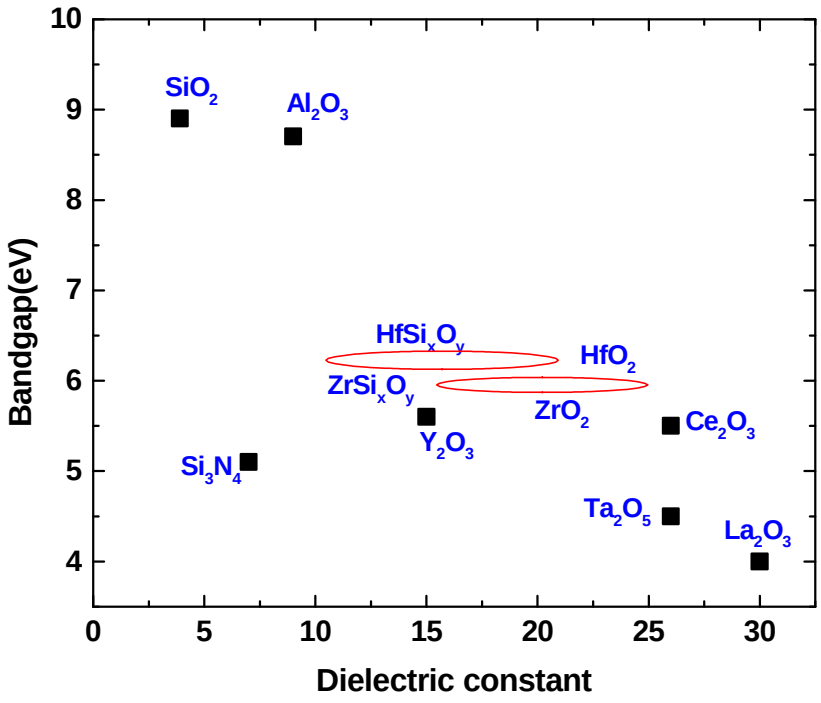


Fig.7-2. Correlation of dielectric constant and bandgap of some high dielectric constant dielectric candidates.

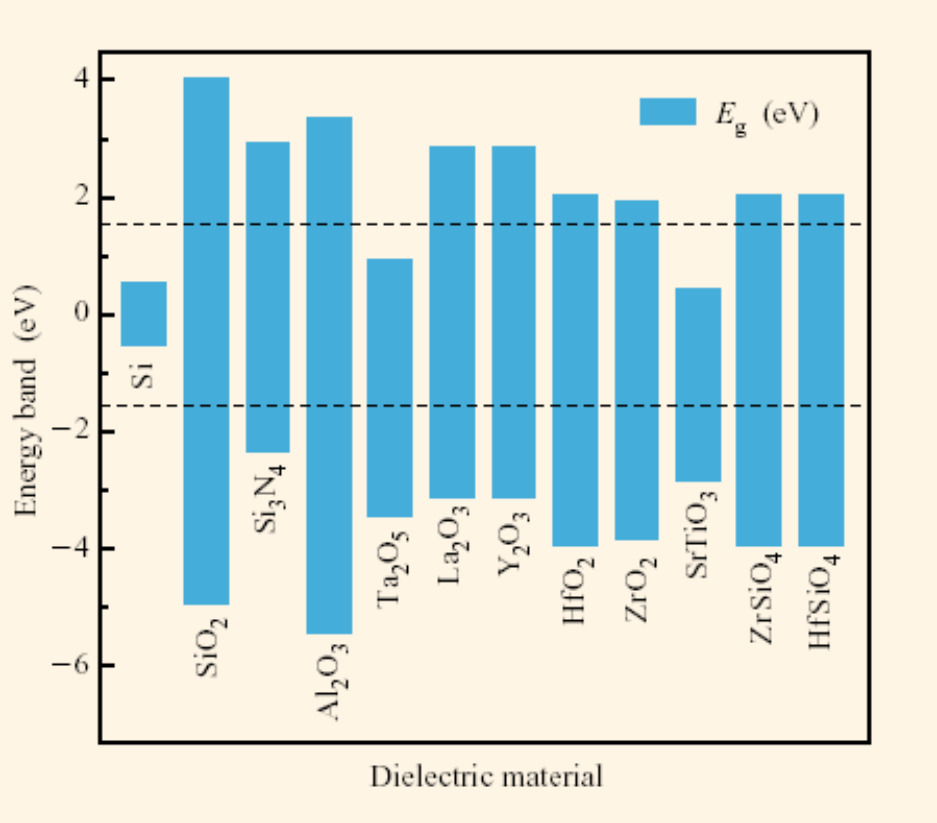


Fig.7-3. Bandgap and band alignment of high-k dielectric with respect to silicon. The dash line represents 1eV above/below the conductive/valence bands

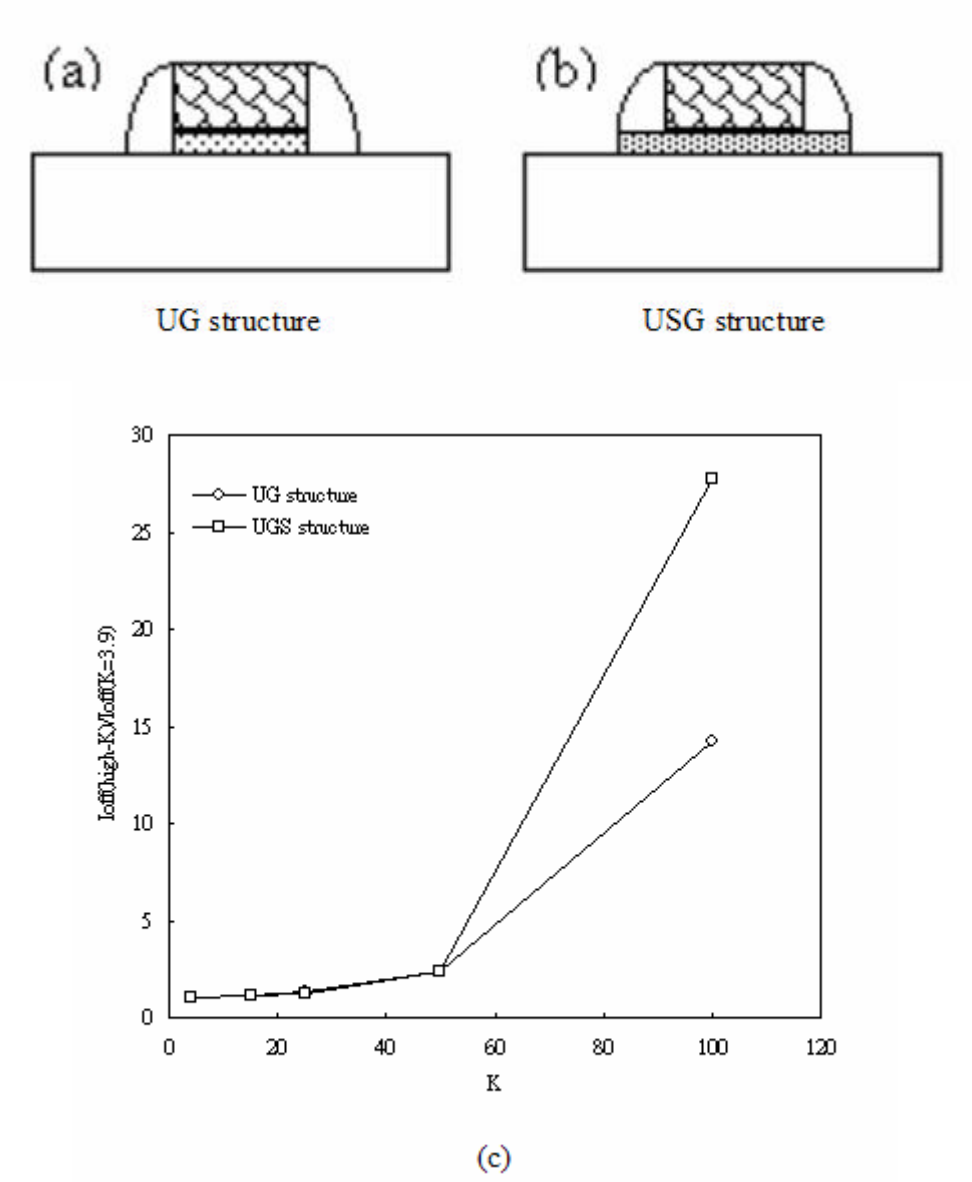
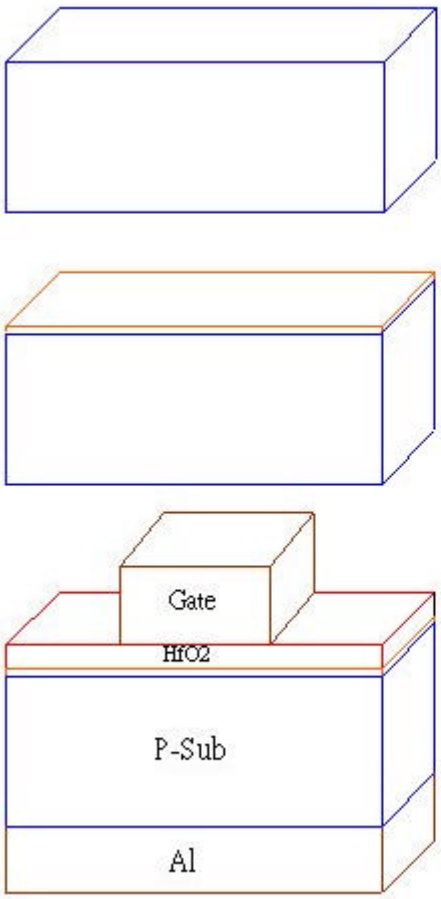


Fig.7-4. (a) UG structure, (b) USG structure, and (c) Comparison of I_{off} versus dielectric constant in UG and USG structure.



- ✓ P-sub RCA clean
- ✓ Surface treatment
  (HF-dip, RTO, or NH_3 treated)
- ✓ Deposited HfO_2
- ✓ Post deposition annealing
- ✓ Gate electrode deposition and patterned
  - ■ Metal gate : lift-off
  - ■ Poly-Si : lithography & etch
- ✓ Backside aluminum

Fig.7-5. Fabrication process flow of MIS-C structure.

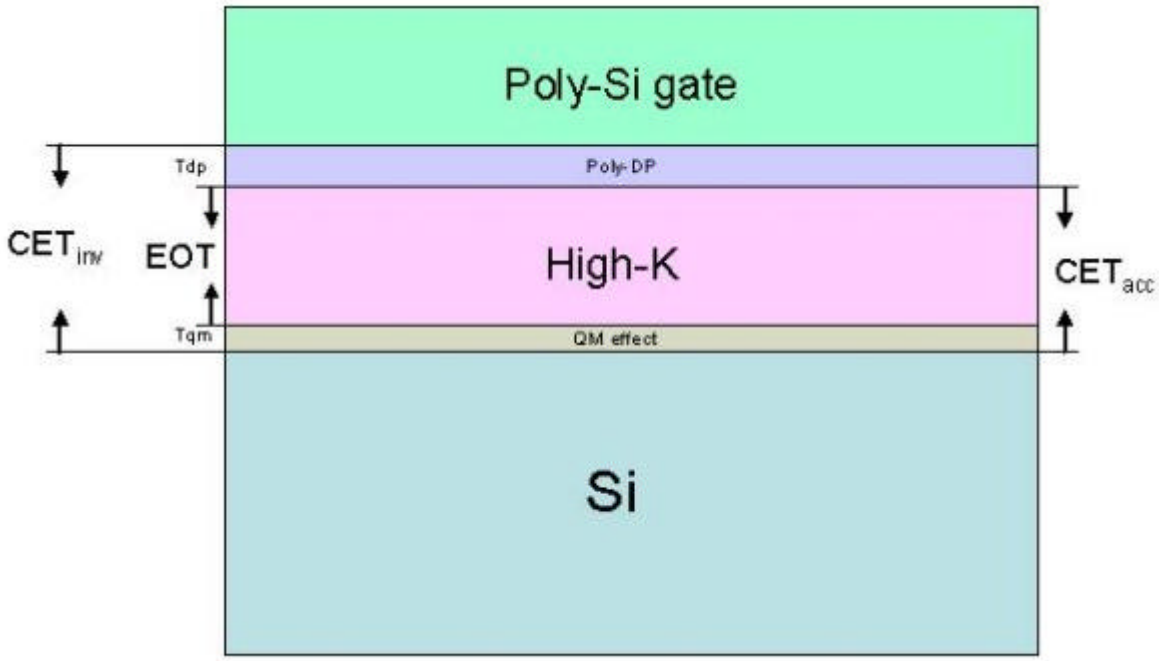


Fig.7-6. Definition of equivalent oxide thickness (EOT) and capacitance equivalent thickness (CET).

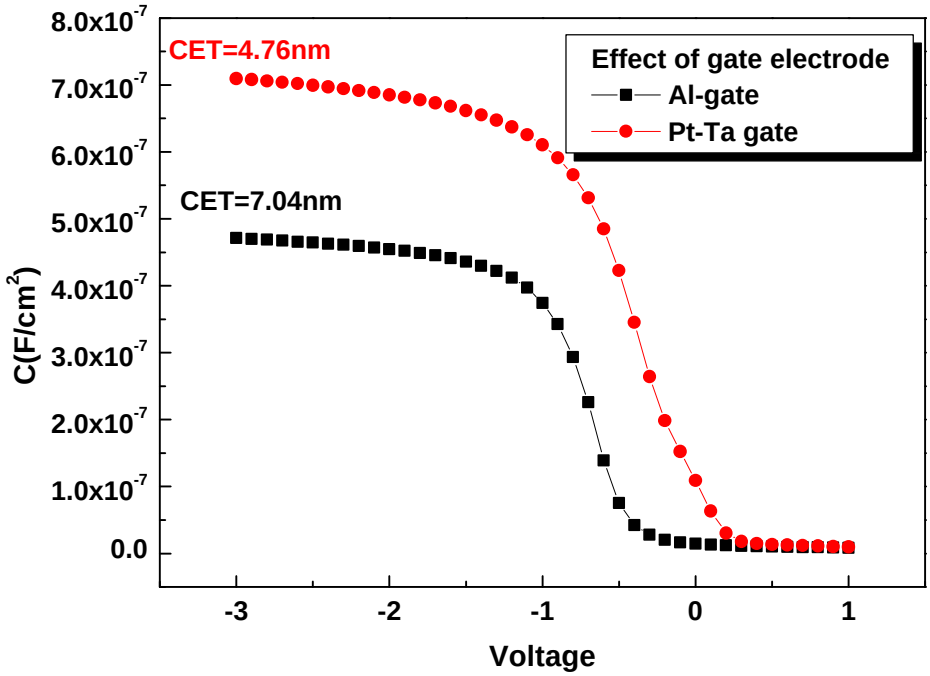


Fig.7-7. Current-Voltage characteristics of Al gate and Ta-Pt gate MIS structure.14nm HfO_2 was deposited on HF-last Si surface. PDA was performed in N_2 RTA system at 600 ℃ for 30sec

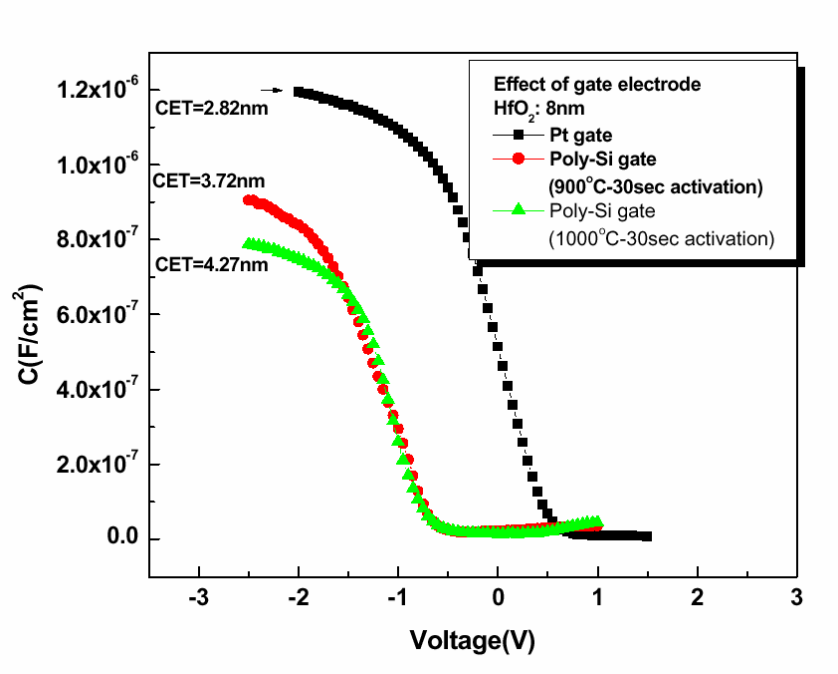


Fig.7-8. Capacitance-Voltage characteristics of Poly-Si gate and Pt gate MIstructure. 8nm HfO_2 was deposited on NH_3-treated Si surface. PDA was performed in N_2 RTA system at 600℃ for 30sec

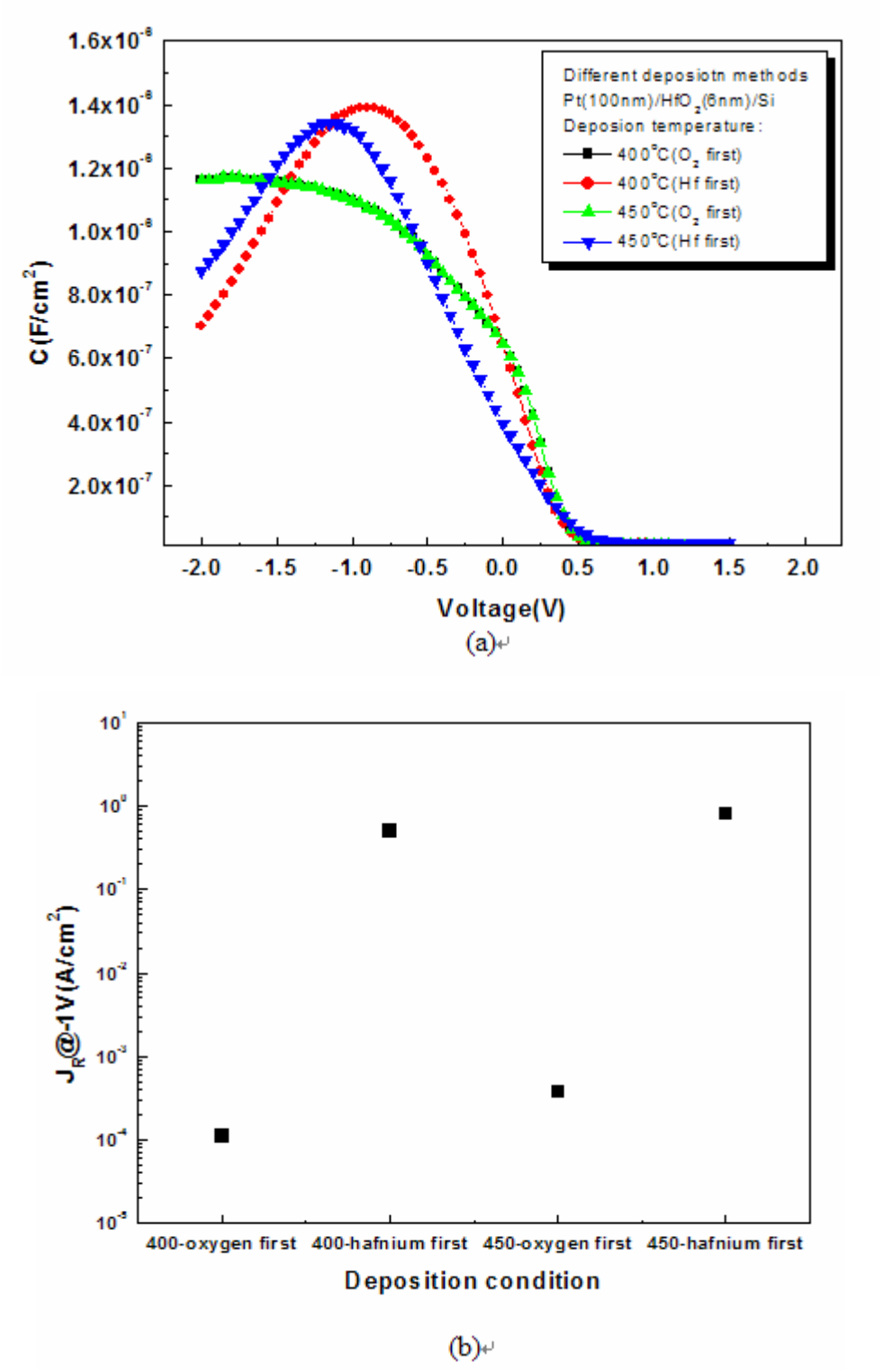


Fig.7-9. (a)C-V characteristics and (b)current density at -1V, of samples with HfO_2 deposited at 400℃ and 450℃. The O_2 flow rate = 300sccm and P = 3mbar.

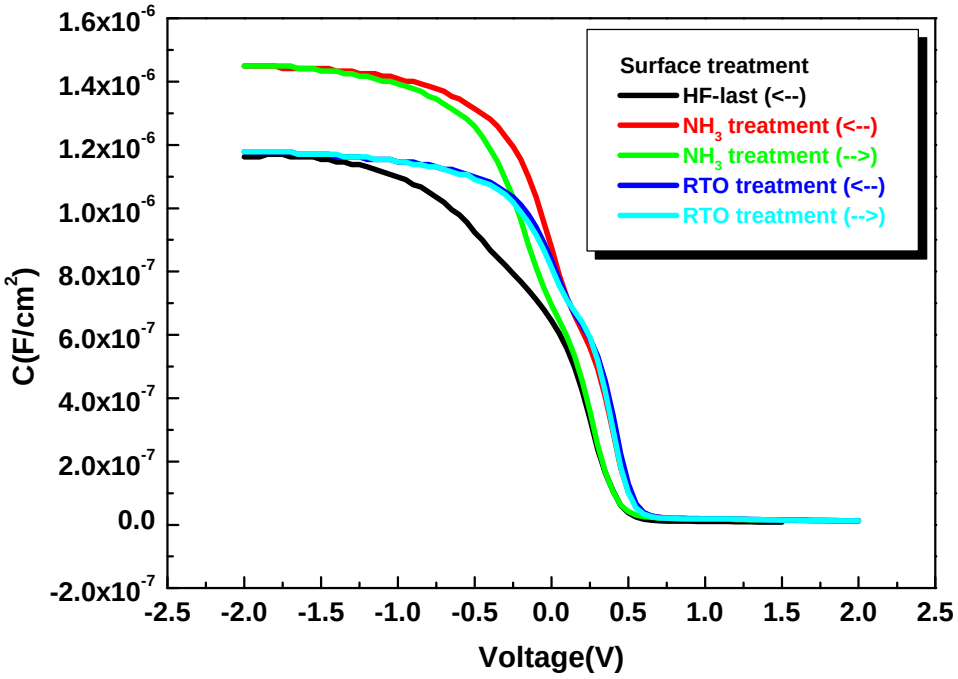
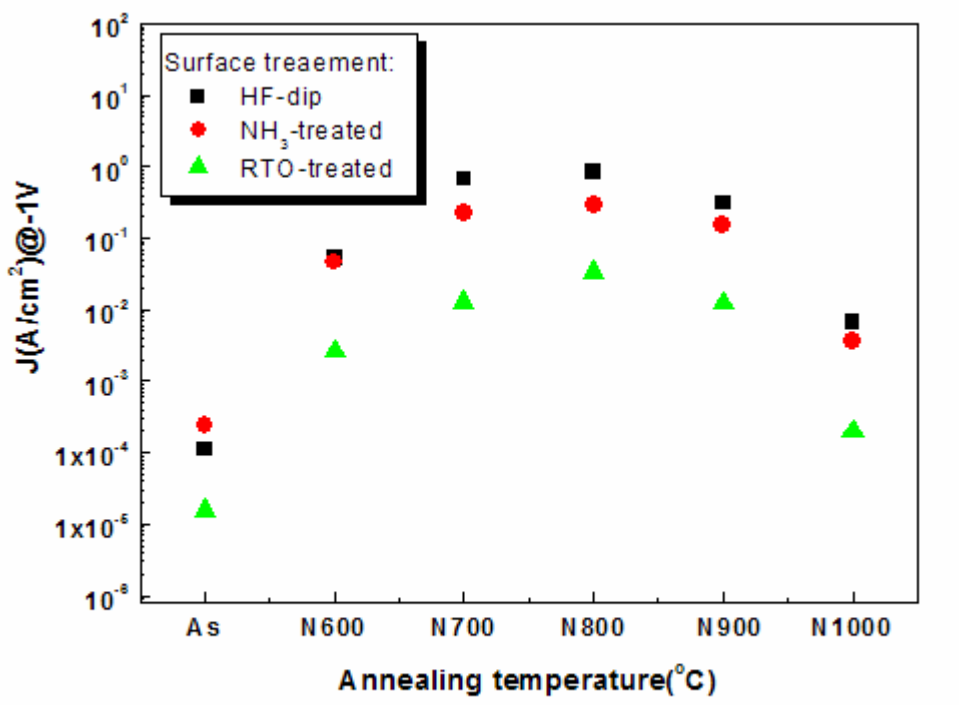
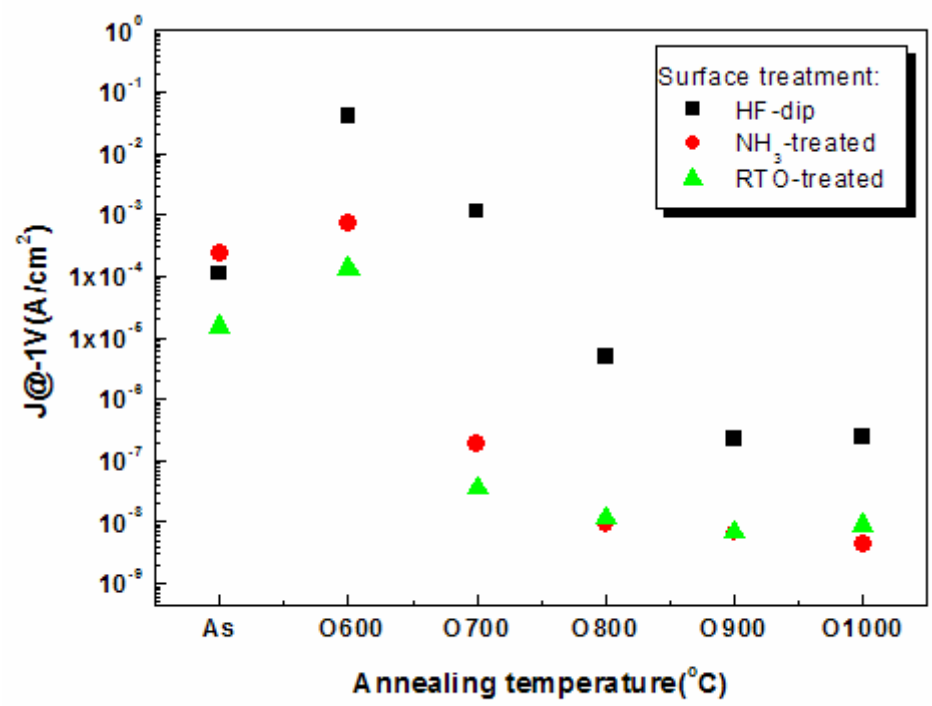


Fig.7-10. C-V characteristics of MIS-C with different surface treatment. HfO_2 was deposited at T = 400℃, O_2 flow rate = 300sccm, and P=3mbar.



(a)



(b)

Fig.7-11. Current density versus PDA temperature in (a) N_2 ambient, and (b) O_2 ambient.

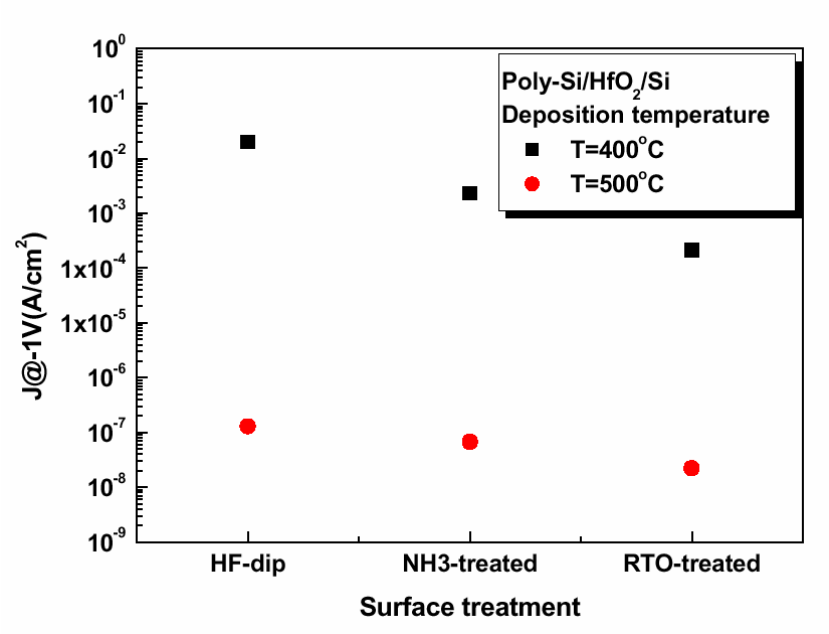


Fig.7-12. Comparison of the leakage current of HfO_2 deposited at T=400℃ and 500℃with different surface treatment substrate. The O_2 flow rate is 500sccm and P=5mbar.

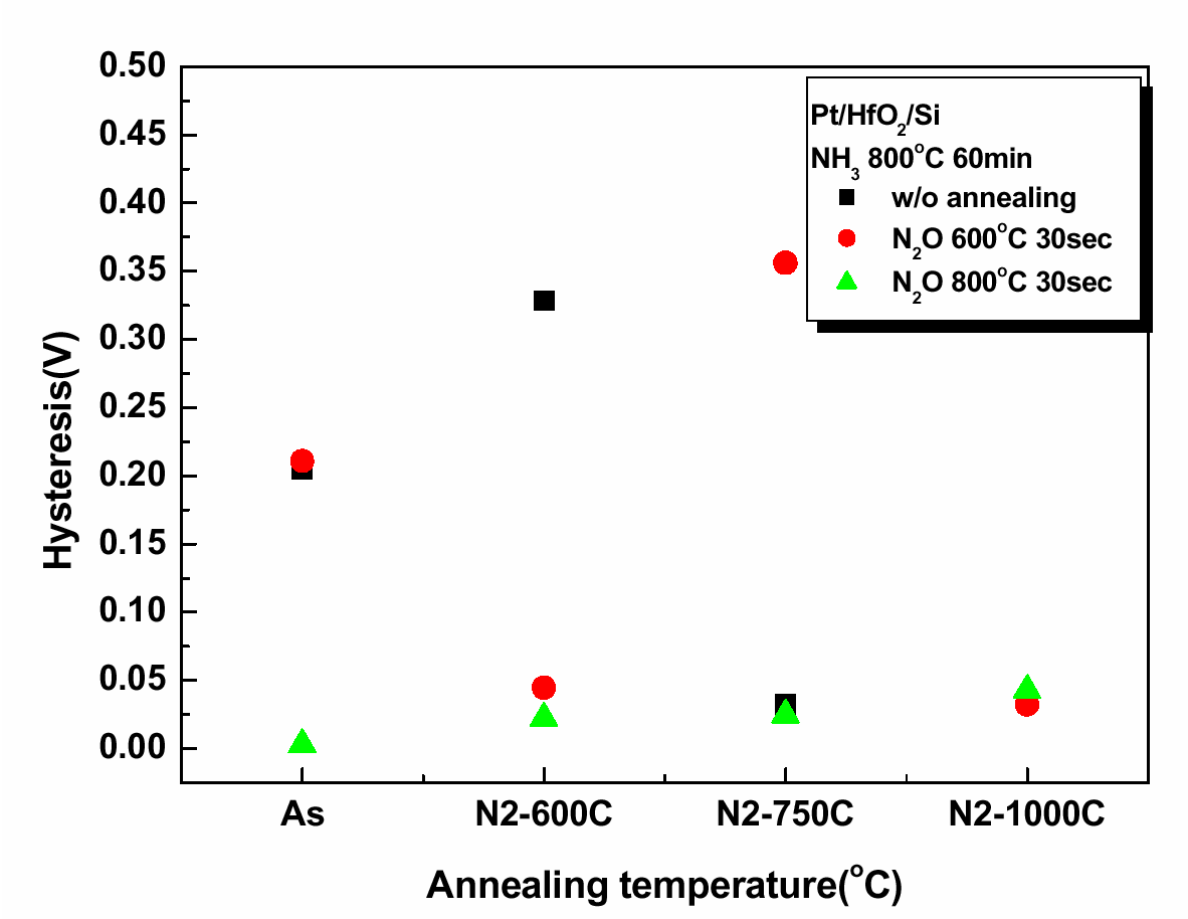


Fig.7-13. The magnitude of hysteresis of NH3-treated samples wafer with post treatment annealing (PDA) at 600℃ and 800℃ in N2O ambient for 30sec.

(Square) LPCVD NH_3 800℃ 60min without annealing

(Circle) LPCVD NH_3 800℃ 60min + RTA N_2O 600℃ 30sec

(Triangle) LPCVD NH_3 800℃ 60min + RTA N_2O 800℃ 30sec

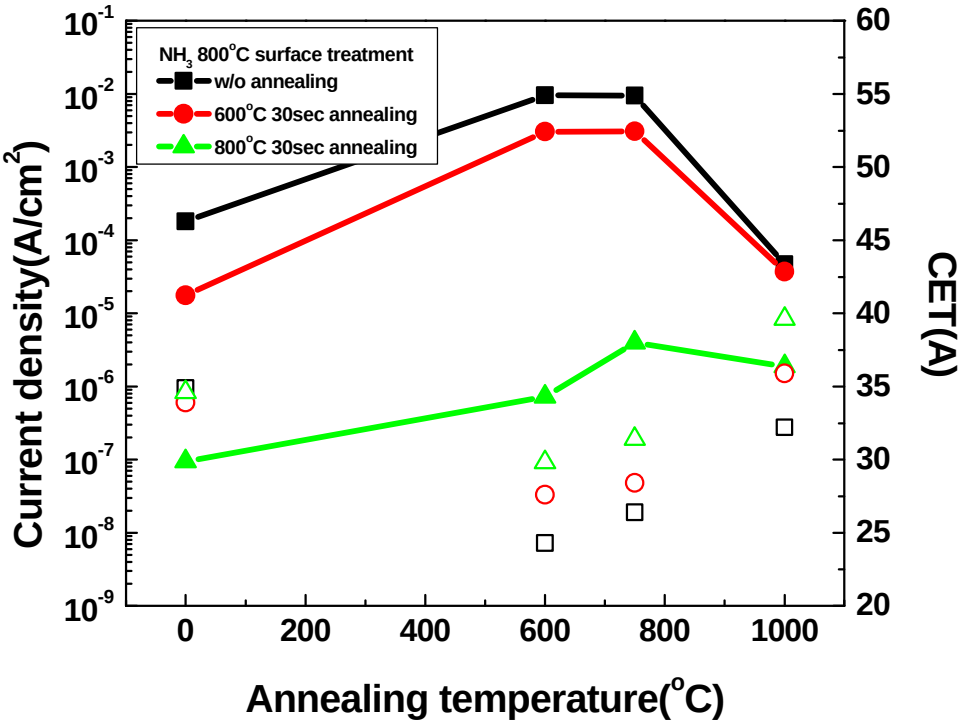


Fig.7-14. The leakage current density and CET of NH_3-treated samples wafer with post treatment annealing (PTA) at 600℃ and 800℃ in N_2O ambient for 30sec.

(Square) LPCVD NH_3 800℃ 60min without annealing

(Circle) LPCVD NH_3 800℃ 60min + RTA N_2O 600℃ 30sec

(Triangle) LPCVD NH_3 800℃ 60min + RTA N_2O 800℃ 30sec

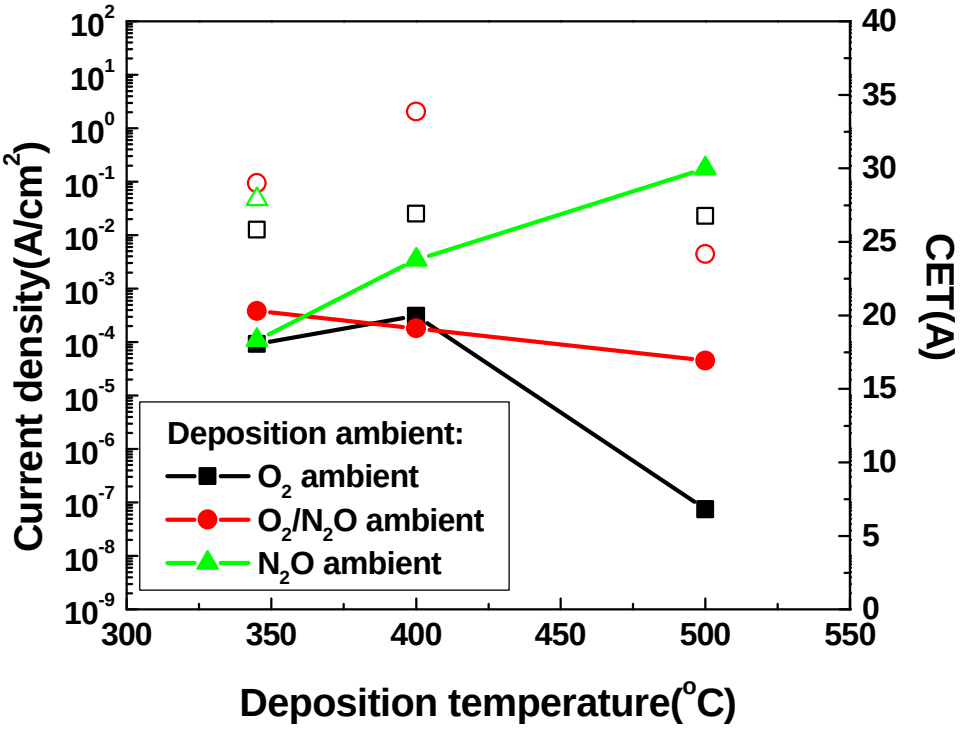


Fig.7-15. The current density and CET versus deposition temperatures at different deposition ambient before PDA.

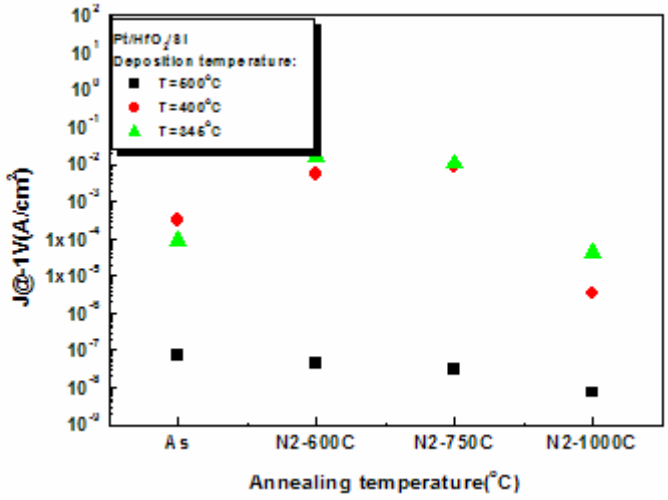
Line : Current density (A/cm^2) , Point: CET (A)

(Square) O_2 = 500sccm

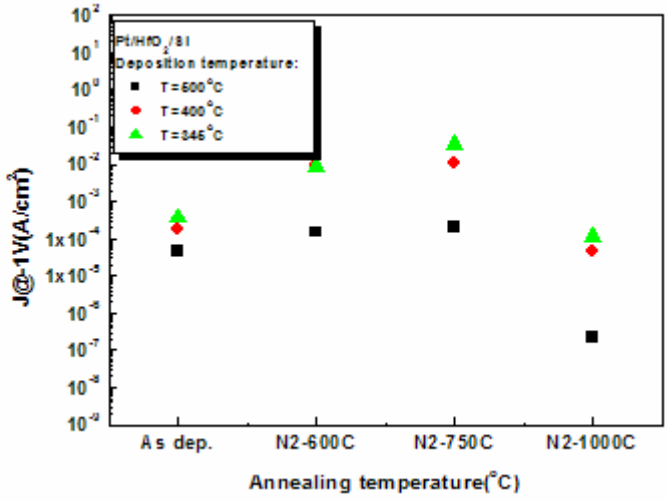
(Circle) O_2/N_2O = 250/250sccm

(Triangle) N_2O = 500sccm

(a) O_2 ambient



(b) O_2/N_2O ambient



(c) N_2O ambient

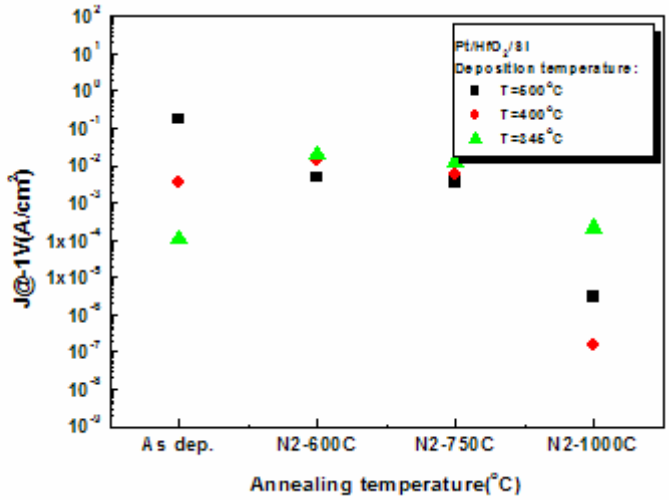
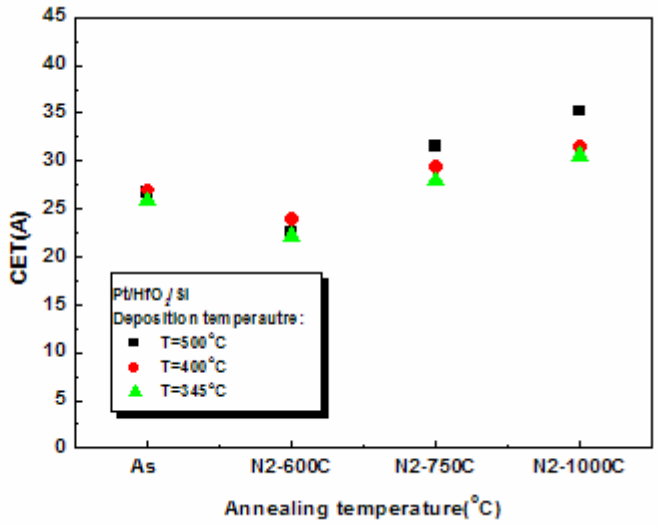
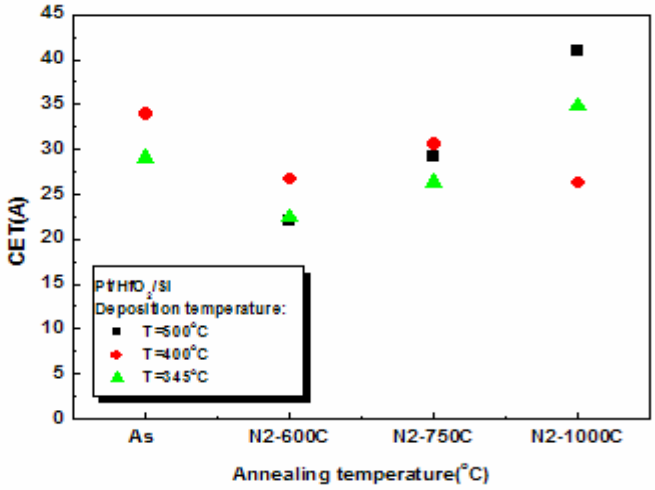


Fig.7-16. Current density of HfO_2 deposited at different temperature and ambient on NH3-treatment samples versus PDA temperature: (a) O_2 ambient, (b) O_2/N_2O ambient, and (c) N_2O ambient.

(a) O_2 ambient



(b) N_2O/O_2 ambient



(c) N_2O ambient

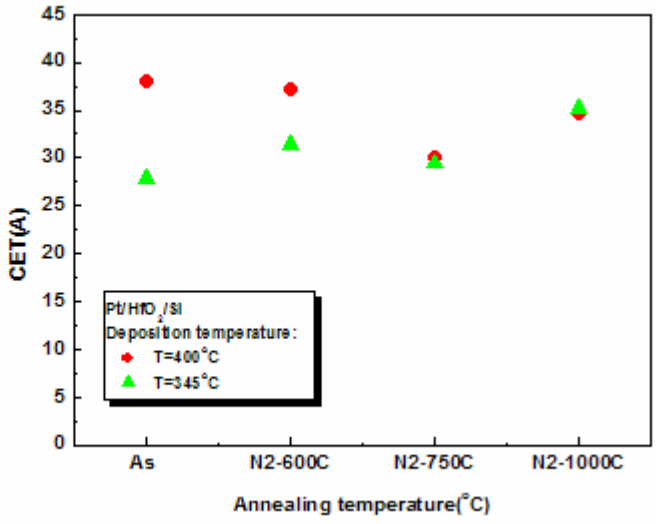


Fig.7-17. CET of HfO_2 deposited at different temperature and ambient on NH_3-treatment samples versus PDA temperature: (a) O_2 ambient, (b) O_2/N_2O ambient, and (c) N_2O ambient.

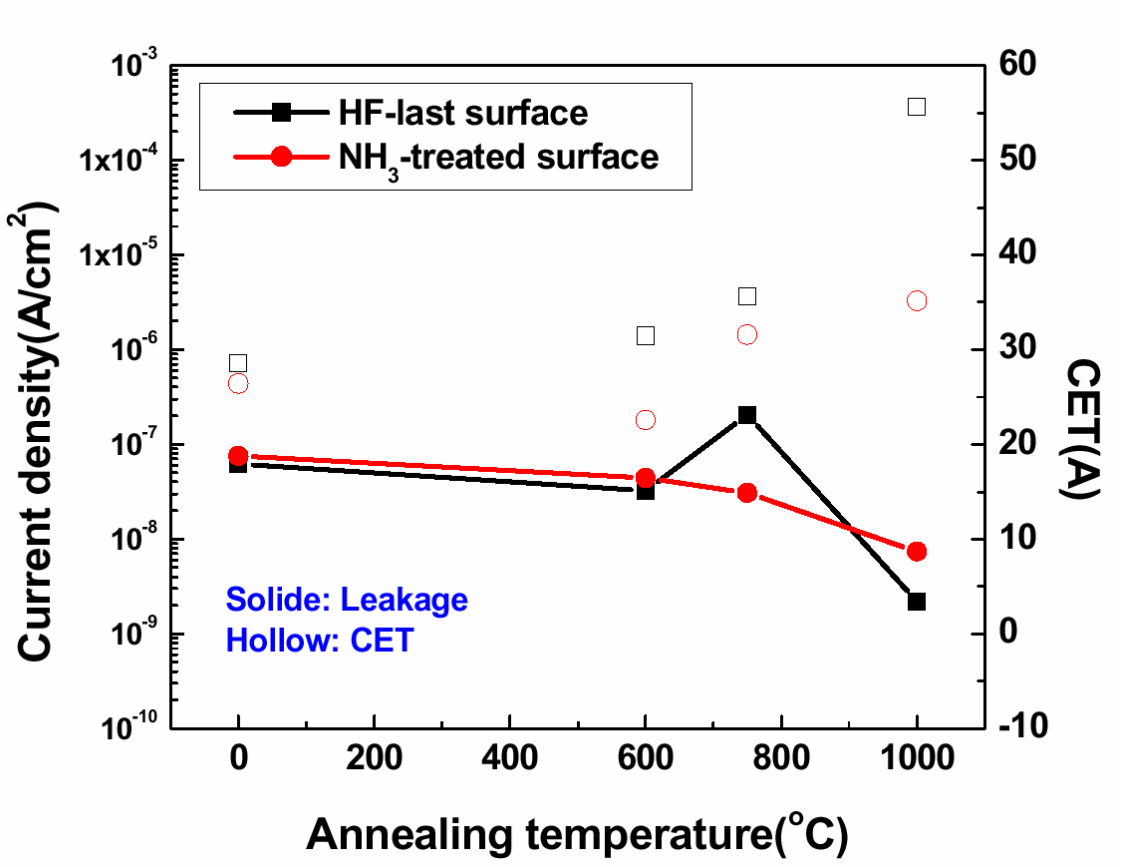


Fig.7-18. Comparison of the electrical properties of HfO_2 film deposited at T=500℃, with O_2=500sccm, P=5mbar on both HF-last and NH_3 treated substrate.

(Square) HF-last surface

(Circle) NH_3 treatment surface

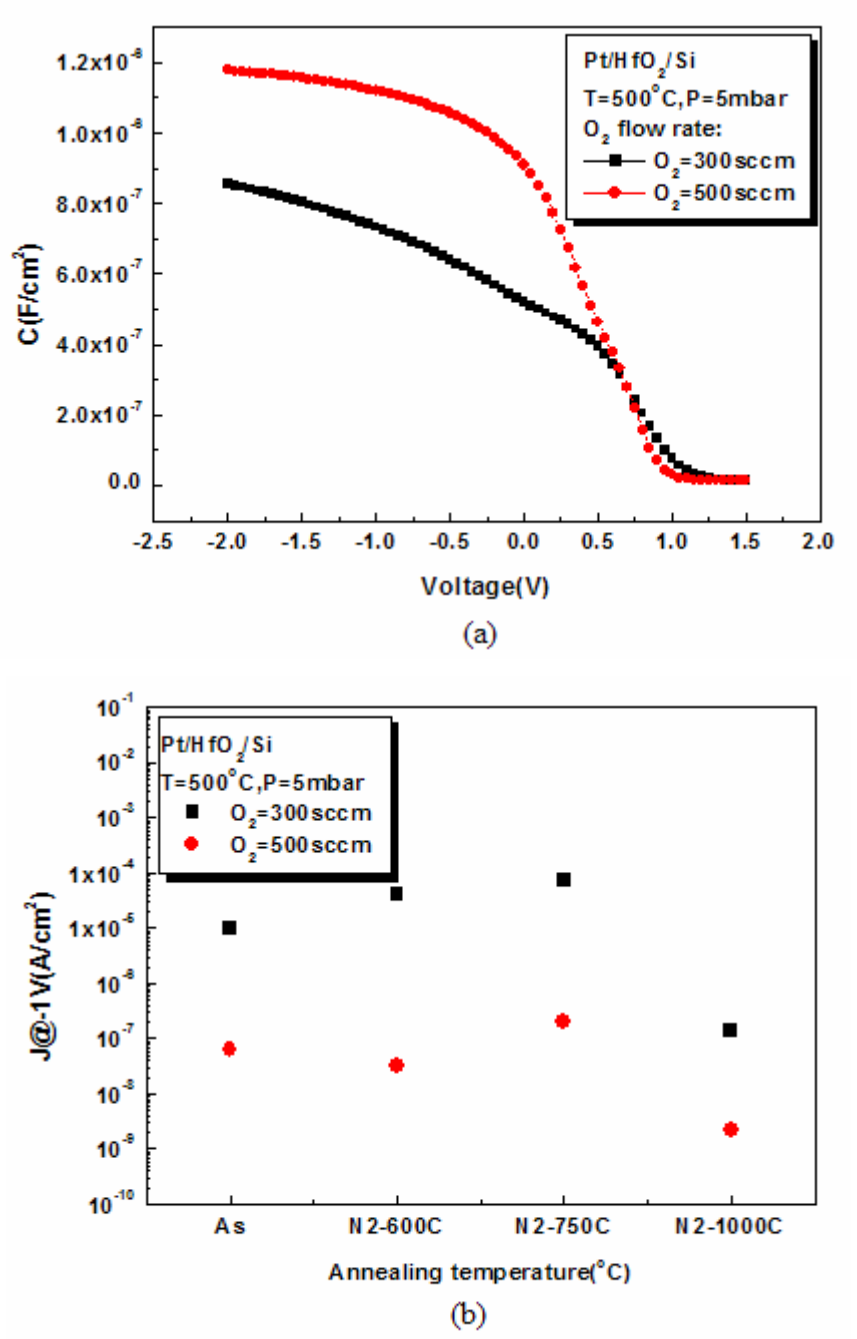


Fig.7-19. (a) C-V characteristics and (b) leakage current at -1V versus PDA temperature of the HfO_2 films deposited at 500℃ with different O_2 flow rate on HF-treated wafers.

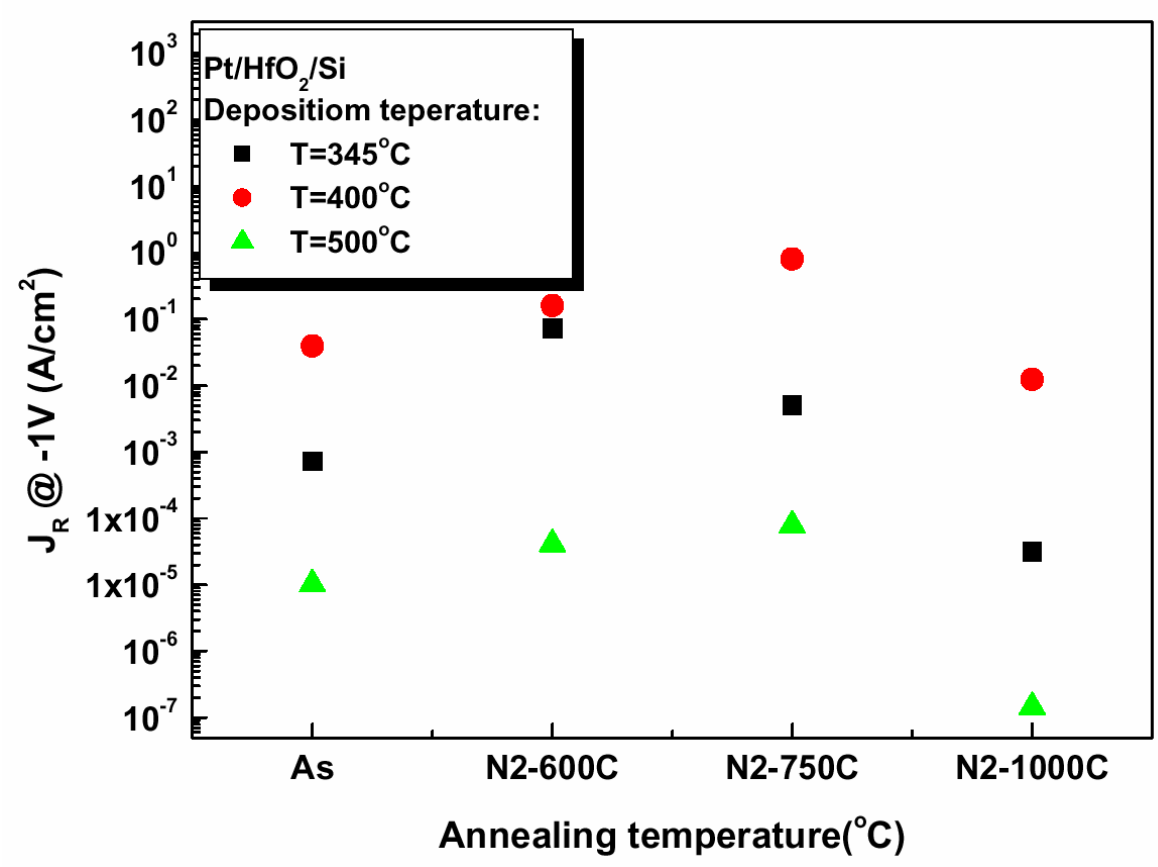


Fig.7-20. Current density versus PDA temperature with HfO_2 deposited at different temperature, with O_2 flow rate = 300sccm, P= 5mbar.

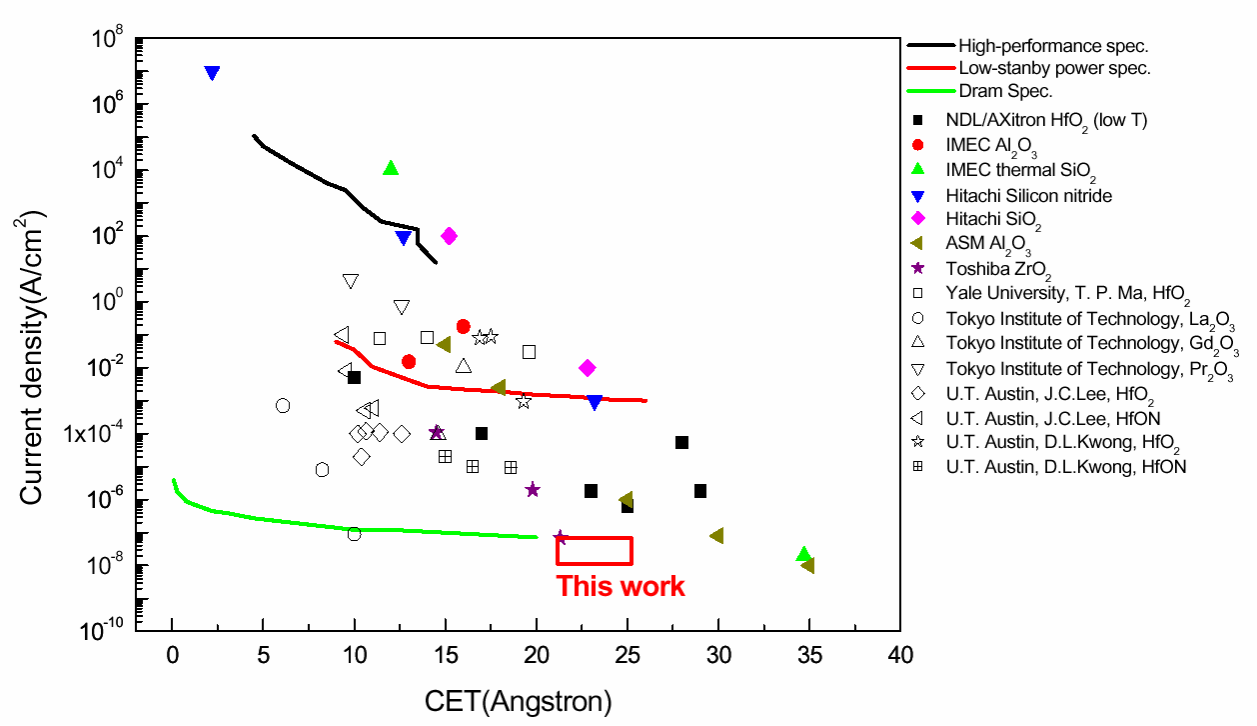


Fig.7-21. Correlation between leakage current density and CET from literature. The best results obtained in this work are indicated as the red square.

Chapter 8
Physical Characteristics of HfO_2 Film Prepared by MOCVD

8-1 Introduction

The electrical properties of HfO_2 films have been discussed in previous chapter comprehensively. Several interesting phenomenon which are different from those reported in literature are found. At first, the leakage current of HfO_2 films deposited at high temperature and high O_2 flow rate is much lower than that deposited at low temperature or low O_2 flow rate. With similar CET value, the leakage current could be significantly different. For the low temperature deposited samples, the leakage current increases but the CET value decreases with the increase of PDA temperature in the medium temperature range (600-800℃). On the contrary, the leakage current of high temperature deposited HfO_2 films decreases monotonically with the increase of post deposition temperature in the whole range. Reducing the O_2 flow rate or introducing N_2O gas during deposition results in high leakage current. In this chapter, physical and chemical analyses techniques including atomic force microscopy (AFM), x-ray diffraction (XRD), transmission electron microscopy (TEM), as well as x-ray photoelectron spectroscopy (XPS) were employed to reveal the microstructures of the HfO_2 films deposited at different conditions. Through these analyses, the factors affecting leakage current are identified and new guideline will be proposed to deposit low leakage current HfO_2 film.

8-2 Material Analysis

8-2-1 Thickness Analysis

Optical measurement has its detection limit on precise thin film thickness determination especially in the case of multi-layer structure with similar optical properties for each layer. The HfO_2/interfacial layer stack structure is one of the examples. Cross-sectional TEM (x-TEM) inspection is the most common and precise method to determine thin film thickness. In this subsection, x-TEM inspection is employed to determine the thickness of the HfO_2 layer and interfacial layer.

Fig.8-1 shows the x-TEM micrographs of samples deposited at 400℃ on HF-treated wafer with various post annealing temperatures in N_2 ambient for 30sec. The O_2 flow rate is

300 sccm and the pressure is 1.5mbar. The measured thickness of HfO_2 layer and interfacial layer are plotted as Fig.8-1(e). The scale is calibrated with the lattice image of the Si substrate. It is observed that the thickness of HfO_2 layer increases after 600℃ PDA and tends to saturate after annealing at higher temperatures. It is postulated that the as-deposited HfO_2 film is metal-rich because the Hf-precursor may not decompose completely at 400℃ so that the HfO_2 layer grows continuously during PDA. Once all hafnium atoms react with oxygen, the HfO_2 film thickness becomes saturated. This postulation will be discussed again in the subsection D.

The thickness of interfacial layer increases with the increase of PDA temperature monotonically. Because HfO_2 is a poor diffusion barrier for oxygen, oxygen may diffuse through HfO_2 layer and reacts with silicon or hafnium atoms to form SiO_2-like or silicate-like interfacial layer during PDA. The increase of HfO_2 layer thickness (from 3.2nm to 4.2nm) is larger than the increase of interfacial layer (from 1.85nm to 2.0nnm) after 600℃ PDA, which explains the decrease of CET as seen in Chapter3 results. Furthermore, the large increase of interfacial layer thickness after 1000℃ PDA accounts for the apparent decrease of leakage current.

Electron probe microanalysis (EPMA) with energy dispersion spectrometer (EDS) was employed to identify the composition of interfacial layer. Fig.8-2 shows the high resolution x-TEM micrograph of the sample deposited at 400℃ followed by a PDA at 1000℃ in N_2 ambient. The positions at where EPMA were performed are indicated on the micrograph. The EDS spectrum at the lower portion of interfacial layer shows significant Hf signal as shown in Fig.8-2(b). Although the spatial resolution of EPMA is not good enough so that the Hf signal may come from the HfO_2 layer, it is still suspected that the interfacial layer is Hf-silicate but not SiO_2 because the Hf signal is very strong.

Fig.8-3 shows the X-TEM micrographs of samples deposited at 400℃ on NH_3-treated wafer. The O_2 flow rate is 500sccm and the pressure is 5mbar. As stated in chapter 2, the thickness of surface layer after NH_3 treatment is 1nm measured by ellipsometry method. Using the Si lattice image as scale, the measured thickness of HfO_2 layer and interfacial layer from the TEM micrographs are plotted as Fig.8-3(d). The phenomenon of apparent increase of HfO_2 layer after PDA shown in Fig.8-1(e) is not observed in this case. It might be due to the sufficient supply of O_2 during deposition and thus the amount of un-reacted Hf is reduced. The increase of interfacial layer with the increase of PDA temperature is confirmed.

Similar results are observed on the samples deposited at 500℃ as shown in Fig.8-4. It should be noted that the thickness of interfacial layer of the 500℃ deposited samples are

similar to that of the 400℃ deposited samples but the leakage current has a difference of several orders of magnitude. This observation concludes that the leakage current reduction of samples deposited at 500℃ can not be explained by the formation of interfacial layer. Another important observation is that the interfacial layer of HfO_2 film deposited on NH_3-treated wafer is thinner than that on HF-treated wafer. This observation implies that the surface treatments used in this thesis are not efficient enough. Therefore, more efficient surface treatment method must be developed to scale-down the CET to sub-1nm regime.

8-2-2 Thin Film Composition

The compositions of HfO_2 layer was analyzed with XPS using the method similar to that used to determine the Si and SiO_2 transition region composition [1]. Both pure Hf and pure HfO_2 powder were prepared. The electron binding energy of Hf in Hf an HfO_2 state can be detected. The electron binding energy of Hf in the deposited HfO_x film was analyzed at the same condition. And then the x value can be interpolated. The calculated results of some samples were shown in Fig.8-5. Most of the samples show x values very close to 2. This result indicates that the stoichiometry of the deposited HfO_2 film is correct. The film deposited in N_2O ambient show lower x value after PDA at higher temperature, this might be due to some Hf-O bonds are replaced by Hf-N bonds so that the content of O in the film is reduced. It is noted here that the electron binding energy of Hf-N is lower than the Hf-O bond. After 1000℃ PDA, the x-value decrease slightly. It might relate to the growth of interfacial layer. Fig.8-6 shows the measured XPS spectrum can be deconvoluted into two spectra. The spectrum corresponding to lower binding energy is related to Hf-silicate [2]. It seems that the samples deposited in N_2O ambient show stronger Hf-silicate than the sample deposited in O_2 ambient. This observation might explain the decrease of x value of the N_2O ambient deposited film after high temperature annealing.

XPS depth profile was also employed to confirm the formation of silicate layer. Fig.8-7 shows the XPS spectrum of $Hf_{4f7/2}$ of HfO_2 film after different surface sputtering time. Since the sputter rate of as-deposited film is much faster than that of the annealed film, the detection position is closer to the interfacial layer for the as-deposited sample. It is clear that as the detection position becomes closer to the interfacial layer, the signal corresponded to HfO_2 (higher energy signal) becomes weaker and the signal corresponded to Hf-silicate (lower energy signal) becomes stronger. All of these analyses indicate that the interfacial layer is silicate-like but not SiO_2-like.

8-2-3 Surface morphology

Surface morphology of HfO_2 films deposited at different temperatures and ambient followed by different post annealing temperatures and ambient were examined by AFM. The thickness of the deposited films are around 6nm~8nm. According to the published literature, rough surface is expected as HfO_2 crystallizing after PDA. Smooth surface is desired since roughness will enhance local electric field, which is believed to be detrimental to the gate dielectric integrity. Fig.8-8(a), (b), and (c) show the AFM images of HfO_2 films deposited at 345℃ without PDA, after 900 ℃ PDA in N_2 ambient, and after 900℃ PDA in O_2 ambient, respectively. The other deposition parameters are O_2 flow rate=300sccm and pressure=1.5mbar. The corresponded root-mean-square roughness (R_{ms}) values are 0.569nm, 0.519nm, and 0.467nm. The low temperature deposited film show large roughness but PDA can slightly improve.

Fig.8-9 shows the AFM images of HfO_2 film deposited at 400℃ with PDA at different temperatures in N_2 ambient. During deposition, the O_2 flow rate was 300 sccm and the pressure was 1.5 mbar. The R_{ms} values are 0.203nm, 0.163nm, 0.178nm, and 0.159nm for the samples without PDA, after 600℃ PDA, after 750℃ PDA, and after 1000℃ PDA, respectively. Fig.8-10 compares the leakage current density at -1V and the CET and R_{ms} values of these samples. It is observed that the surface roughness is irrelevant to the PDA temperature and the high leakage current of the as-deposited and 600℃ annealed samples can not be attributed to surface roughness.

Fig.8-11 shows the AFM images of HfO_2 films deposited at 500℃ in pure O_2 deposition ambient and N_2O deposition ambient. The flow rates of both gases and pressure are 500 sccm and 5 mbar, respectively. The surface of HfO_2 film deposited in N_2O ambient is rougher than that deposited in O_2 ambient. It has been reported that by adding nitrogen into HfO_2 film, the crystallization temperature could be raised [2]. It is thus postulated that the smooth surface of HfO_2 film deposited in N_2O ambient could be attributed to its amorphous nature. However, as has been observed in chapter 2 that the leakage current of HfO_2 film deposited in N_2O ambient is much higher that that deposited in O_2 ambient. It is concluded that the surface roughness does not affect the leakage current again. Before ending this subsection, it should be noted that the R_{rms} value of original Si substrate is around 0.2nm, which is similar to and slightly better than that of the surface of HfO_2 films deposited at 400℃ and 500℃, respectively.

8-2-4 Phase Transformation

In this subsection, grazing angle X-Ray diffraction (G-XRD), planar view TEM inspection, and TEM diffraction were employed to identify the crystalline and micro-structure of the deposited HfO_2 films. Fig.8-12 shows the G-XRD spectra of HfO_2 films of 8nm thick deposited at 345℃, 400℃ and 500℃ without PDA. The O_2 flow rate is 300 sccm and the pressure is 5mbar. For HfO_2 films deposited at 345℃ and 400℃, the intensities of the signals are extremely weak. As a result, it is unlikely to exactly identify the structure of HfO_2 thin films with these broad and weak signals. The only thing can be verified is that the films deposited at low temperature show poor crystalline. However, for the 500℃ deposited film, several diffraction signals can be identified to be HfO_2 phases. It is supposed that the film becomes polycrystalline as deposited at higher temperature because crystalline state is the most stable state of HfO_2 [3].

Fig.8-13(a) and (b) show the XRD spectra of HfO_2 films deposited in O_2 ambient and N_2O ambient, respectively, followed by PDA in N_2 ambient at different temperatures. For the HfO_2 film deposited in O_2 ambient, the as-deposited films show clear HfO_2 orthorhombic crystal structure. As the PDA temperature increases, the signal intensity becomes more and more strong. On the other hand, as deposited in N_2O ambient, the as-deposited film is amorphous type and the crystallization temperature increases to 750℃ as shown in Fig.8-13(b). Fig.8-14 compares the XPS binding energy of N in HfO_2 film. The film deposited in pure O_2 ambient shows weak N-signal where the nitrogen content comes from the Hf-precursor. The N_2O gas incorporate additional N into the HfO_2 film so that the HfO_2 film deposited in N_2O ambient shows stronger N-signal. These observations indicate that nitrogen incorporation in HfO_2 film destroys the HfO_2 structure and then increases crystallization temperature.

The detailed micro-structure was investigated by high-resolution plane-view TEM (PV-TEM) inspection. The PV- TEM micrographs of HfO_2 thin film deposited at 400℃ followed by different PDA temperatures are shown in Fig.8-15. The O_2 flow rate is 300 sccm and the deposition pressure is 1.5mbar. The as-deposited film shows many nano-scale grains (nano-crystals) separated by amorphous state material. The average grain size is 20 nm. After 600℃ PDA, the amorphous region reduces and more nano-crystals are observed. Continuous increase the PDA temperature to 1000℃, nano-crystals merge and the grain size increases to 40 nm.

Fig.8-16(a)-(d) shows the corresponded conductive AFM image. In each figure, the upper half is the surface morphology image and the lower half is the conduction image. The bright points of the conduction image indicate the high conductivity positions, i.e. the leaky

points. The sample without PDA shows some bright points. As the PDA temperature increases to 600 and 750℃, the density of bright points increases dramatically. Comparing the TEM micrographs in Fig.8-15 and the conductive AFM images in Fig.8-16 with the leakage current in Fig.8-10, it is quite reasonable to conclude that the increase of leakage current after 600℃ PDA arises from the crystallization of the HfO_2 film. Because the resolution of AFM image is not high enough, we can not judge whether the leakage path is through the nano-crystals or at the boundary of the nano-crystals. After PDA at 1000℃, the leakage current decreases apparently due to the growth of interfacial layer. The lacking bright points in the conductive AFM image does not mean that the HfO_2 film do not leak after 1000℃ PDA, but reflects the fact that the thick interfacial layer effectively blocks the current transport.

Fig.8-17 shows the PV-TEM micrographs of HfO_2 films deposited at 500℃ in O_2 ambient and N_2O ambient. The O_2 flow rate is 500 sccm and the pressure is 5 mbar. Not similar to the HfO_2 film deposited at 400℃, the film deposited at 500℃ in O_2 ambient shows completely poly-crystalline structure. The grain size of the as-deposited film is 20 nm. The grain size increases from 30 nm to 50 nm as the PDA temperature increases from 600℃ to 1000℃. On the contrary, the HfO_2 film deposited in N_2O ambient shows amorphous nature. Even if after 1000℃ PDA, only few nano-crystals are observed.

It had been reported and widely accepted that crystallization of HfO_2 film will result in high leakage current. And it is assumed that the leakage path is the crystallized grain. Our results on the 400℃ deposited HfO_2 film seems support the explanation. However, if it is true, the HfO_2 film deposited at 500℃ should exhibit the highest leakage current and the films deposited in N_2O ambient should exhibit the lowest leakage current under the same CET. Unfortunately, the leakage current measured in chapter 3 shows totally different results. Therefore, the leakage path can not be the nano-crystals. The most possible leakage path becomes the boundary of the nano-crystals.

Fig.8-18 compares the microstructure of the HfO_2 films deposited at 400℃ and 500℃. The nano-crystals of the 400℃ deposited film are round shape and are surrounded by amorphous region. On the other hand, the nano-crystals of 500℃ deposited film are polygonal shape and contact to each other tightly. It is suspected that the boundary between the amorphous region and the nano-crystals has different composition or structures. This postulation is possible because the impurities in Hf precursor may not decompose completely and can incorporate into the deposited film. During PDA, these impurities are repelled out of the nano-crystals and pile-up at the nano-crystal boundary. Similar mechanism had been approved in many polycrystalline films such as poly-Si or metal silicides. The high impurity

concentration region also stops the growth of nano-crystals. Finally, the nano-crystals are surrounded by an amorphous region and show round shape. Since the major impurity in the film is nitrogen and the compound of HfN is metallic, the boundary of nano-crystals serves as leakage path. At high deposition temperature, for example 500℃, precursor decomposes and Hf reacts with O completely. Nano-crystals grow until they touch with each other. Therefore, nano-crystals contact tightly. The lack of high impurity region of the high temperature deposited HfO_2 film accounts for the low leakage current.

Because the nano-crystals are so small, G-XRD does not provide sufficient resolution to identify the phase and orientation. Fig.8-19 and Fig.8-20 show the TEM diffraction pattern of samples deposited at 400℃ and 500℃, respectively. Although the 400℃ deposited sample exhibit poor crystalline, consistent with G-XRD result, it tends to be polycrystalline after 1000℃ PDA. Classical polycrystalline diffraction pattern is observed in the 500℃ deposited samples. Plenty crystalline structures are observed while XRD only reflects the strongest one.

The actual structure of nano-crystals is identified from the high resolution plane view TEM image. As indicated in Fig.8-21 and 8-22, two d-spaces of diffraction planes as well as the intersection angle could be measured from the two dimensional lattice images, and then the structure of the grain can be identified. Most of the grains are identified as the orthorhombic structural HfO_2. It is worthy to note that XRD signals obey the “selection rule” so that some d-spaces measured from the TEM image may be not found in XRD data sheet

For general comment, amorphous gate dielectric is suitable for device applications due to the lower leakage current, superior heterogeneous interface quality, and better blocking capability against impurity diffusion from poly-Si gate electrode. However, once nano-crystals form in the dielectric film, leakage current increases. Although adding nitrogen into HfO_2 increases the crystallization temperature, high leakage current still occurs due to few nano-crystals. Instead, HfO_2 film with fully crystallized structure, for example deposited at 500℃ and O_2 flow rate 500sccm (i.e. high deposition temperature with sufficient oxygen supply), show the lowest leakage current among the HfO_2 films studied in this thesis.

8-3 Summary

In this chapter, material and microstructure analyses are performed to investigate the microstructure of the deposited HfO_2 film and to explain the electrical characteristics observed in chapter 2. The film thickness is examined at first. For the film deposited at low temperature or with insufficient O_2 supply, not decomposed Hf-precursor incorporates into

HfO_2 film results in HfO_2 layer increase during PDA. The interfacial layer increases with the increase of PDA temperature. However, its thickness at medium PDA temperature does not increase apparently. Therefore, the leakage current is not dominated by the interfacial layer. After 1000℃ PDA, the interfacial layer increases to around 3 nm so that the current transport is blocked effectively. The interfacial layer is identified as silicate-like material. It must be pointed out that the surface treatment methods employed in this thesis are not efficient enough to suppress the growth of interfacial layer. To further scales down the CET into sub-1nm regime, advanced surface treatment method must be developed.

The surface roughness of the high temperature (>=400℃) deposited HfO_2 films is good enough. It is observed that the surface roughness of HfO_2 film depends on the deposition condition but is not affected by PDA conditions apparently. This observation indicates that the surface roughness does not play role on the observed leakage current.

The most stable state of HfO_2 is crystalline state so that the HfO_2 films tend to crystallize during PDA. Nano-crystals are observed in films deposited at any conditions. For HfO_2 films deposited at low temperature or with insufficient O_2 supply, the nano-crystals are separated by amorphous region and show round shape. It is postulated that the boundary of these nano-crystals contains high concentration impurities especially nitrogen. The HfN-like boundary layer accounts for the leakage current of these samples. Hf-precursor decomposes completely during high temperature deposition, and therefore, with sufficient O_2 supply, the film becomes polycrystalline completely. The lack of high impurity boundary layer results in very low leakage current.

HfO_2 with different crystalline structures may have different flat-band voltages and/or oxide charges. This fact may contribute to the kink of the C-V characteristics shown in section 8-2.

References

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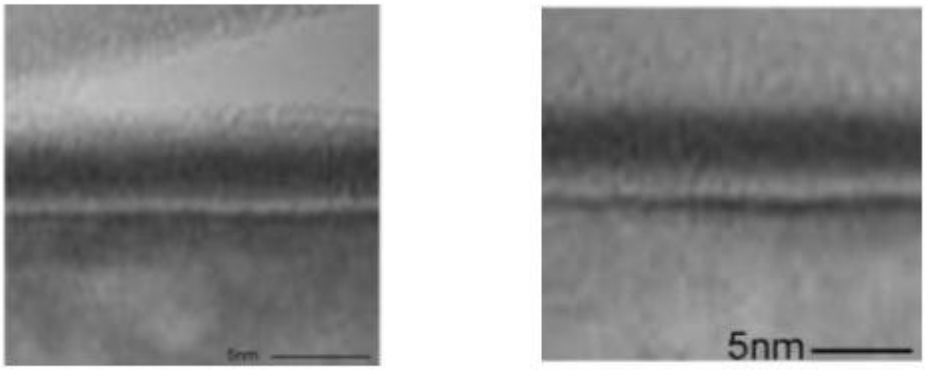
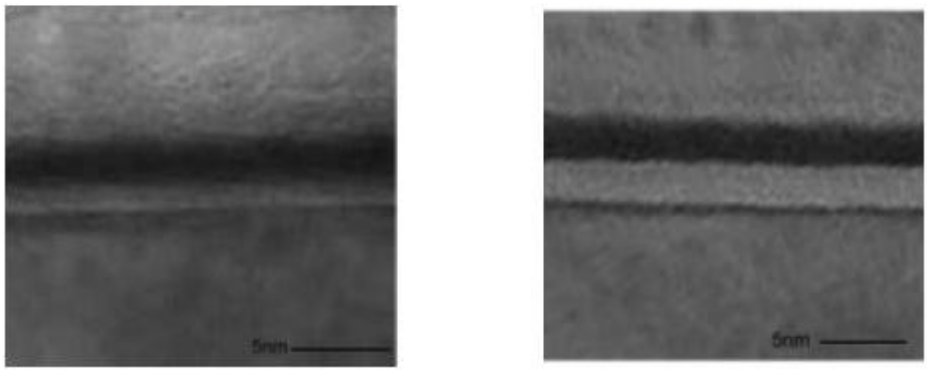
[2]. C. H. Chien, Private Communication

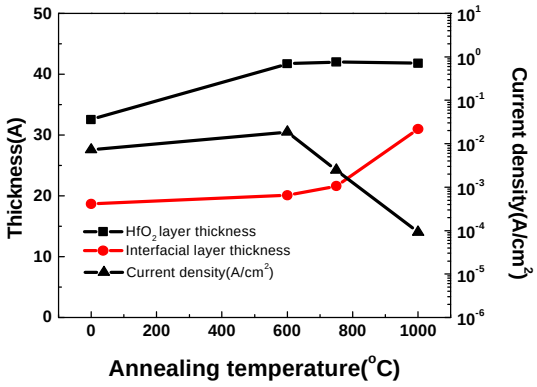
[3]. M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo and A. Nishiyama, “Thermally Stable Ultra-Thin Nitrogen Incorporated ZrO_2 Gate Dielectric Prepared by Low Temperature Oxidation of ZrN” *IEDM Tech. Dig.* sec.20-03 , 2001



(a) As dep. (b) N_2-600℃



(c) N_2-750℃ (d) N_2-1000℃



(e)

Fig.8-1. X-TEM micrographs of samples deposited at T=400℃ on HF-treated wafer with various post annealing temperatures in N_2 ambient for 30sec: (a) as-dep., (b) N_2-600℃, (c) N_2-750℃, and (d) N_2-1000℃. The measured thickness of HfO_2/interfacial layer and correlative are plotted in (e).

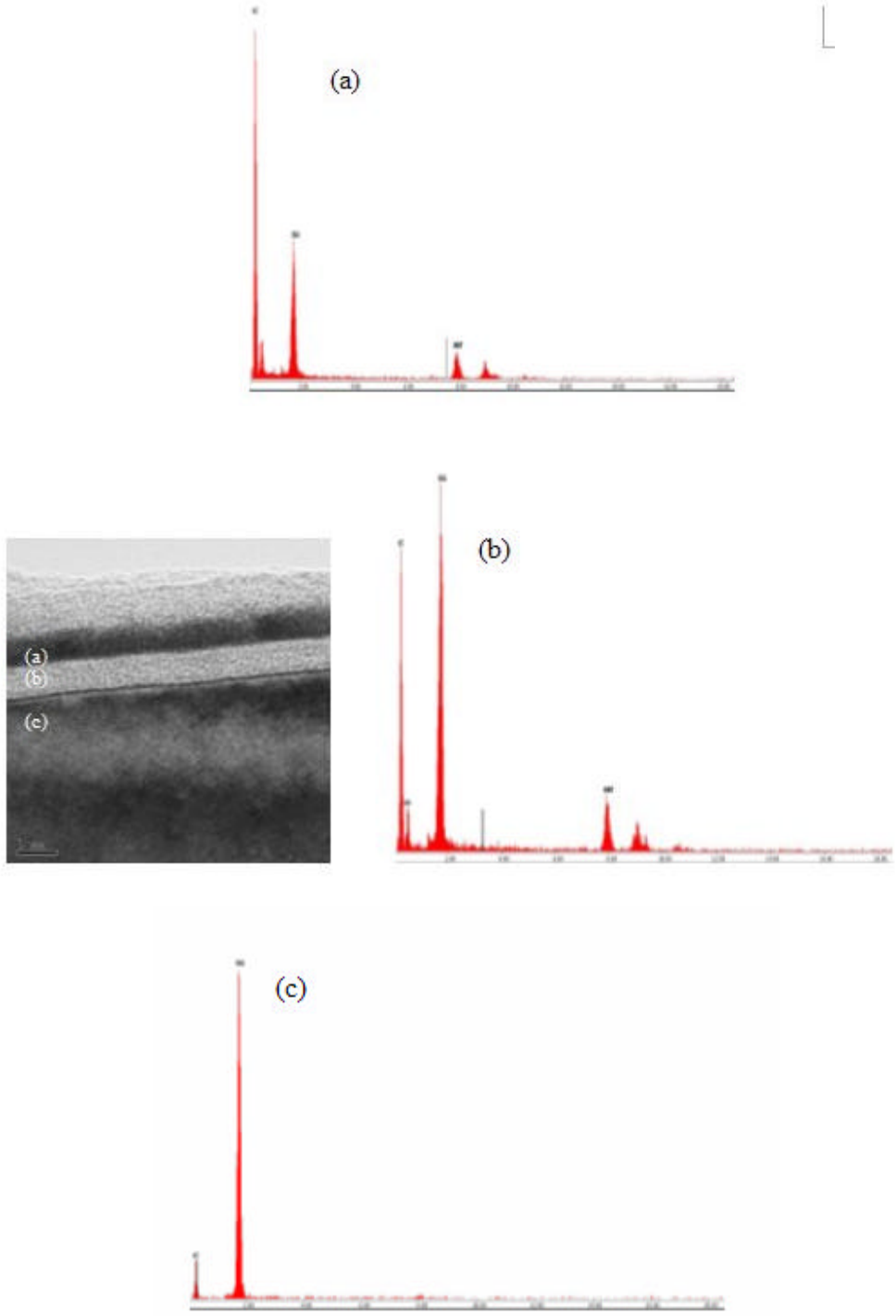


Fig.8-2. Electron probe microanalysis (EPMA) with energy dispersion spectrometer (EDS) to identify the composition of interfacial layer. HfO_2 was deposited at T=400℃ followed by a PDA at 1000℃ in N_2 ambient.

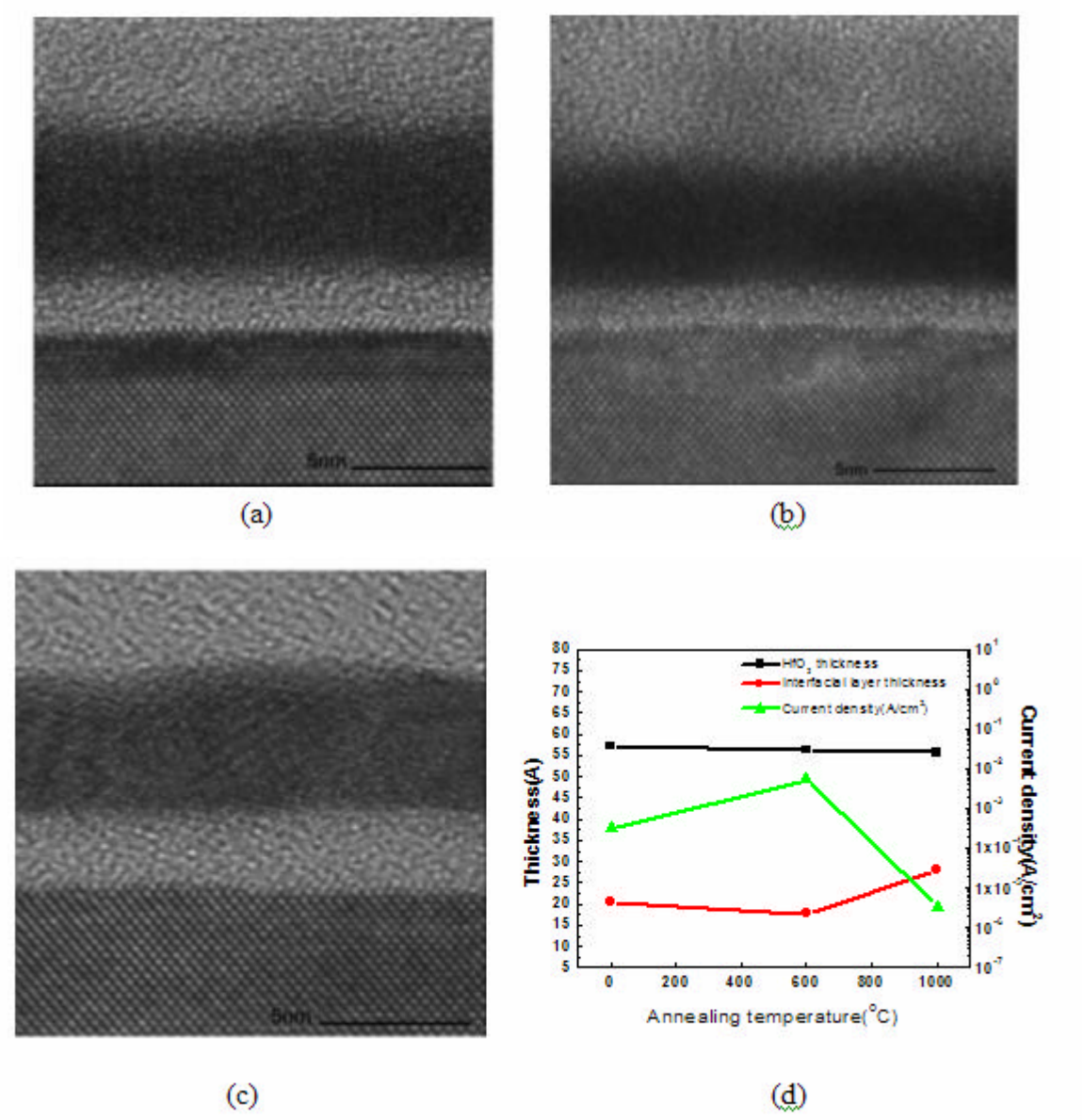


Fig.8-3. X-TEM micrographs of samples deposited at 400℃ on NH_3-treatedwafer. The O_2 flow rate is 500sccm and the pressure is 5mbar. (a) as-dep. (b) N_2-600℃ (c) N_2-1000℃, and (d) HfO_2 /interfacial layer thickness and correlative leakage current..

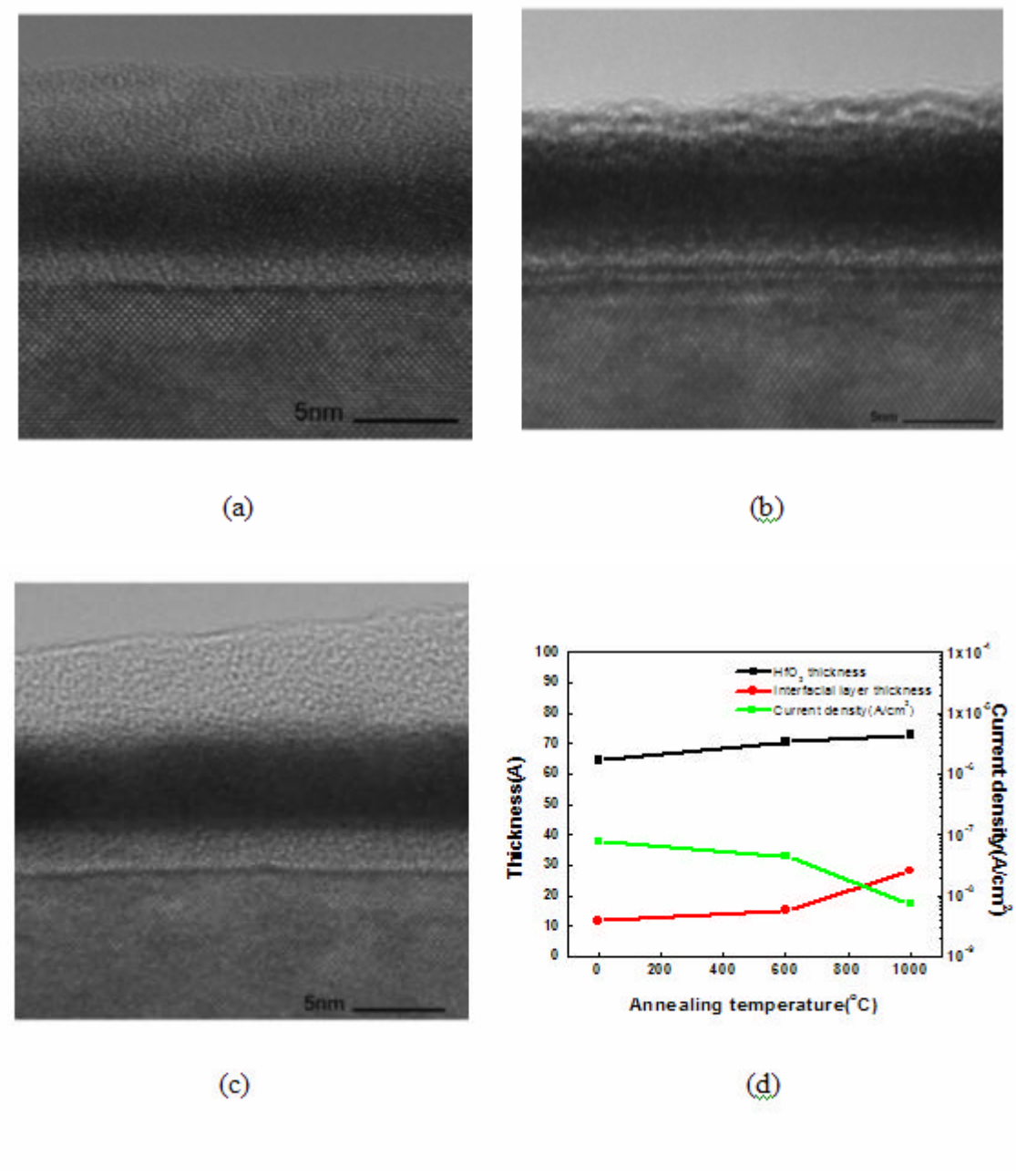


Fig.8-4. X-TEM micrographs of samples deposited at 500℃ on NH_3-treatedwafer. The O_2 flow rate is 500sccm and the pressure is 5mbar. (a) as-dep. (b) N_2-600℃ (c) N_2-1000℃, and (d) HfO_2 /interfacial layer thickness and correlative leakage current.

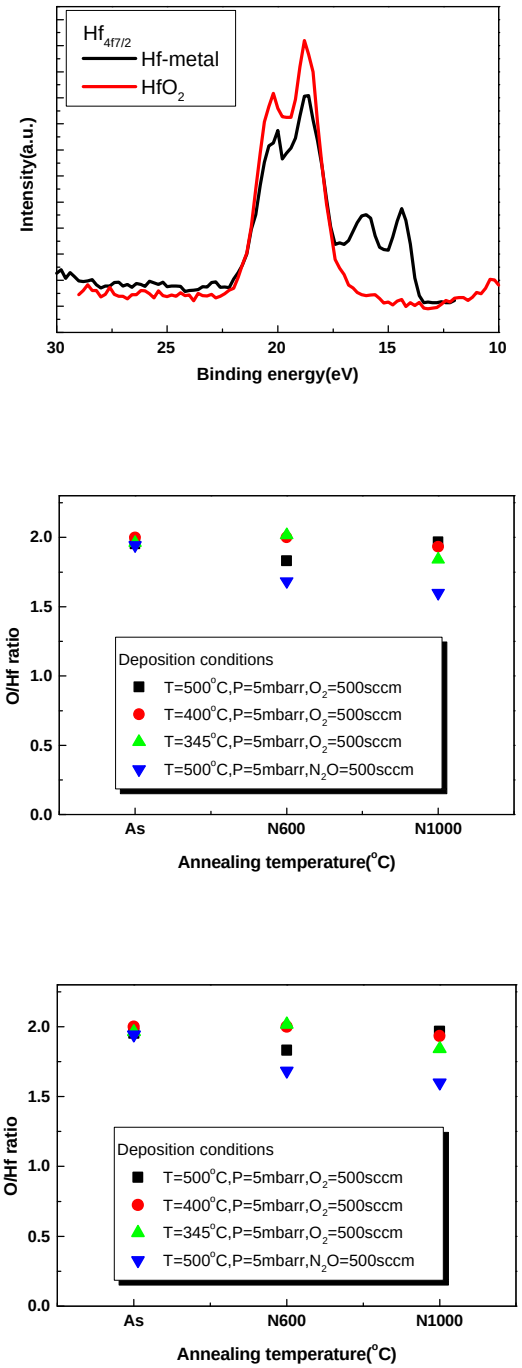


Fig.8-5. Hf metal and HfO_2 XPS spectra for composition analysis and the calculated results of different deposition condition thin film.

(a) Hf spectra of Hf metal and pure HfO_2

(b) O spetctra of Hf metal and pure HfO_2

(c) Thin film composition by XPS analysis

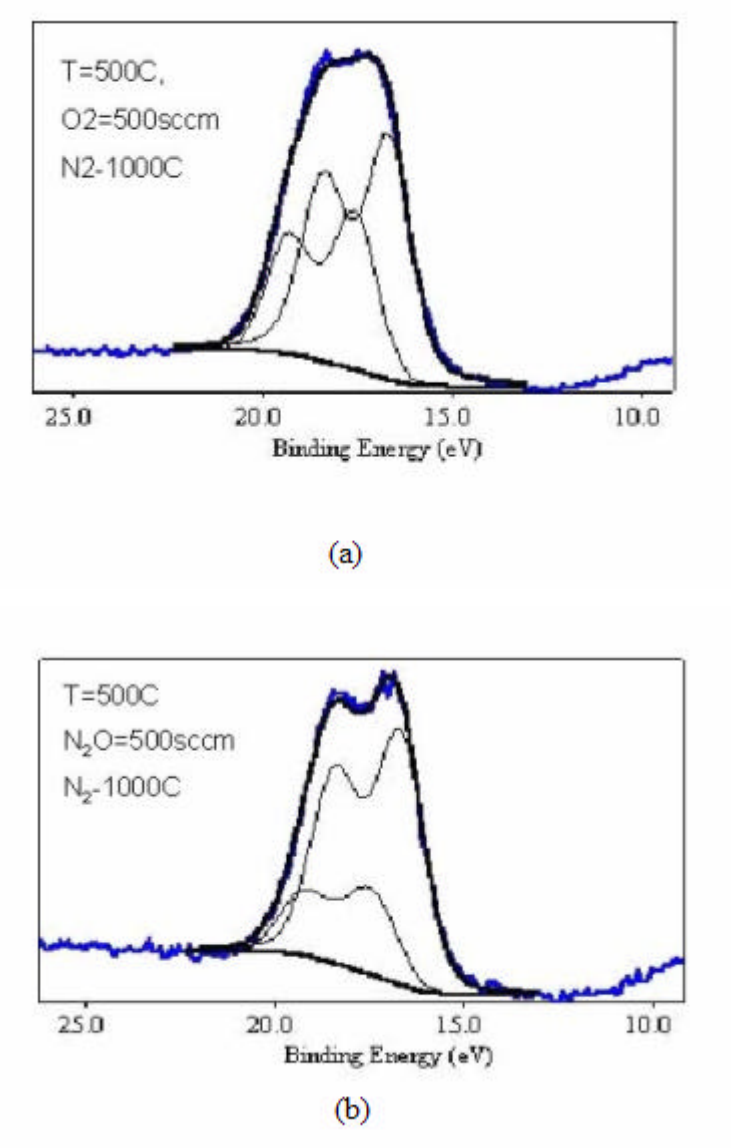
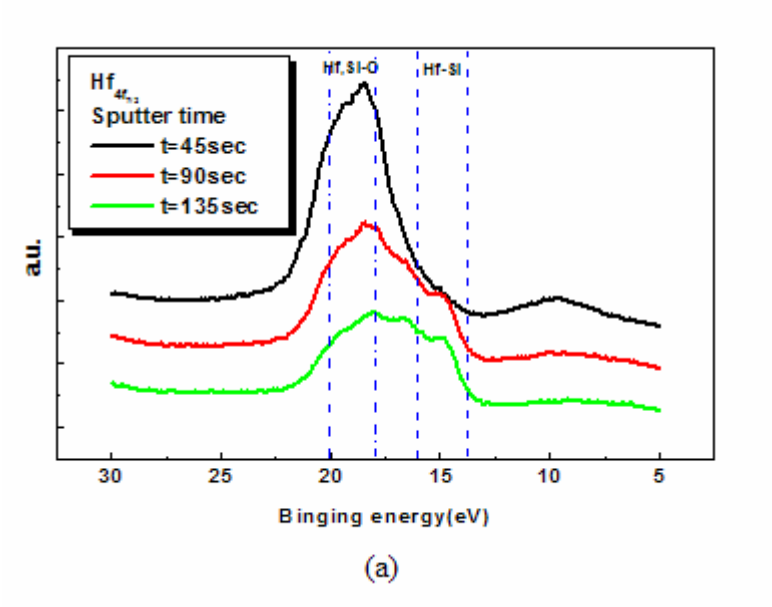


Fig.8-6. Deconvoluted of HfO_2 thin film Hf spectra with N_2-1000℃ post deposition annealing. (a) HfO_2 deposited at T=500℃, O_2=500sccm. (b) HfO_2 deposited at T=500℃, N_2O=500sccm.



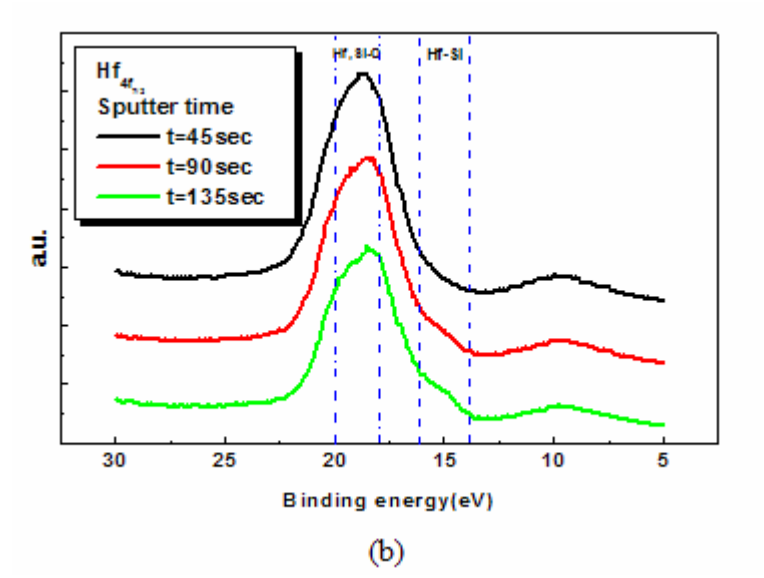
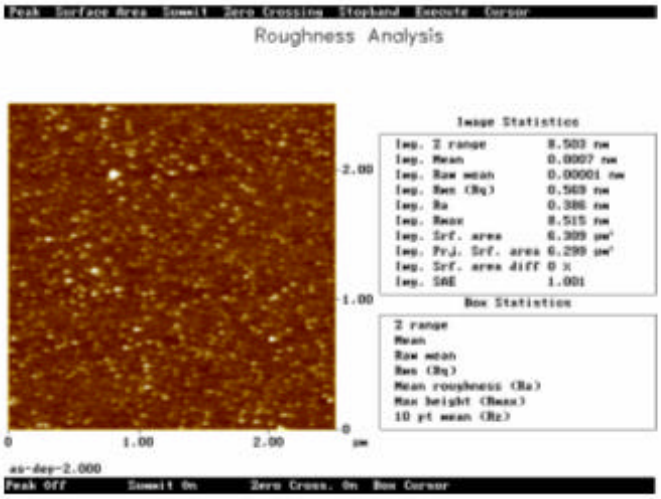
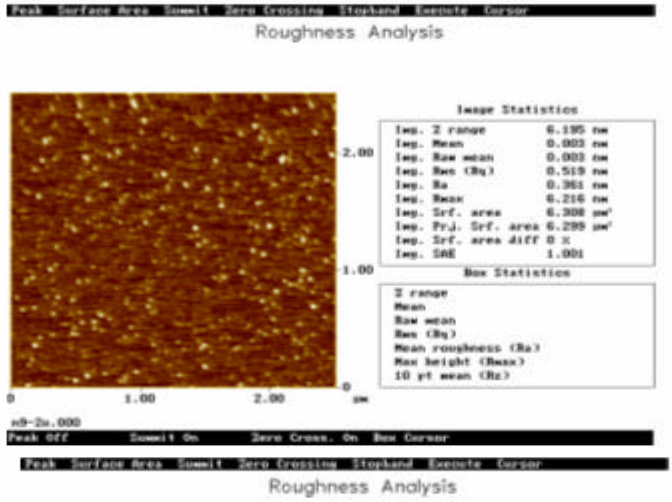


Fig.8-7. XPS spectrum of $Hf_{4f7/2}$ of HfO_2 film after different surface sputtering time. HfO_2 was deposited at T=500℃, P=5mbar, and O_2=500sccm. (a) as-deposition. (b)T=1000℃ for 30sec N_2 ambient PDA.

(a) As deposition



(b) N_2-900℃



(c) O_2-900℃

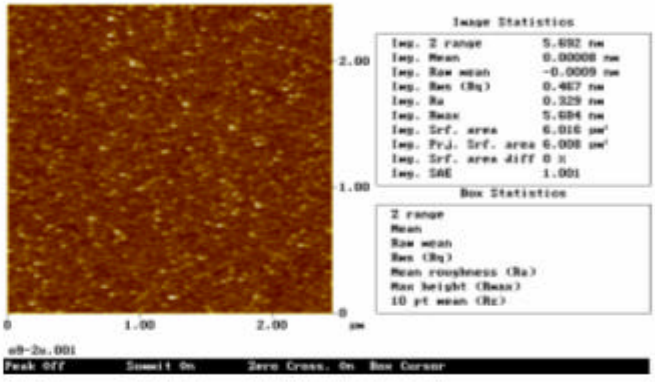


Fig.8-8. AFM images of HfO_2 deposited at T=345℃ O_2 ambient with various post deposition annealing: (a) As deposition, (b) N_2-900℃ for 30sec PDA, and (c) O_2-900℃ for 30sec PDA

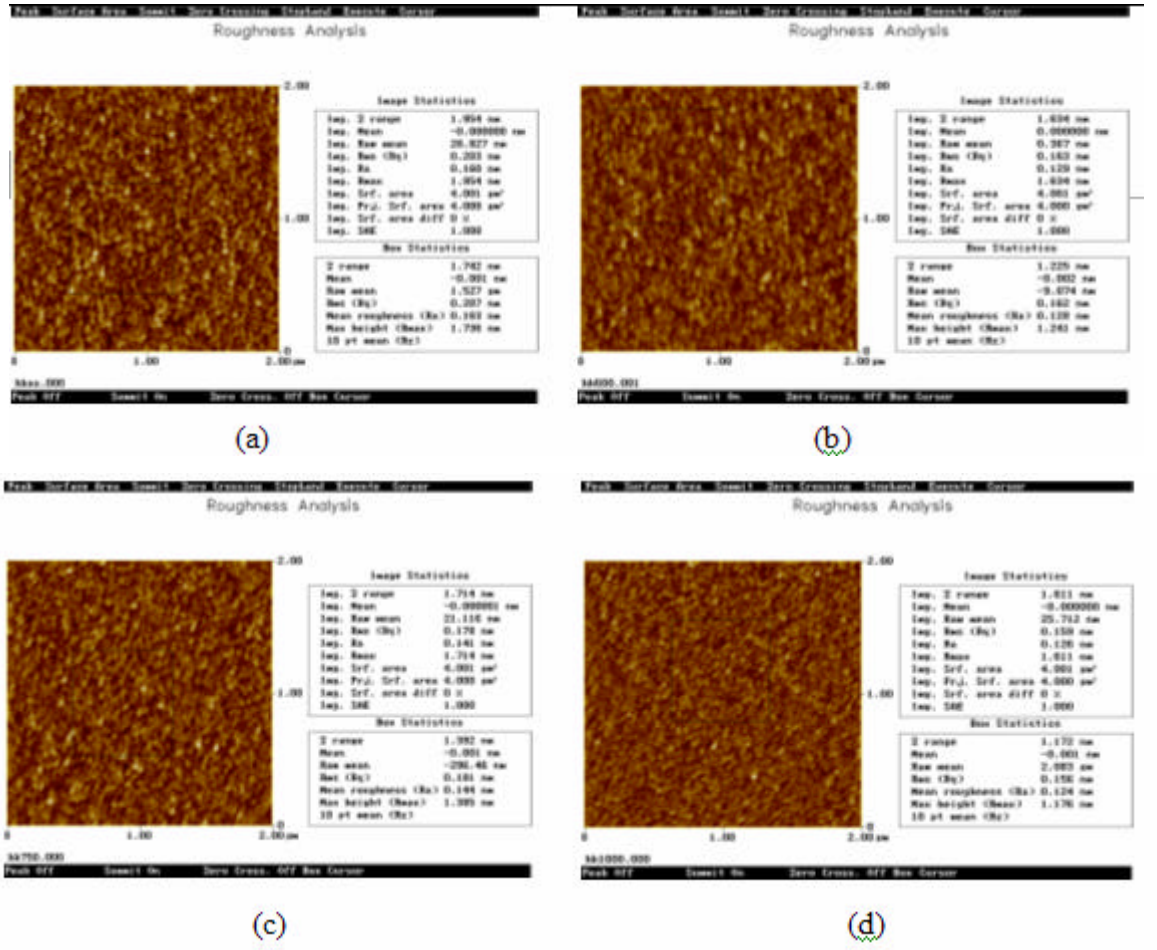


Fig.8-9. AFM images of HfO_2 deposited at T=400℃, O_2=300sccm, P=1.5mbar with different annealing temperature for 30sec. (a) As deposition, (b) N_2-600℃, (c) N_2-750℃, and (d) N_2-1000℃

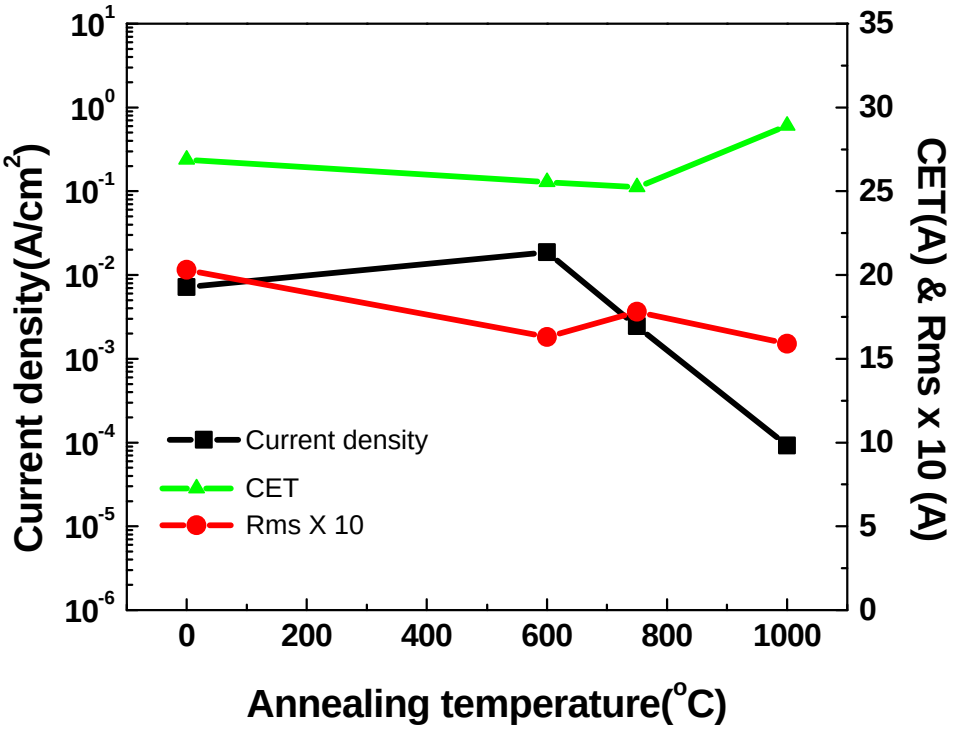


Fig.8-10. Leakage current density, CET and R_{ms} values versus annealing temperature of the samples shown in Fig.8-9.

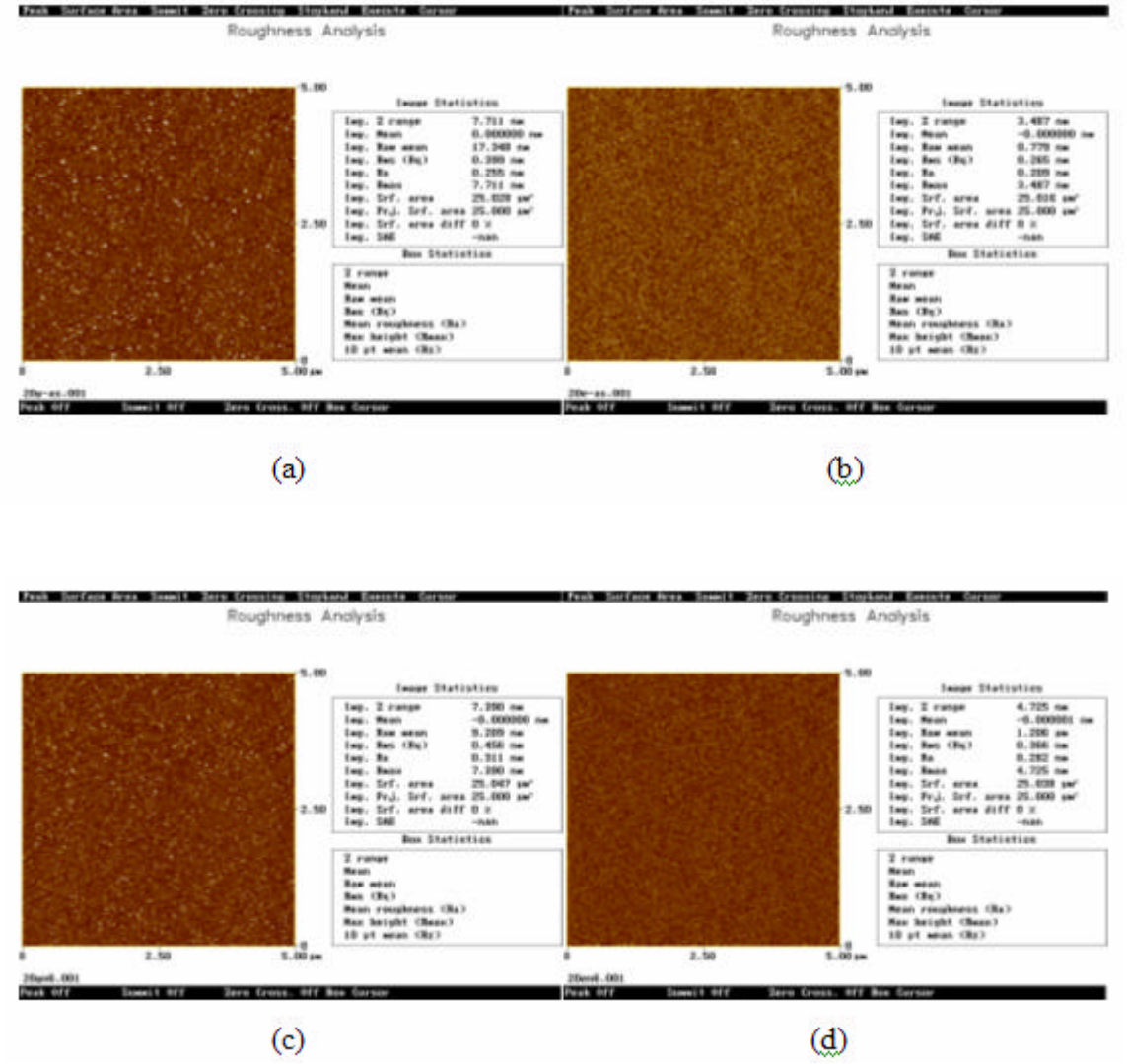


Fig.8-11. AFM images of HfO_2 film deposited at T=500℃ in pure O_2 deposition ambient and N_2O deposition ambient.

(a) O_2 reaction chamber, As deposited samples.

(b) N_2O reaction chamber, As deposited samples.

(c) O_2 reaction chamber, N_2 600℃ 30sec post annealing

(d) N_2O reaction chamber, N_2 600℃ 30sec post annealing

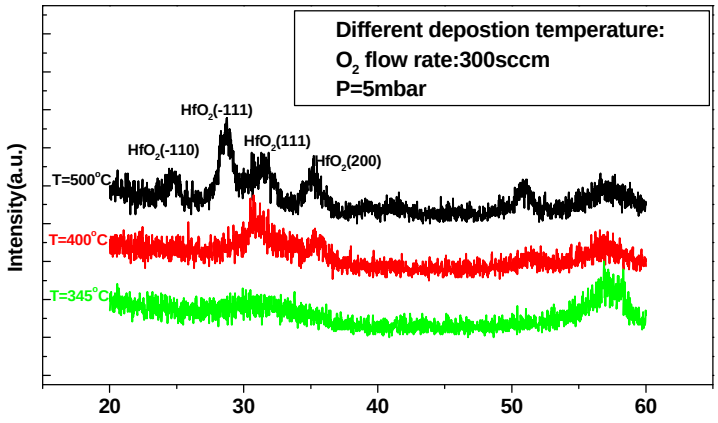
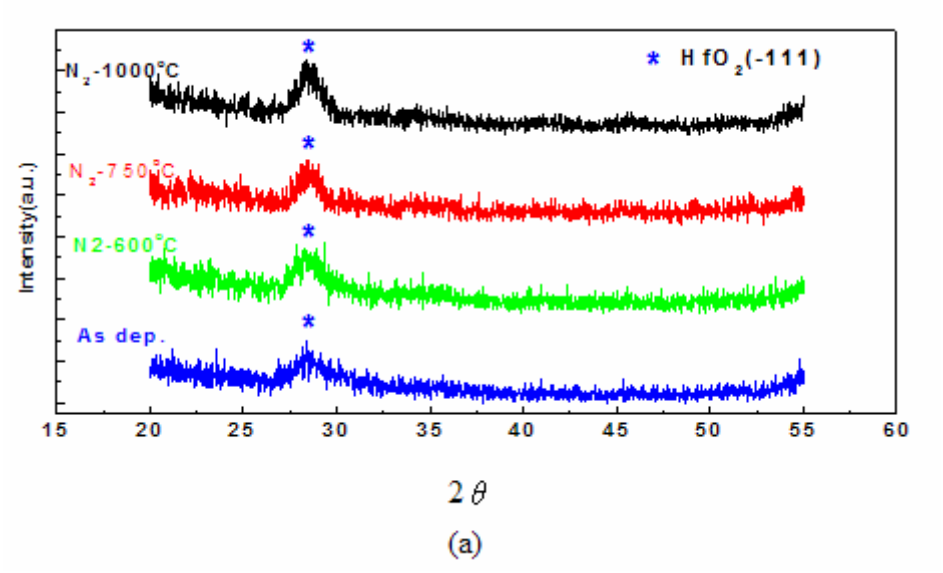


Fig.8-12. G-XRD spectra of HfO_2 film deposited at T = 345℃, 400℃, and 500℃ without PDA.



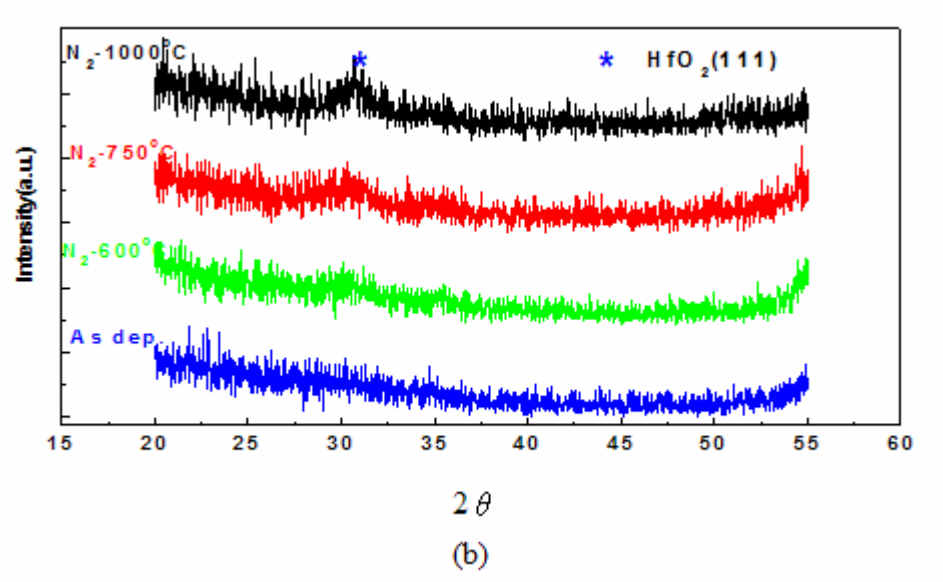


Fig.8-13. G-XRD spectra of HfO_2 films deposited in (a) O_2 ambient, and (b) N_2O ambient followed by PDA in N_2 ambient at different temperatures.

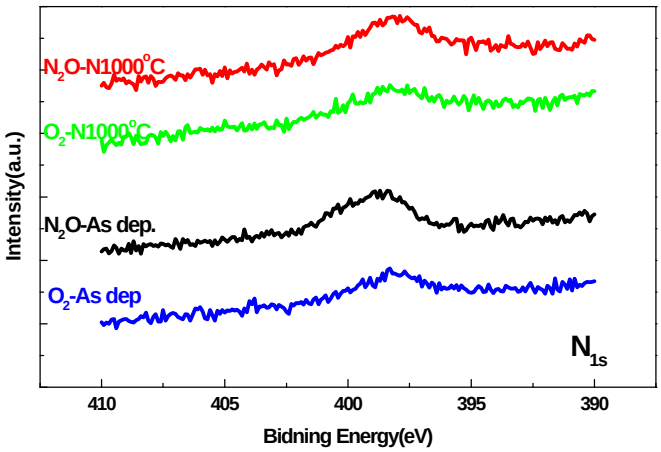


Fig.8-14. XPS binding energy of N in HfO_2 film.

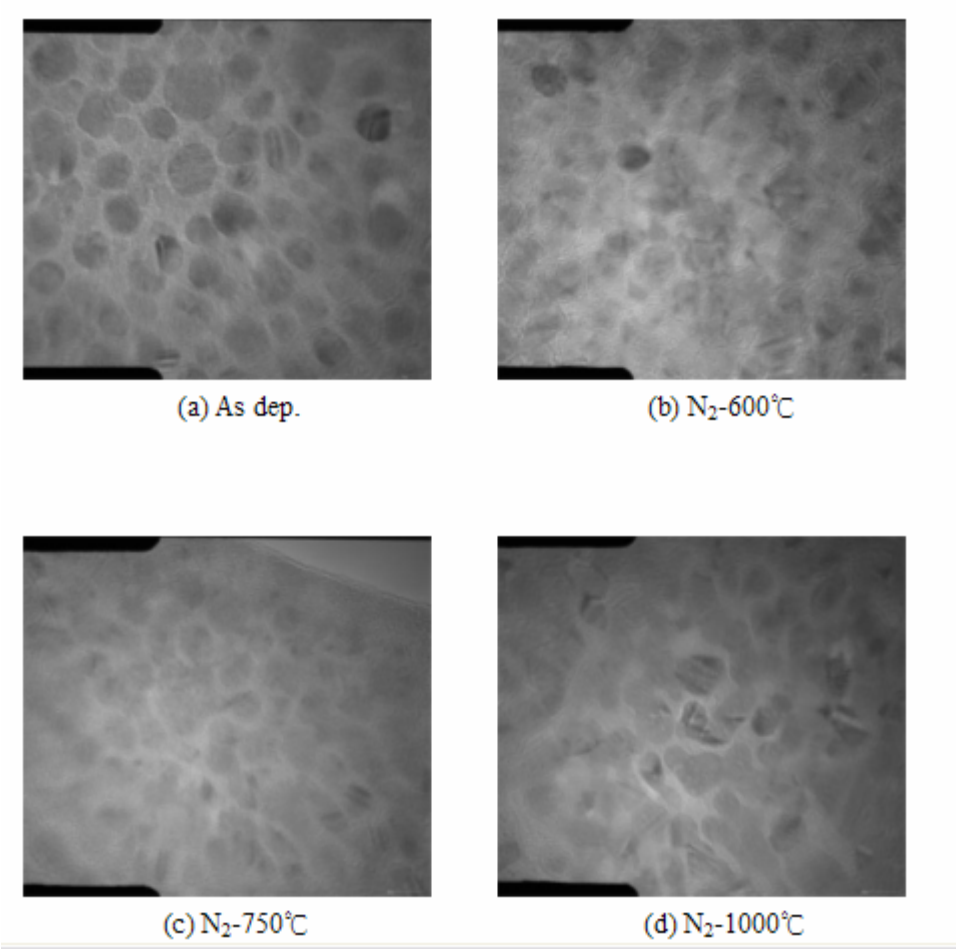
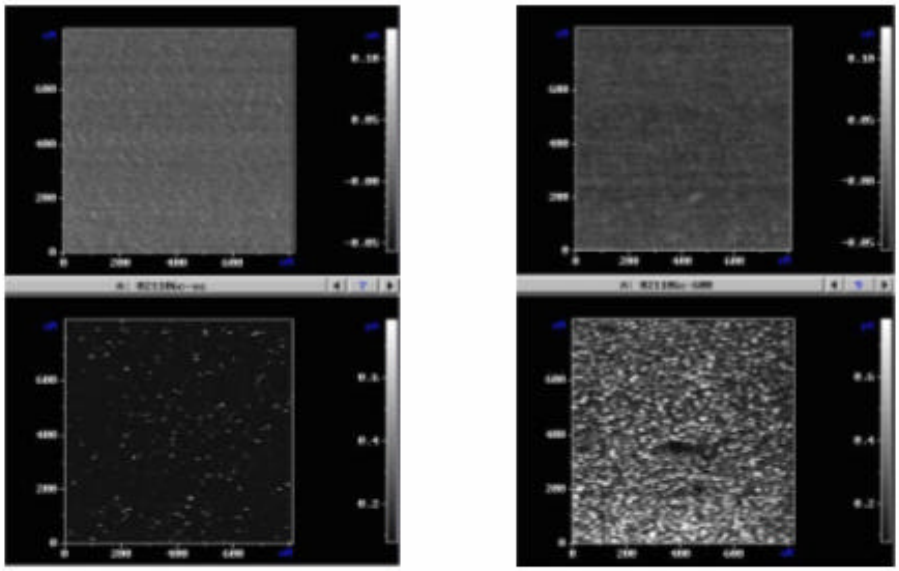
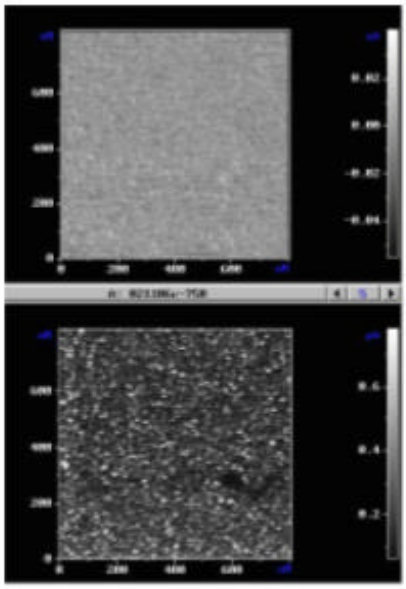


Fig.8-15. The PV-TEM micrographs of HfO_2 thin film deposited at 400℃ with O_2= 300sccm follow by different PDA temperatures: (a)as-deposited, (b)N_2-600℃, (c)N_2-750℃, (d) N_2-1000℃. For annealing time is 30sec. Grain merges at higher annealing temperatures.

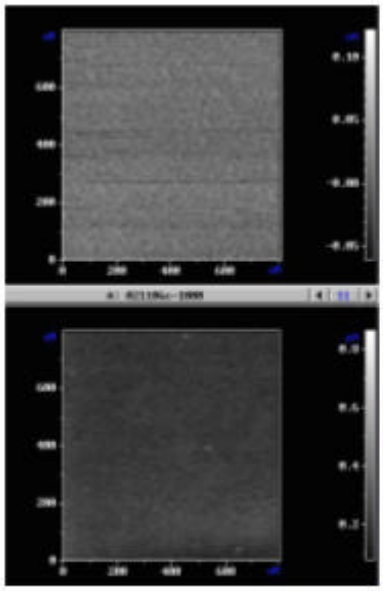


(a) As dep.

(b) N_2-600℃



(c) N_2-750℃



(d) N_2-1000℃

Fig.8-16. Conductive AFM images corresponded to Fig.8-15.

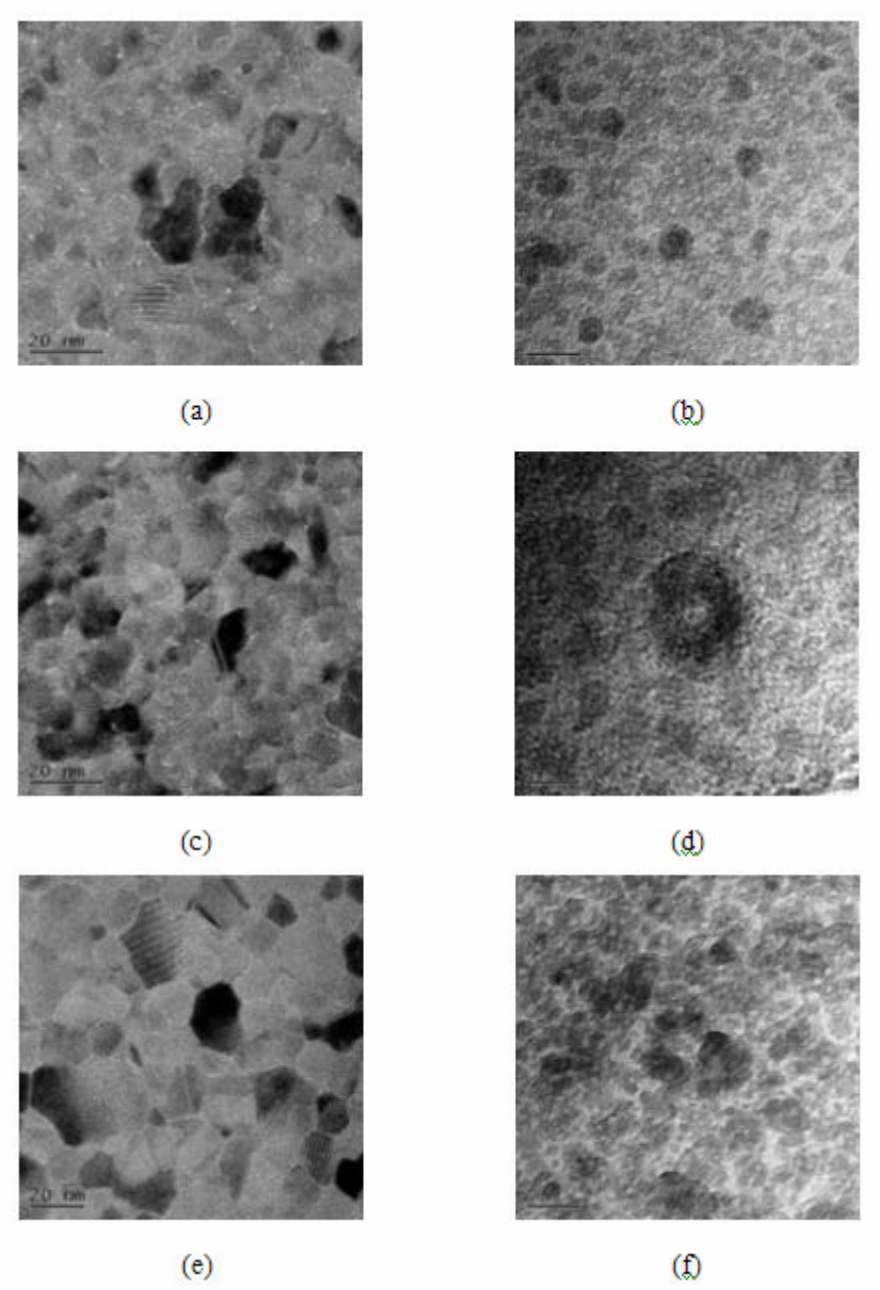


Fig.8-17. PV-TEM micrographs of HfO_2 deposited at T=500℃, P=5mbar both in O_2 and N_2O ambient.

(a) O_2 = 500sccm without PDA

(b) N_2O=500sccm without PDA

(c) O_2=500sccm with N_2-600℃ 30sec PDA

(d) N_2O=500sccm with N_2-600℃ 30sec PDA

(e) O_2=500sccm with N_2-1000℃ PDA

(f) N_2O=500sccm with N_2-1000℃ PDA.

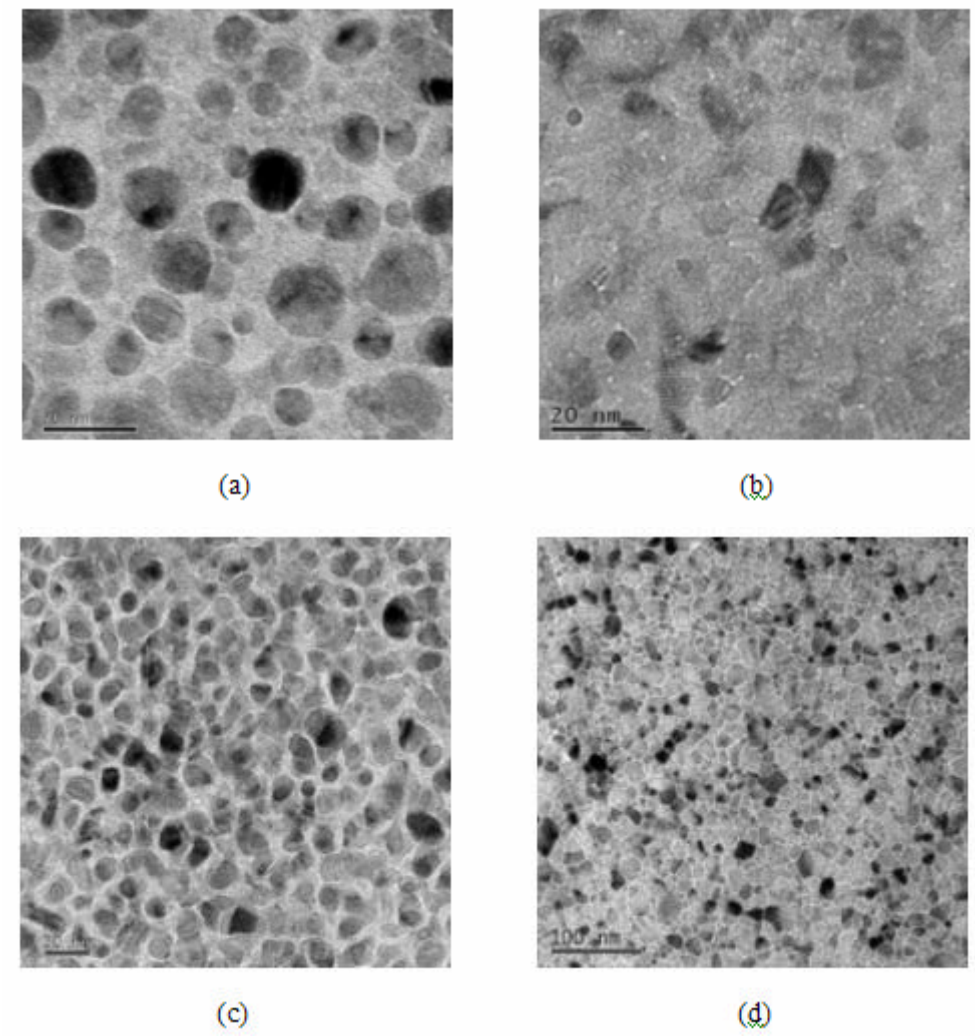


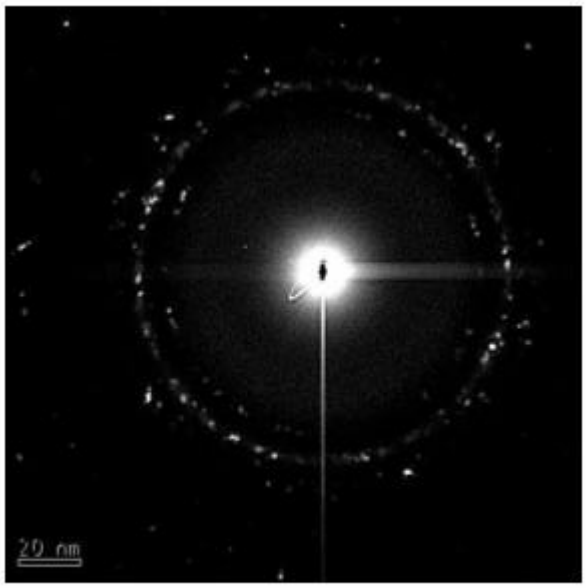
Fig.8-18. The microstructure of HfO_2 deposited at different temperatures:

(a)T = 400℃ without annealing

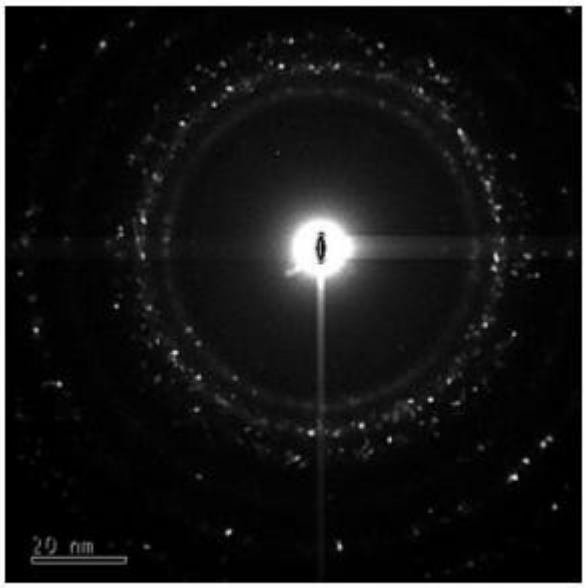
(b)T = 500℃without annealing

(c)T = 400℃ with N_2-1000℃ PDA

(d)T = 500℃ with N_2-1000℃ PDA



(a) As deposition



(b) N_2-1000℃

Fig.8-19. The TEM diffraction pattern of HfO_2 deposited at T=400℃ with different post deposition annealing:

(a) As deposition

(b) N_2-1000℃ for 30sec post deposition annealing

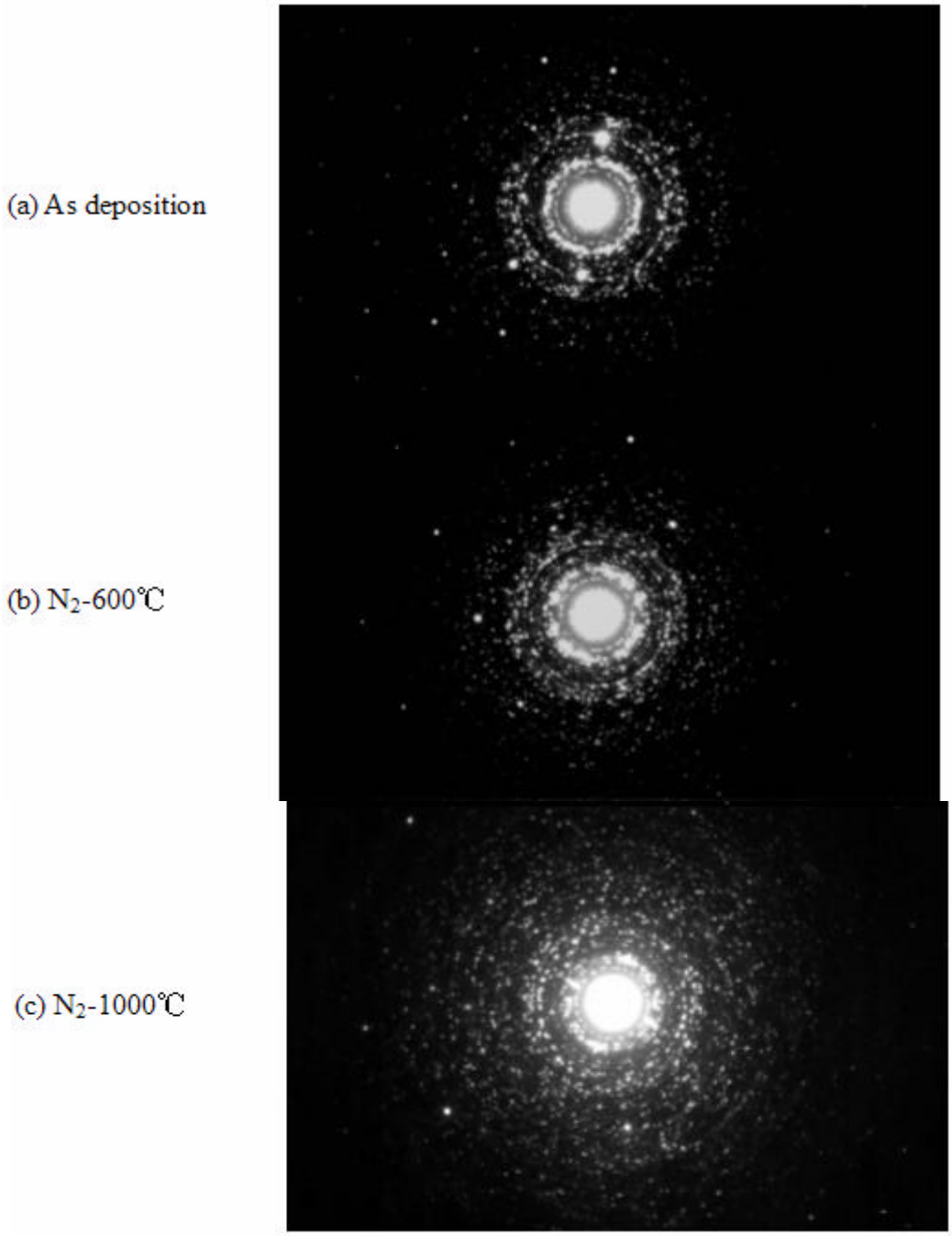


Fig.8-20. The TEM diffraction pattern of HfO_2 deposited at T=400℃ with different post deposition annealing:

(a) As deposition

(b) N_2-600℃ for 30sec post deposition annealing

(c) $N_2$1000℃ for30sec post deposition annealing

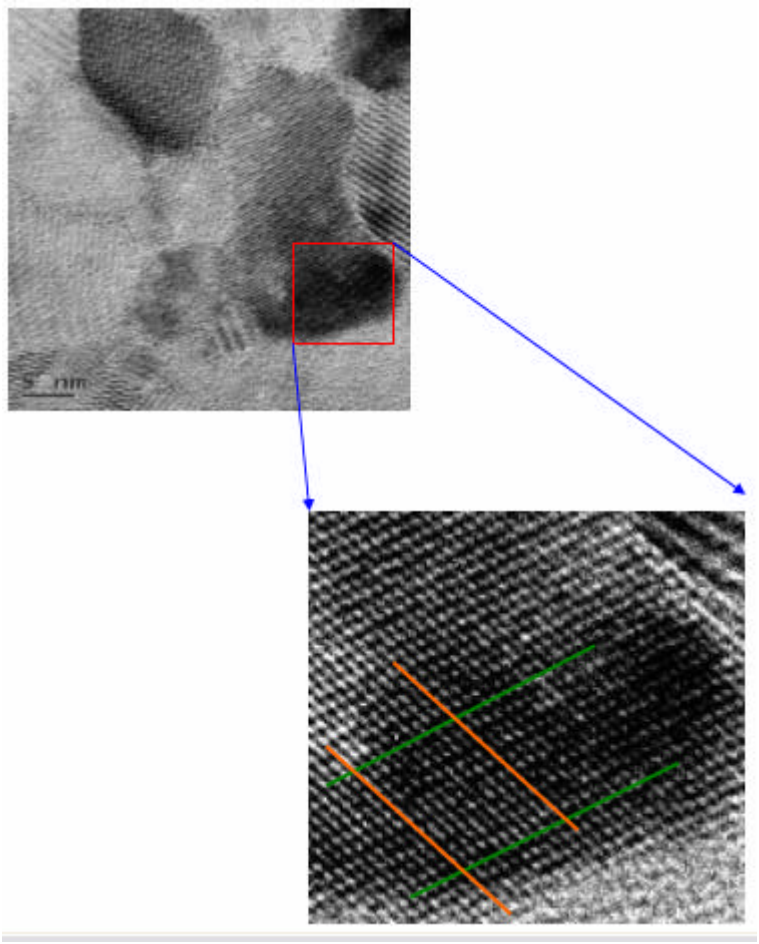


Fig.8-21. 2-D planar view TEM to identify phase structure. HfO_2 was deposited at T=500℃, P=5mbar, O_2=500sccm without post deposition annealing.

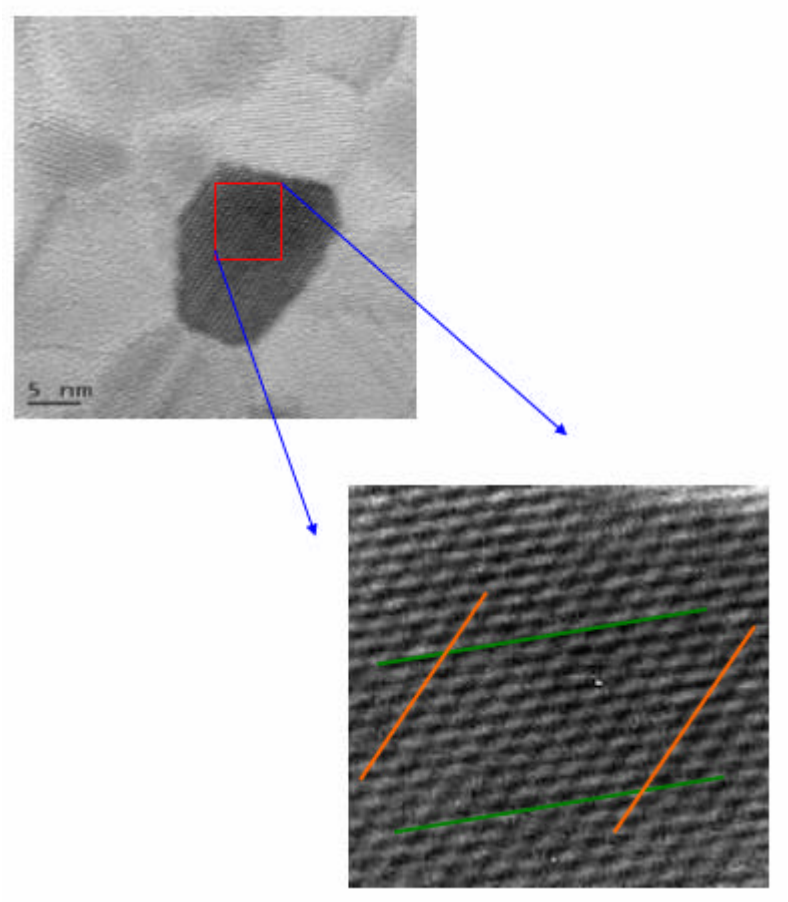


Fig.8-22. 2-D planar view TEM to identify phase structure. HfO_2 was deposited at T=500℃, P=5mbar, O_2=500sccm with N_2-1000℃ 30sec annealing.

Chapter 9
Fringing-Induced Barrier Lowering (FIBL) of Nano-Scale MOSFETs

9-1. Introduction

Silicon dioxide (SiO_2) have been used as gate dielectric of CMOS devices for several decades because of its superior properties such as low interface state density, large energy bandgap (8.9eV), low leakage current, and good thermal stability for Si substrate and poly-Si gate. As device dimensions scale down, the thickness of SiO_2 must be reduced to keep sufficient current driving capability. But when the thickness of SiO_2 becomes thinner than 3.5nm, direct tunneling current increases 100 times for every 0.4~0.5 nm decrease of thickness [1]. This high gate leakage current would increase standby power consumption and induce loss of inversion layer charges. In order to reduce gate current caused by direct tunneling, the physically thickness of dielectrics must increase such that the effective oxide thickness (EOT) can scale down continuously. New gate dielectrics with dielectric constant (*k*) higher than SiO_2 must be developed. Many alternative high dielectric constant (high-*k*) materials with dielectric constant higher than SiO_2 have been studied to overcome the challenge of gate dielectric scale down [2-10]. However, a side effect called fringing-induced barrier lowering (FIBL) arising from the use of high-*k* gate dielectric has been reported [11-16]. The fringing electric field originated at drain penetrates into channel through the high-*k* gate dielectric and suppress the barrier height from source to channel. Therefore, the off-state drain current (I_{off}) increases and the maximum allowable *k* value of high-*k* dielectric is limited by the FIBL effect.

Several works had been performed to understand the effect of FIBL on device and circuit performance. Some works also discussed the effect of device structure on FIBL. Yeap et al reported the FIBL for the first time. The FIBL is clearly evident for $k>25$ [11]. Remaining high-*k* dielectric under spacer greatly enhances the FIBL. It is also proposed that an oxide buffer layer under high-*k* dielectric can suppress the FIBL. Lai et al studied the effect of stack gate dielectric more detailed [12]. But the results of severer FIBL at shallower junction depth and longer spacer length are not straight forward. Kencke et al studied the effect of FIBL with asymmetric devices

having different source and drain spacer dielectrics [13]. They found that FIBL is caused largely by drain side high-*k* spacers. On the basis of their results, long spacer length and low dielectric spacer are preferred. Kamata et al simulated the effect of FIBL on elevated source/drain devices and concluded that although the FIBL is enhanced with the extension elevation, the enhancement is negligible with the presence of thin low-K sidewalls [14]. Lin and Kuo reported that the effect of FIBL on SOI devices is similar to that on bulk devices [15], while X. Liu et al reported that the fully depleted SOI device has better immunity on the FIBL induced Ioff degradation [16]. Recently, Mohapatra et al studied the effect of stack gate dielectric and lateral channel engineering and proposed that the overlap length (L_{ov}) between gate and source/drain is an important parameter for FIBL [17, 18].

Although so many works have been conducted to understand the effect of FIBL on device characteristics, the knowledge about FIBL is still insufficient. At first, the above literatures simulated FIBL with different EOT, gate length, junction depth, and/or spacer length (L_{sp}). Therefore, some literature reports several orders of magnitude increase of I_{off} due to FIBL while another literature reported only a few times increase of I_{off} [11, 13, 15]. On the other hand, some confused results were reported for example the longer the spacer is, the severer the FIBL effect is [12]. Finally, the shortest gate length (L_g) studied in previous literature is 50nm [13, 18] but is known that high-*k* gate dielectric will not be used until the 65 nm technology node which implies a L_g of shorter than 40nm [19].

In this work, two-dimensional simulators SUPREME and MEDICI [20, 21] were employed to study the effect of device structure on FIBL with L_g down to 25 nm. The structural parameters studied including the gate length, the spacer length, the overlap length between gate and source/drain, the stack gate dielectric, and the material of spacer material. The impact of high-*k* dielectric under spacer is also evaluated. Finally, the effect of FIBL on SOI device is also investigated at the same basis.

9-2 Simulation Procedure

Commercial SUPREME and MEDICI programs were used to generate doping profile and to simulate electrical characteristics, respectively. A typical device structure with simple shallow source/drain junction is used. In most cases, the spacer length is set to be equal to the gate length. Since the shortest L_g studied in this work is 25 nm, the channel doping profile and source/drain

doping profile of the 25 nm device are carefully adjusted so that the threshold voltage (V_{th}) is 0.25 V and the I_{off} as k=3.9 is $3x10^{-7}$A/um at a drain voltage of 1 volt. This device is called as the 25nm reference device. During the device simulation, poly-depletion, quantum-effect, impact ionization, energy balance, and channel surface scattering are all considered to make sure the designed 25nm reference device with k=3.9 is practical. Five different k values of gate dielectric are simulated. They are 3.9, 15, 25, 50, and 100. The k value of 15 is close to that of Hf-silicate or Zr-silicate while the k value of 25 is close to that of HfO_2 or ZrO_2 [22]. The channel width and effective oxide thickness is fixed at 1um and 1 nm, respectively. For the SOI devices, the thickness of Si layer is 50 nm and the channel and source/drain doping profiles are identical to those used for bulk devices. Because it is a fully depleted device, the threshold voltage of the SOI device is slightly lower than that of the bulk device. In the whole work, only NMOSFET was simulated.

9-3 Results and Discussion

9-3-1 Basic Phenomenon

Fig.1 compares the $I_{off}/I_{off}(k=3.9)$ ratio as a function of k value of devices with L_g=50nm and 25nm. The doping condition of the 50 nm device is identical to that of the 25 nm reference device. As expected, the I_{off} degradation increases with the decrease of gate length and the increase of k value of gate dielectric. Since the L_{sp} and device doping are fixed, the observed difference of I_{off} degradation between devices is simply attributed to the gate length effect. It should be noted that the increase of I_{off} as k value increases from 3.9 to 100 is less than one decade even if the L_g is only 25 nm. It seems that the FIBL effect does not degrade I_{off} as serious as those reported previously. This discrepancy will be discussed later.

It was reported that the high-k dielectric should exist under gate electrode only. Otherwise, the high-k dielectric under spacer will enhance the FIBL effect [11]. Unfortunately, to remove exposed high-k dielectric after gate etching is very difficult. At first, traditional poly-Si gate etching must stop on gate dielectric to avoid micro-trenching phenomenon at gate edge. Second, the thermal annealed HfO_2 or ZrO_2 film is hard to be wet etched [23, 24]. No chemical which can etch HfO_2 or ZrO_2 at sufficient high etching rate while has sufficient selectivity to field oxide has been proposed till now. Since the above suggestion is drawn at the condition of L_g=70nm, k=100, and EOT=1.5nm and is not practical, it is worthy to re-examine the impact of high-k dielectric

under spacer at sub-45nm technology node.

The structure with high-*k* dielectric under gate electrode only is noted as UG structure and the structure with high-*k* dielectric under both gate electrode and spacer is noted as UGS structure. Fig.2 shows the $I_{off}/I_{off}(k=3.9)$ ratio as a function of *k* value of devices with L_g=25nm. The inset is the schematic drawings of UG and UGS structures. It is clear that as *k* value is lower than 25, the FIBL effect is not serious and the difference between UG device and USG device is negligible. This result indicates that it is not necessary to remove high-*k* dielectric immediately after gate patterning if the *k* value is not higher than 25 if there are no other issues such as contamination, parasitic capacitance, etc. The device integration can be simplified.

9-3-2 Effect of L_{ov}

Electric potential distribution is simulated with the MEDICI program and is shown in Fig.3. Both L_g and L_{sp} are 25nm and *k* value is 100. In this simulation, gate, source, and substrate are all grounded and drain is biased at 1V. It is observed that most of the fringing field lines which originate from drain region out of spacer and under spacer tend to terminate at gate electrode. The main fringing field resulting in barrier lowering originates from the gate/drain (G/D) overlap region.

Since the fringing field originates from the G/D overlap region, FIBL should be sensitive to the length of overlap region (L_{ov}). To verify this inference, devices with doping profile identical to that of the 25nm reference device but with various G/D overlap were simulated. The L_{ov} in Fig.3 is 1 nm. To increase the L_{ov} while keeps the same source/drain doping profile and similar device performance, the spacer, gate electrode, and gate oxide were removed after generating the reference device. Then, gate structure with L_g=50 nm was reconstructed so that the L_{ov} becomes 13.5nm. Fig.4 shows the simulated equal potential contours at drain voltage of 1V. Comparing with Fig.3, the long L_{ov} enhances the penetration of fringing field into channel region. Fig.5 shows that the I_{off} degradation of device with L_{ov}=13.5 nm is one order of magnitude higher than that with L_{ov}=1nm. Since the L_{ov} decreases with the scale down of design rule to control the short channel effect, the degradation of I_{off} due to FIBL effect could be relaxed due to the short L_{ov}. In the earlier study on FIBL effect, device structure is designed following the 90nm or 130nm technology node. In those cases, the L_{ov} is longer than that used in this work. The different L_{ov} explains the wide variation of FIBL effect induced I_{off} degradation in previous literatures.

9-3-3 Effect of Spacer Length

Because both L_g and L_{sp} were scaled down simultaneously in most of the literatures, which factor dominates the I_{off} degradation is not clear. To clarify the effect of L_{sp} on FIBL, devices with identical effective channel length but different L_{sp} must be generated. To achieve this, the 25nm reference device was generated at first. Then the spacer was removed and a 50nm long spacer was reformed. Fig.6 shows the I-V curves of devices with various L_{sp} as k=100. The inset illustrates the schematic structure of the devices. It is observed that the I_{off} degradation is reduced by the reduction of spacer length. This observation is similar to that reported by Lai et al. [12]. Lai explained their observation by the decrease of FIBL region as L_{sp} decreases. However, as discussed in previous sub-section, the fringing field originating from the region out of the gate/drain overlap region plays minor role on the FIBL effect. We propose a new mechanism to explain the effect of spacer length.

It is known that the fringing field exits at both drain side and source side. The drain electrode is biased at high voltage and the fringing field from drain side tends to lower the electron injecting barrier height near source side. Since the source electrode is grounded, the fringing field from source side tends to sustain the channel barrier height. This is called the Fringing-Induced Barrier Shielding (FIBS) and was proposed by D. L. Kencke et al and Y. Kamata et al. [13, 14]. As the L_{sp} increases, the FIBL effect from drain side is less affected by the long spacer because the FIBL effect is dominated by the gate/drain overlap region. However, the source electrode becomes away from channel as the spacer length increases and the FIBS effect from source side becomes weak. The shorter the L_{sp} is, the stronger the FIBS effect is. For the short L_{sp} device, the FIBS effect from source side compensates the FIBL effect from drain side partly. Therefore, shorter L_{sp} results in less I_{off} degradation. Fig.7(a) and (b) show the equal potential contours of the devices with L_{sp}=25nm and L_{sp}=50nm, respectively. The dense potential contour at source side of the L_{sp}=25nm device supports the above explanation. This phenomenon is positive because the spacer length scales with the gate length.

9-3-4 Stack Gate Dielectric

It is known that stack gate dielectric, a buffer SiO_2 layer under or above the high k dielectric, can relax the FIBL effect. This method is much more effective as the buffer SiO_2 layer is placed

under high-*k* layer than above high-*k* layer. This difference can be explained by the observation in the previous sub-section. Since the fringing field originates from the G/D overlap region, it enters high-*k* layer if the buffer SiO_2 layer is located above high-*k* layer. In the case of fixed EOT, the effect of buffer layer is to reduce the thickness of high-*k* layer. Therefore, the improvement of FIBL effect is very limited. On the other hand, as the buffer layer is located under the high-*k* layer, fringing field enter the buffer layer at first. Therefore, the low dielectric constant of the buffer layer relaxes the FIBL effect apparently. Fig.8 shows the simulated I-V curves of devices with various gate dielectric structures. The device structure parameters are L_g=25 nm, L_{sp}=25 nm, L_{ov}=1 nm, and EOT=1 nm. It is observed that the FIBL induced I_{off} degradation as *k*=100 can be reduced by 50% using stack gate dielectric of 0.3nm thick buffer SiO_2 layer under the high-*k* layer. However, the FIBL effect can not be eliminated totally using this strategy.

In real case, it is difficult to avoid a buffer layer or interfacial layer between Si channel and high-*k* layer. Buffer SiO_2 layer can improve carrier mobility [25, 26] but it will hurt the EOT because of its relatively low *k* value. Fortunately, several literatures reported that a Hf-silicate (Zr-silicate) layer forms if HfO_2 (ZrO_2) is used as gate dielectric [27-29]. The *k*-value of both kinds of silicate is around 15. Fig.9 compares the effect of *k* value of buffer layer. The EOT of buffer layer is fixed at 0.3nm and the total EOT of stack gate dielectric is fixed at 1nm. The *k* value of high-*k* layer is 100. It is observed that as L_{ov} is 1 nm, either the *k* value of buffer layer being 3.9 or 15 results in almost identical I_{off}. However, as L_{ov}=13.5nm, buffer layer with higher *k* value results in slightly lower I_{off}. To explain this unexpected phenomenon, the electric potential distribution of devices with L_{ov}=13.5nm and different buffer layer are examined. Using SiO_2 as buffer layer, Fig.10(a) shows that because the SiO_2 layer is only 0.3nm thick, fringing field can penetrate the SiO_2 layer and enter the high-*k* layer easily. Since the EOT of buffer layer is fixed at 0.3nm, the physical buffer layer thickness as *k*=15 is thicker than that as *k*=3.9 so that less fringing field enters the upper high-*k* layer as shown in Fig.10(b). According to the result shown in Fig.1, the FIBL effect as *k*=15 is negligible and then the FIBL effect of device with buffer layer of *k*=15 is lower than that of *k*=3.9. It is thus concluded that the interfacial layer formed at the high-*k*/Si interface can relax the FIBL effect no matter it is oxide or silicate and silicate is preferred from the FIBL effect point of view.

9-3-5 Conductive Spacer Material

Since the fringing field terminating at gate electrode plays no role on I_{off} degradation, it is expected that using conductive spacer to attract fringing field may be a possible solution to suppress FIBL effect. Device with conductive spacer has been proposed by F. Gonzalez et al to reduce short channel effect [30]. Fig.11 shows the equal potential contours of device with conductive spacer. The device parameters are L_g=25nm, L_{sp}=25nm, L_{ov}=1nm, and k=100. The spacer is consists of an insulating layer of 3nm thick and a conductive layer of 22 nm thick. The conductive spacer is kept at the same potential as the gate electrode. It is observed that that fringing field near gate edge directs toward conductive spacer now. Fig.12 shows the efficiency of conductive spacer on the I_{off} degradation. With L_{ov}=1nm and 13nm, I_{off} as k=100 can be improved to 3.6 and 2 times of that as k=3.9, respectively. Again, G/D overlap length dominates the FIBL effect.

Fig.13(a) and (b) summarize the FIBL of 25nm devices with various structures. As L_{ov}=1nm, single high-k dielectric results in I_{off} degradation of 23 times. A 0.3nm thick interfacial SiO_2 layer reduces the degradation to 3.6 times, while conductive spacer reduces the dagradation to 3.3. Combining stack dielectric and conductive spacer, the I_{off} degradation can be reduced to 1.6 times. As L_{ov}=13nm, similar tendency is observed but I_{off} degradation is higher than one order of magnitude for all structures. It should be noted that as the k value is reduced to 25, all of the corresponded Ioff degradation are lower than 1.5.

9-3-6 SOI versus Bulk Devicesl

The FIBL effect on SOI devices have been studied in some literatures [15, 16]. It is reported that SOI devices, especially fully depleted SOI devices, has better resistance to FIBL effect. The gate length used in the previous studies is 70-100nm. Since SOI device would be the mainstream beyond the 45nm technology node, the FIBL induced I_{off} degradation on SOI and bulk devices are compared. The L_g and L_{sp} are 25nm and the EOT is 1nm for both SOI and bulk devices.

In Fig.14, it is confirmed that the I_{off} degradation of SOI device is smaller than that of bulk device. This phenomenon can be explained by the thin Si layer. Because the thin Si layer of SOI, the space charge in channel depletion region of SOI device is fewer than that of bulk device, and then gate voltage has higher efficiency to control the channel surface potential. It is also clear that stack gate dielectric and conductive spacer can relax the I_{off} degradation. Longer L_{ov} results in severer I_{off} degradation. These trends on SOI device are consistent with those on bulk device. If

the L_{ov} can be controlled to be 1 nm, simple stack gate dielectric scheme can reduce the I_{off} degradation factor to two even if the K-value of high-*k* dielectric is 100. It is expected that the novel device structures such as ultra-thin body SOI, double gate SOI, as well as FinFET can further improve the I_{off} degradation.

9-4 Conclusion

In this work, TCAD tools were used to investigate the FIBL effect at sub-45nm technology node and beyond comprehensively. The effect of device structure was also examined. Although the FIBL effect becomes more pronounced as gate length becomes shorter, the I_{off} degradation due to FIBL from drain side will be partly compensated by the FIBS from source side if the spacer length scales down with the gate length. The key factor to affect the FIBL effect is the gate to drain overlap length. Most of the fringing field originating from this region. Since the overlap length must be reduced to control short channel effect, it is expected that the FIBL effect can be further relaxed. Because the overlap length plays important role, high-*k* material existing under spacer does not affect FIBL apparently if K-value does not exceed 50. This result implies that the most promising high-*k* candidate – HfO_2 can be removed after spacer formation. The device integration can be easier.

It is known that stack gate dielectric scheme with a buffer SiO_2 layer between high-*k* dielectric and Si substrate can relax the FIBL effect. This work reveals that a medium K-value buffer layer, for example Hf-silicate, still has the same influence. Conductive spacer is another effective method to reduce FIBL effect but the process is more complicate.

Fully depleted SOI device shows better resistance to FIBL induced I_{off} degradation due to the better control ability of gate electrode on channel surface potential. Simple fully-depleted SOI device can reduce the I_{off} degradation factor to two at L_g=25nm and *k*=100 using stack gate dielectric scheme. It is expected that the ultra-thin body SOI, double gate SOI, and FinFET will exhibit even stronger FIBL effect resistance. Therefore, it is concluded that although FIBL effect can not be eliminated, its impact on device performance is diminished at sub-45nm technology node and beyond under suitable device structure.

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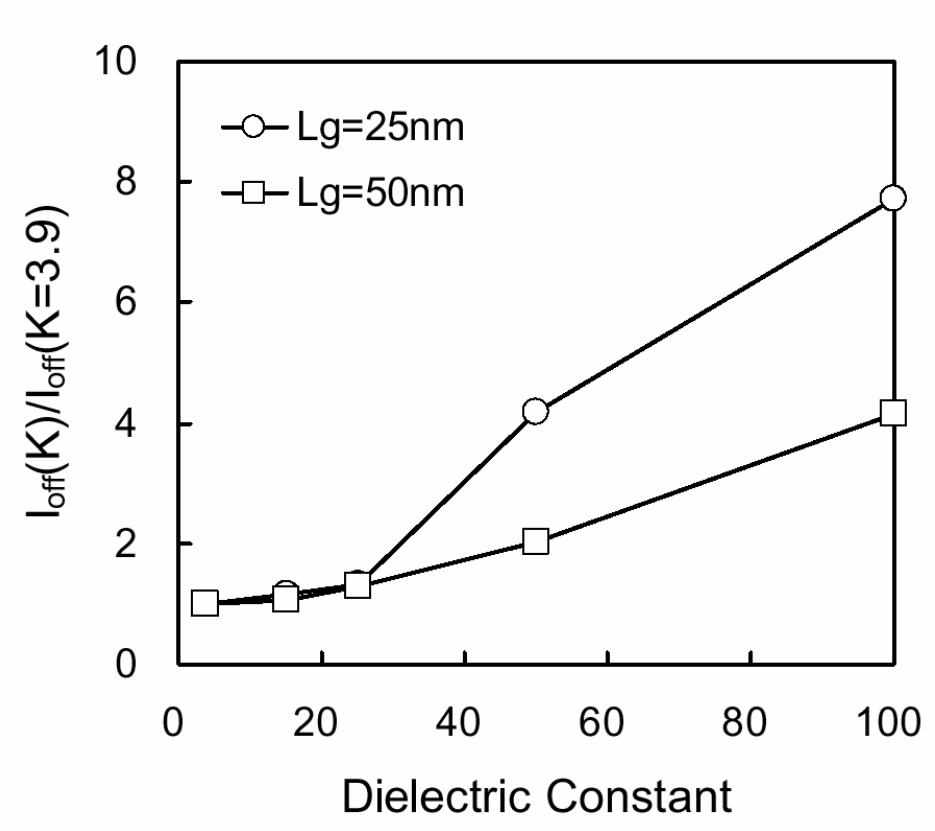


Fig.9-1. The FIBL induced I_{off} degradation as a function of dielectric constant of gate insulator at L_g=50 nm and 25 nm. The simulation parameters are : L_g=25nm, L_{sp}=25nm, L_{ov}=1nm, and EOT=1nm.

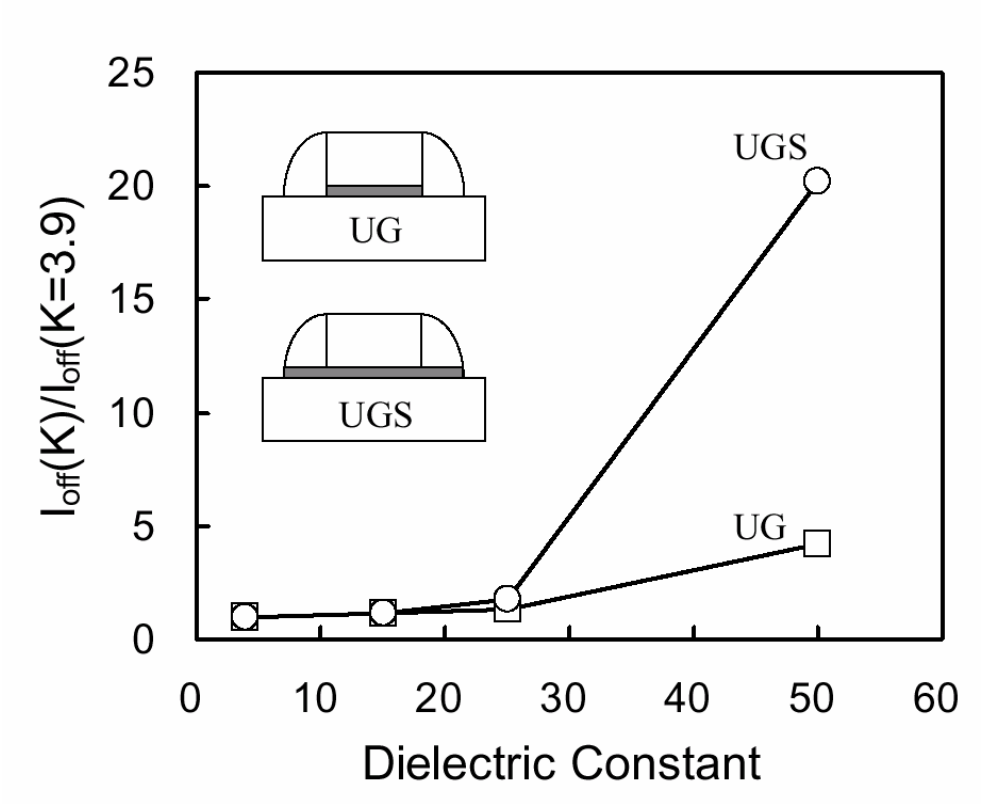


Fig.9-2. The FIBL induced I_{off} degradation as a function of dielectric constant of gate insulator of two different device structures. The inset shows the UG structure and the UGS structure. The UG structure has high-*k* dielectric under gate electrode only and the UGS structure has high-*k* dielectric under spacer also. The other simulation parameters are : L_g=25nm, L_{sp}=25nm, L_{ov}=1nm, and EOT=1nm.

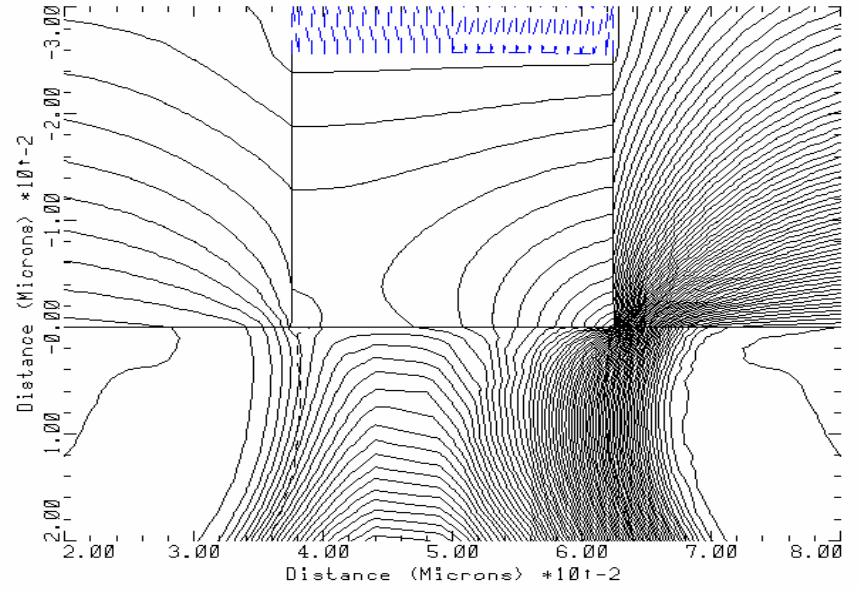


Fig.9-3. The equal potential contours of devices with L_{ov}=1nm. The other simulation parameters are : *k*=100, EOT=1nm, L_g=50nm, and L_{sp}=25nm.

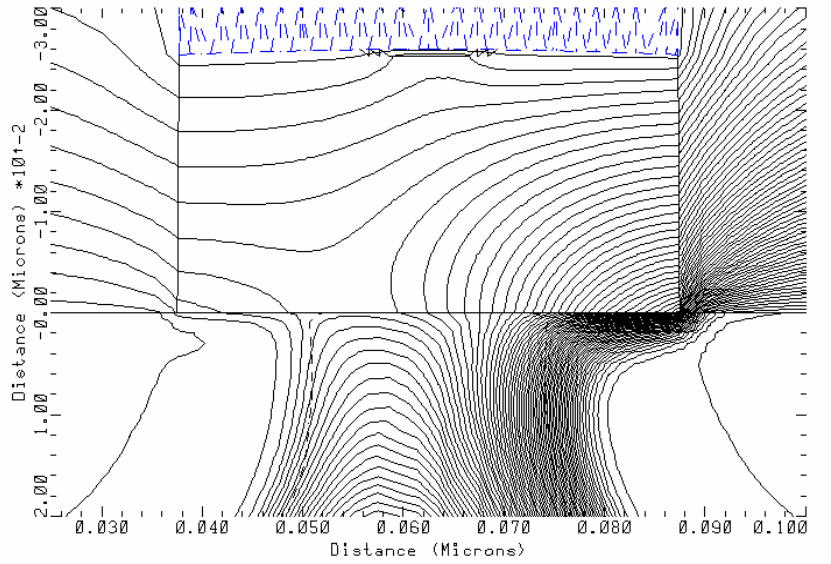


Fig.9-4. The equal potential contours of devices with L_{ov}=13.5nm. The other simulation parameters are : *k*=100, EOT=1nm, L_g=50nm, and L_{sp}=25nm.

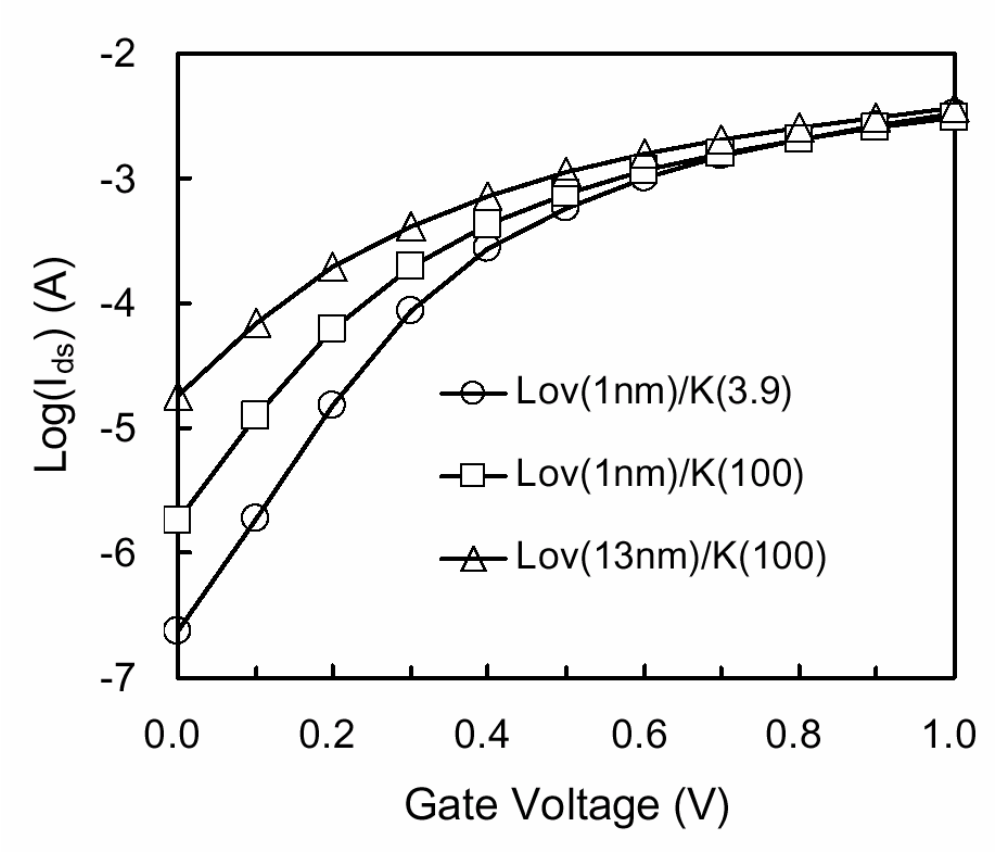


Fig.9-5. Simulated I-V characteristics of devices with various L_{ov} and *k* value. The other simulation parameters are : L_{sp}=25nm and EOT=1nm.

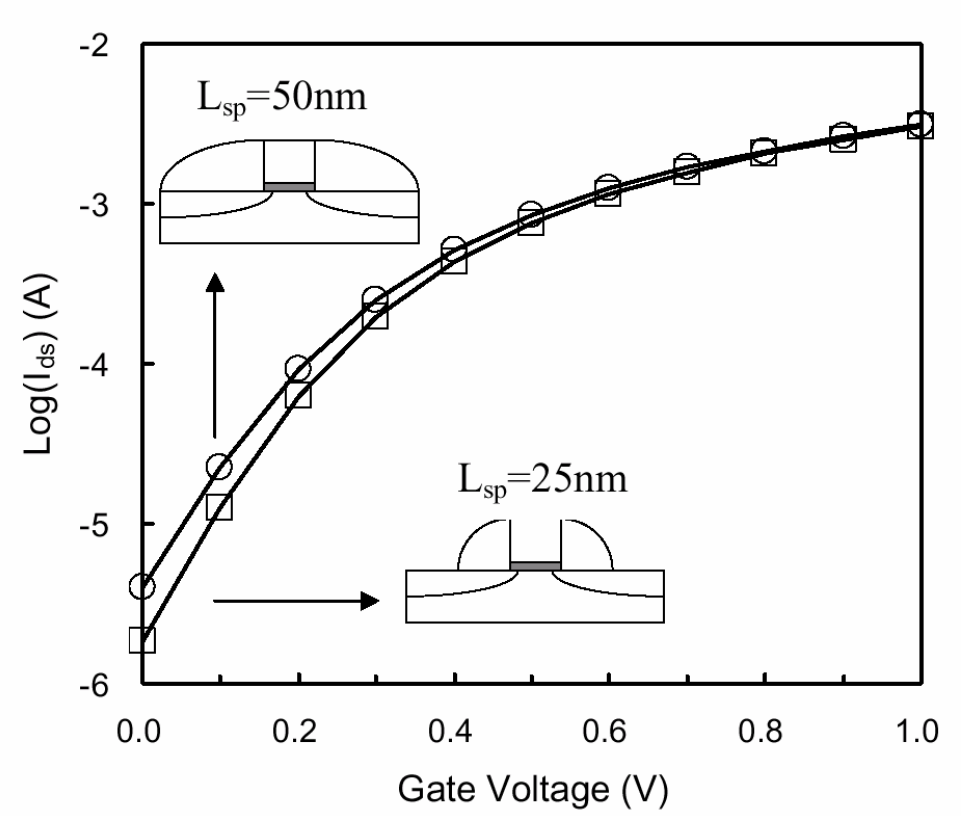
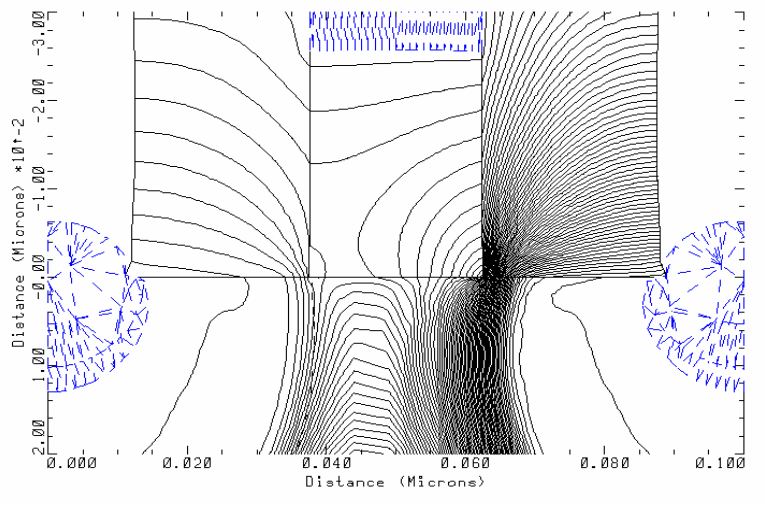


Fig.9-6. Simulated I-V characteristics of devices with various L_{sp}. The other simulation parameters are : k=100, EOT=1nm, L_g=25nm, and L_{ov}=1nm.

(a)



(b)

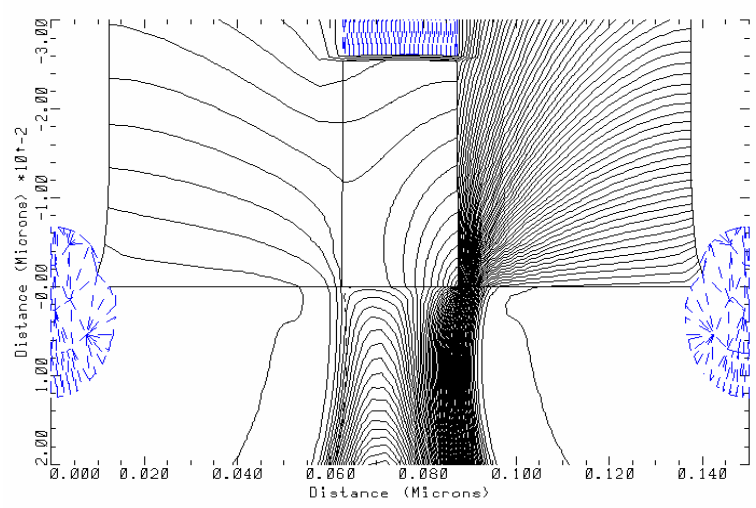


Fig.9-7. The equal potential contours of devices with (a) L_{sp}=25nm and (b) L_{sp}=50nm. The other simulation parameters are : k=100, EOT=1nm, L_g=25nm, and L_{ov}=1nm.

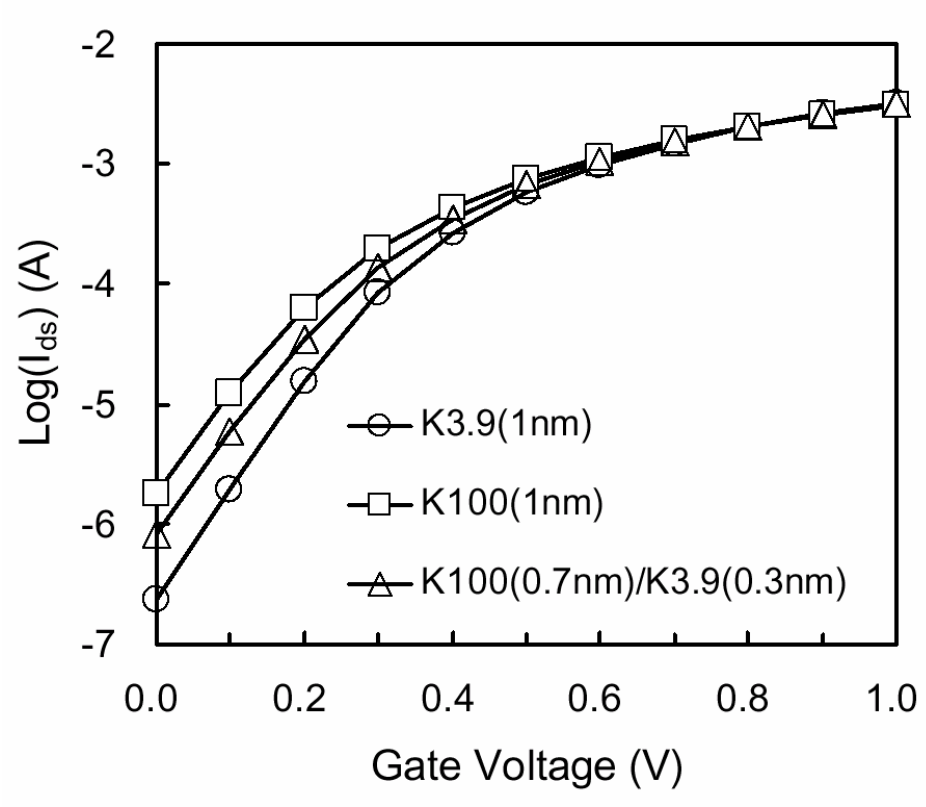


Fig.9-8. Simulated I-V characteristics of devices with various gate dielectric structures. The simulation parameters are : L_g=25nm, L_{sp}=25nm, L_{ov}=1nm, and EOT=1nm.

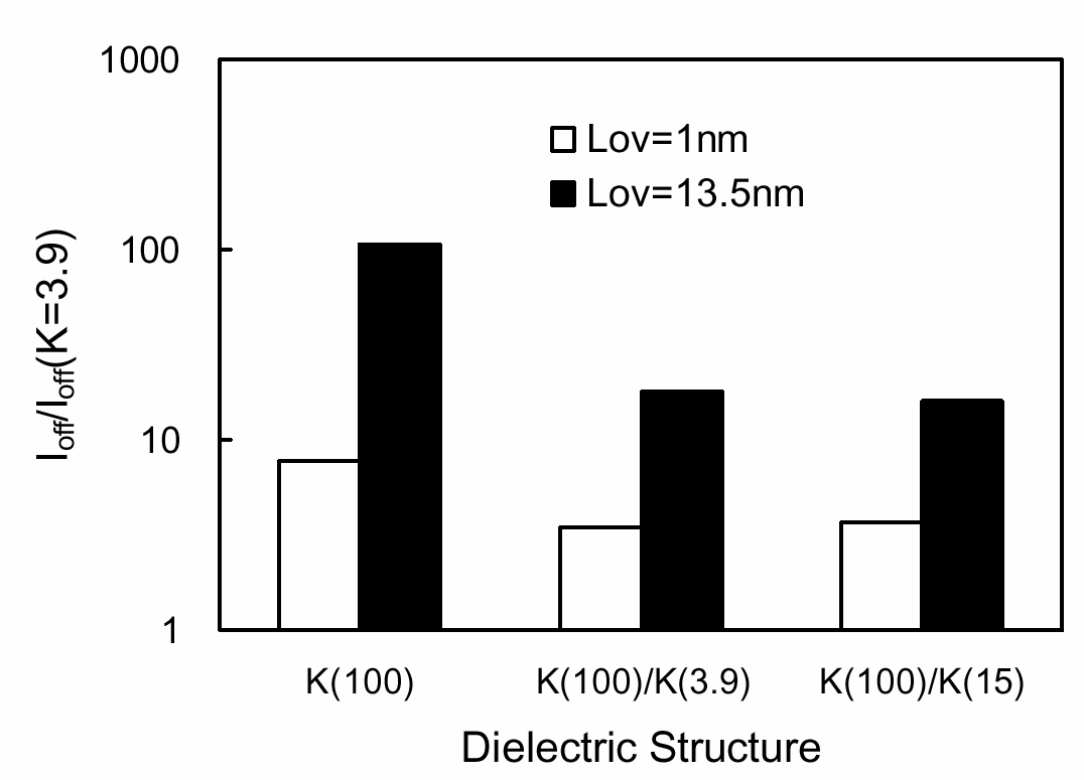
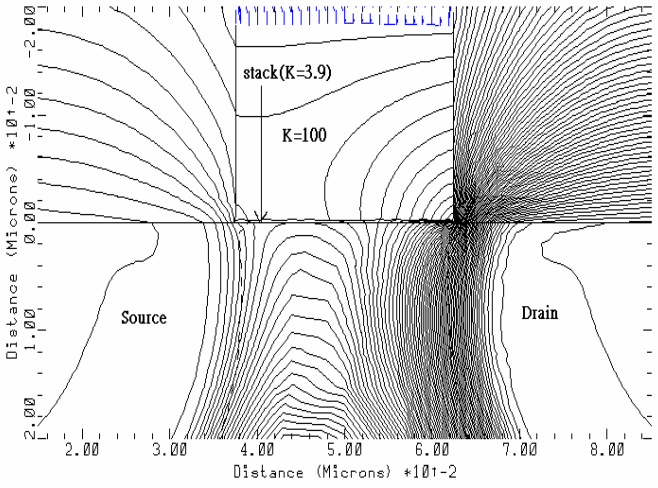


Fig.9-9. The FIBL induced I_{off} degradation of devices with various gate dielectric structures and various L_{ov}. The EOT of buffer layer is fixed at 0.3nm and the *k* value of high-*k* layer is 100. The total EOT of stack gate dielectric is fixed at 1nm. The other simulation parameters are : L_g=25nm and L_{sp}=25nm.

(a)



(b)

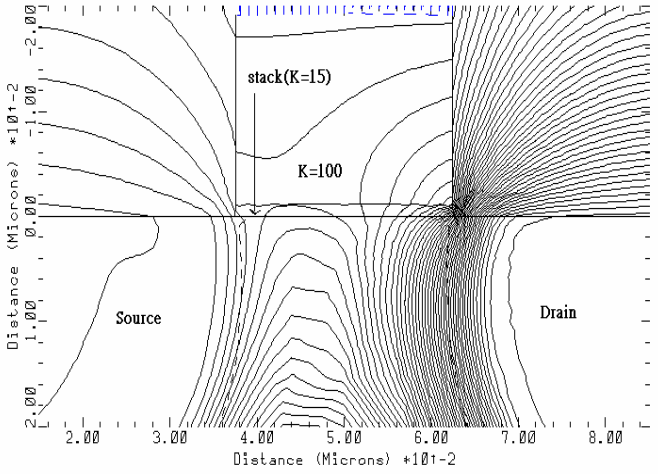


Fig.9-10. The equal potential contours of devices with different buffer layer *k* values of (a) 3.9 and (b) 15. The EOT of buffer layer is fixed at 0.3nm and the *k* value of high-*k* layer is 100. The total EOT of stack gate dielectric is fixed at 1nm. The other simulation parameters are : L_g=25nm and L_{sp}=25nm.

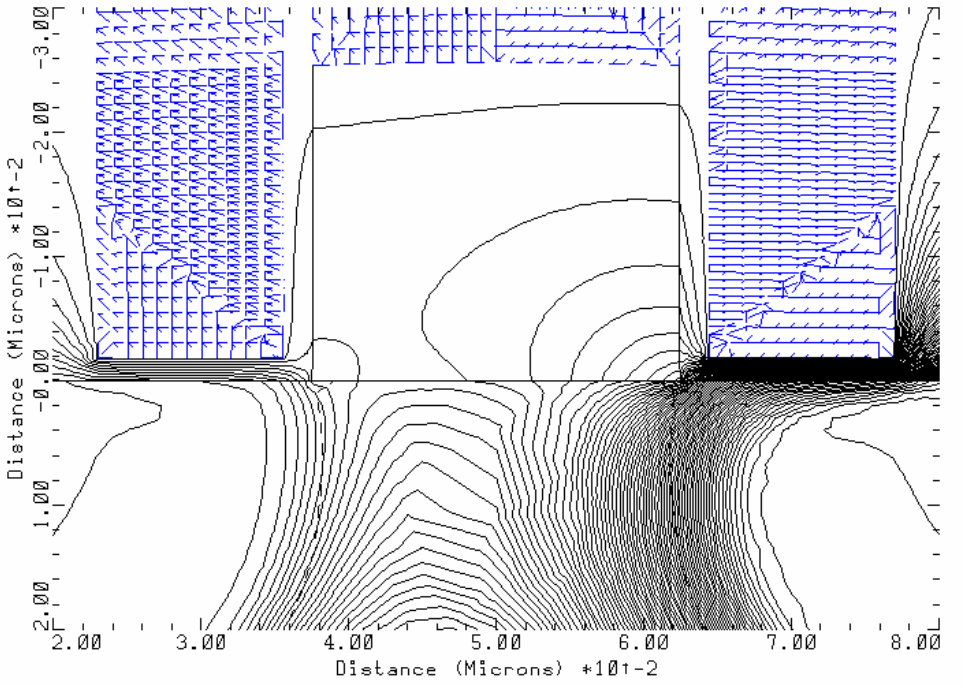


Fig.9-11. The equal potential contours of device with conductive spacer. The simulation parameters are : L_g=25nm, L_{sp}=25nm, L_{ov}=1nm, and EOT=1nm.

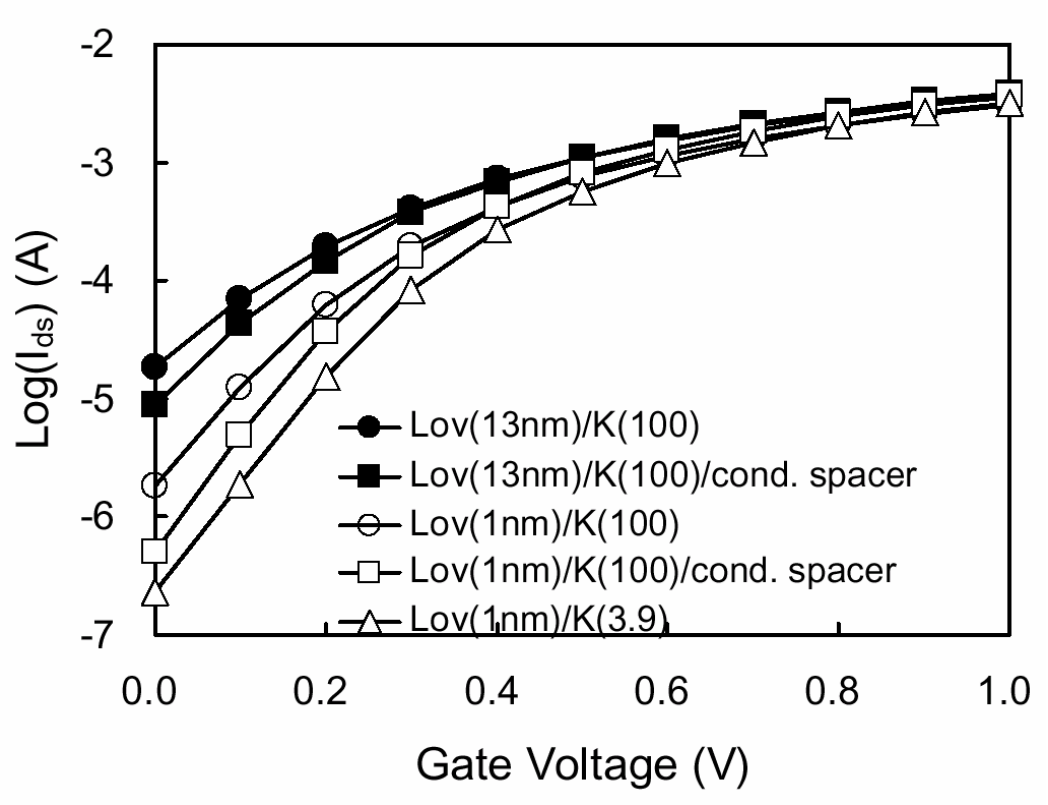


Fig.9-12. Simulated I-V characteristics of devices with and without conductive spacer with L_{ov}=1nm and 13nm. The other simulation parameters are : L_g=25nm, L_{sp}=25nm, and EOT=1nm.

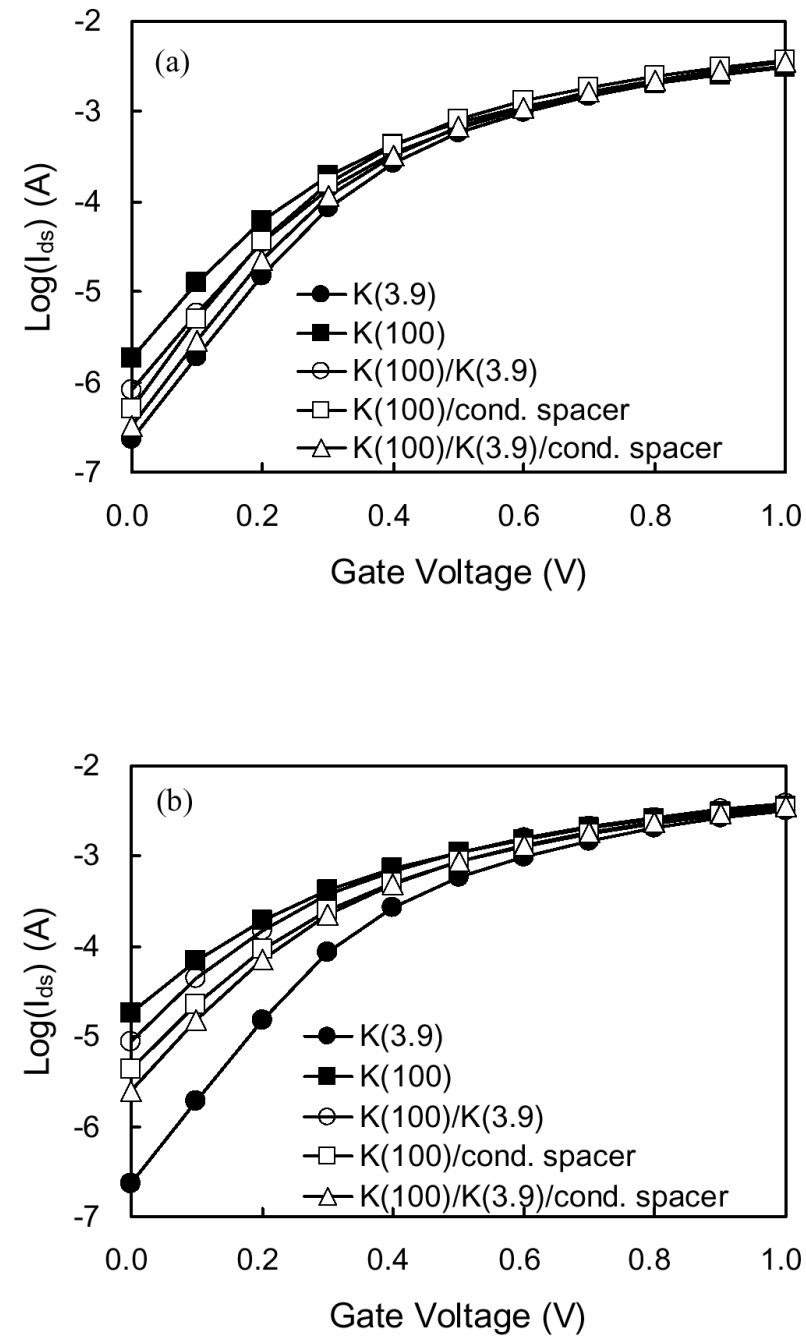


Fig.9-13. Simulated I-V characteristics of devices with various gate dielectric and spacer structures. The L_{ov} is 1nm and 13.5nm in (a) and (b) respectively. The other simulation parameters are : L_g=25nm, L_{sp}=25nm, and EOT=1nm.

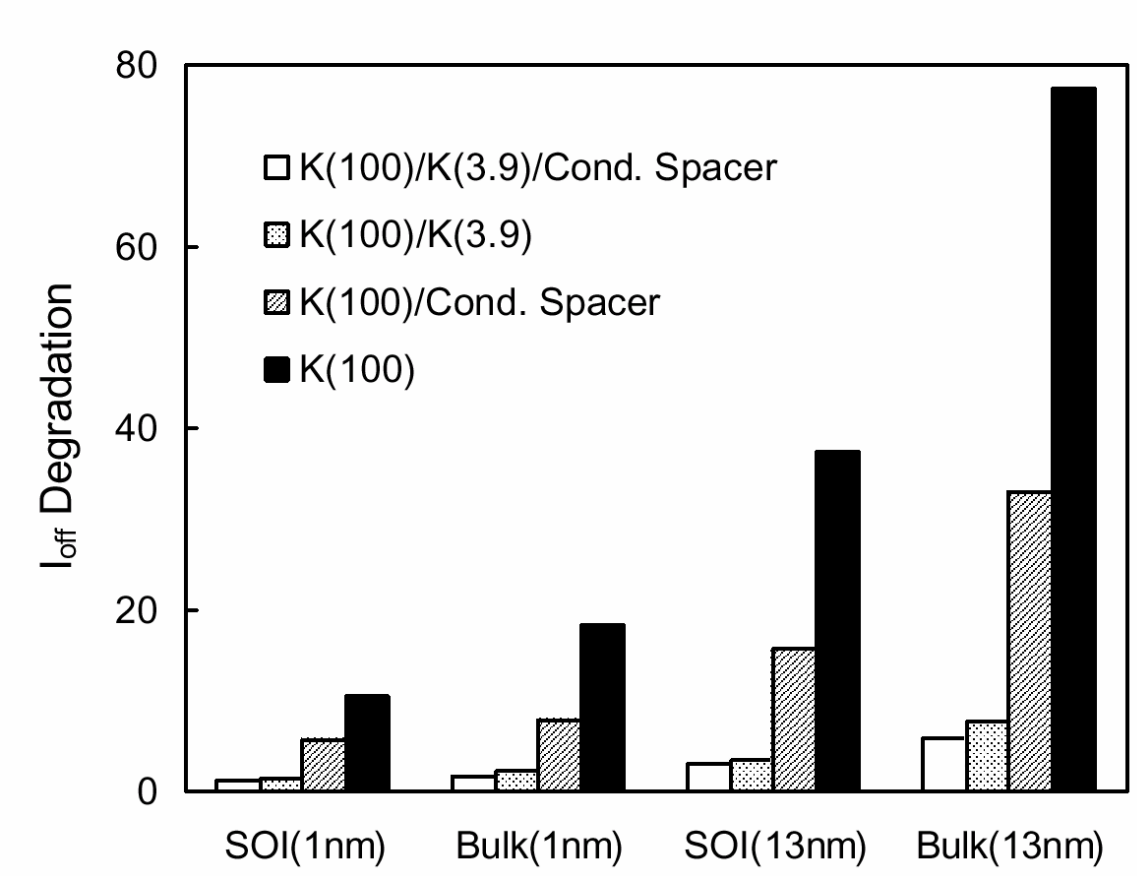


Fig.9-14. The FIBL induced Ioff degradation of SOI devices and bulk device. The simulation parameters are : EOT=1nm, L_g=25nm, and L_{sp}=25nm.

Chapter 10
A Study on Hafnium Contamination

10-1 Introduction

Most high-k materials, including HfO_2, belong to metal oxides, and metal contamination issue must be considered carefully. Metal contamination may come from equipment itself. It had been published that wafer surface becomes rough after standard RCA clean in hafnium-contaminated solution so that gate oxide integrity is degraded [1]. No literature studies metal contamination issues from the metal oxide on device. The self-contamination is very important to determine the device integration scheme.

High-k material is difficult to be etched by either dry etch or wet etch especially for thin film after high temperature annealing [2]. It is hard to remove HfO_2 film after gate electrode etching because dry etching of HfO_2 may damage the S/D extension region and wet etching of HfO_2 exhibit very poor selectivity between high-k dielectric and field oxide. Hf element been knocked into source/drain or field oxide during ion implantation for source/drain extension may be a concern in device fabrication, illustrating in Fig.10-1. Metal could be generation-recombination center in Si and mobile ion or oxide trap in field oxide, and then causes larger junction leakage current and degrades field oxide stability, respectively. Some experiment about hafnium contamination from the deposited HfO_2 itself on device characteristics will be performed in this chapter to evaluate the feasibility of leaving HfO_2 film until spacer etching.

Two parts of experiments about the impact of hafnium contamination on device characteristics were performed. In the first part, p-n junction diodes are used to examine the impact of knocked-in Hf elements on the junction characteristics. In the second part, metal/field oxide/Si (MOS) structure is used to study the impact of knocked-in Hf element on the electrical stability and strength. The depth distribution of Hf after implantation and after drive-in is simulated with a Monte-Carlo simulator of TRIM and analyzed by Secondary-Ion-Mass-Spectroscopy (SIMS).

10-2 Experimental Procedure

10-2-1 P^+N Junction

The p^+n junction diodes were fabricated on 4-inch n-type (100)-oriented silicon wafers with 8~12 O-cm nominal resistivity. After standard RCA cleaning, a 500 nm thick SiO_2 was thermally grown in a pyrogenic oxidation system. Circular active regions with area of $3.22x10^{-3}$, $8.05x10^{-4}$, $2.01x10^{-4}$, and $5.03x10^{-5}cm^2$ were defined by conventional photolithography technique and chemical wet etching in buffered-oxide-etchant (BOE). About 2nm thick HfO_2 was deposited in a sputtering system. The p^+ layer was formed by BF_2^+ implantation through the HfO_2 layer at an energy of 20 or 40KeV with a dose of $2x10^{15}\,cm^{-2}$. Junctions without HfO_2 layer during ion implantation were prepared as reference. For type-A samples, HfO_2 layer was removed by HF-contained solution before activation annealing. For type-B samples, activation annealing was performed before HfO_2 layer removal. The activation annealing temperature is 850℃, 900℃, 950℃, or 1000℃ in N_2 ambient for 30sec in a rapid thermal annealing (RTA) system. Aluminum of 500 nm thick was evaporated and patterned by typical photolithography and wet etching processes as electrode. After backside metallization with Al, a 400℃ N_2 annealing finished the fabrication process. The process flow of p^+n junction diode is illustrated in Fig.10-2. The sample identifications and process conditions were summarized in Table 10-1.

The depth profiles of implanted species and the knocked-in Hf atoms before annealing were simulated with Monte-Carlo simulator (TRIM code, Transport of Ions in Matters). After annealing, junction depth and Hf-distribution were examined with Secondary Ion Mass Spectroscopy (SIMS). Both forward and reversed biased current-voltage (I-V) characteristics were measured with a semiconductor parameter analyzer of model Agilent 4156C. Ideality factor at forward bias and leakage current components at reverse bias were analyzed to understand the effect of HfO_2 layer on junction integrity.

10-2-2 MOS Capacitor

MOS capacitor (MOS-C) structure was used to investigate the effect of Hf on field oxide. The boron doped (100)-oriented silicon wafer with 10-25O-cm nominal resistivity was used. After standard RCA cleaning, a 30 nm dry oxide was thermally grown in dry O_2 ambient. A 300 nm thick and 100 nm thick PE-TEOS oxide was deposited for mobile ion measurement and breakdown field (E_{bd}) measurement, respectively. Then, Hafnium dioxide of 2 nm thick was deposited in a sputtering system followed by an As^+ implantation at 15, 20, 30, and 40 keV to a dose of $2x10^{15}\ cm^{-2}$. Rapid thermal annealing in N_2 ambient at 850℃,900℃,950℃, and 1000℃ for 30 sec was used to repair oxide damage due to ion implantation and drive hafnium into field oxide. Samples without HfO_2 layer and/or without ion implantation were

prepared as references. The metallization processes to form frond side electrode and backside contact are identical to those used to fabricate p^+n junction. The process flow of the MOS-C is illustrated in Fig.10-3. The sample identifications and process conditions were summarized in Table 10-2.

Flat-band voltage (V_{FB}) was extracted from the high frequency C-V characteristic measured with a precision impedance meter of model Agilent 4284 at a frequency of 100 KHz. Breakdown field was measured with a semiconductor parameter analyzer of model Agilent 4156C.

10-3 Results and Discussion

10-3-1 Junction Characteristics

A. TRIM Simulation

To understand how many and how deep the Hf element could be knocked into Si substrate during ion implantation, TRIM code was employed to observe the depth profile of Hf after implantation with different species and energies. Fig.10-4 shows the simulated results of B profile and knocked hafnium profile. From the simulation results, hafnium locates at the shallow surface of the silicon, which is much shallower than the junction depth of boron. Furthermore, the hafnium depth profile is almost regardless of implantation energy at the same implantation species due to the heavy weight of Hf element. It is thus expected that the knocked-in Hf element will not affect junction properties since Hf is not fast diffuser in Si matrix.

B. Forward Bias Characteristics

The current-voltage characteristics of p^+n junction diodes can be expressed by the celebrated Shockley Equation:

$$I_F = I_S [e(qV_F/nkT) – 1]$$

, where V_F is the forward bias voltage, k is the Boltzmann constant, T is the absolute temperature at measurement, and the factor n is called ideality factor. As qV>>kT, the above equation can be simplified as $I_F \sim I_S [e(qV/nkT)]$, so that the ideality factor n is equal to (q/kT)[? V / ? (lnJ)]. The forward current of p^+n junction is composed of two current components: diffusion current and recombination current. An ideality factor of unity indicates diffusion current dominant while a value of 2 indicates recombination current within depletion region dominant. Thus, the ideality factor is an indicator revealing the quality of Si

crystal near the metallurgical junction.

Fig.10-5 shows the forward ideality factor versus post implantation annealing temperature of the reference sample and the HfO_2 capped samples after BF_2^+ implantation at 20 keV and 40 keV to a dose $2x10^{15}$ cm^{-2}. It is observed that the ideality factors of all of the samples are lower than 1.05. This result indicates that the forward current is diffusion current dominant, i.e. no Hf contamination near metallurgical junction. This result is reasonable because it is hard to knock Hf into Si during implantation (as shown in Fig.10-4) and to make Hf diffuse in silicon during typical thermal treatment. Furthermore, the depletion width at forward bias is so narrow to involve the knocked hafnium region so that the effect of these knocked-in Hf is negligible. Since all of the extracted values are lower than 1.05 and no consistent trend is observed with annealing temperature and implantation energy in our results, the scattering of ideality factor may be due to the process deviation and/or numerical calculation.

C. Reverse Bias Characteristics

In this sub-section, the reverse bias leakage current density of the reference and HfO_2 capped p^+n junction diodes (REF, type-A, and type-B) were measured and discussed. All measurement was made at room temperature, and at least fifteen randomly chosen diodes of each process condition were measured to build the cumulative distribution. The noise and leakage current of the measurement system were kept below 50fA.

Fig.10-6 and 10-7 show the cumulative plots of reverse current density measured at -5 volts of REF, Type-A, and Type-B junctions with implantation energy of 20 keV and 40 keV, respectively. The cumulative distributions of all process conditions are similar. The leakage current densities of all samples are lower than $5nA/cm^2$. This result satisfies the requirement of IC application well.

The total reverse current (for $p_{n0} >> n_{p0}$ and $| V | > 3kT/q$) can be approximately given by the sum of the diffusion components in the neutral region and the generation current in the depletion region:

$$J_R = q (D_p/t_p)^{1/2} (n_i^2 / N_D) + (qn_iW /t_e).$$

The former term is diffusion current component and the latter term is generation current component. For the generation current, it is proportion to depletion width. The depletion width is inversely proportional to doping concentration. Because p^+ region is heavily doped, the depletion width is narrow even at reverse bias. According to the simulation results, knocked Hf locates far from depletion region, therefore, it is postulated that the knocked-in Hf

still plays no role on the junction leakage current.

D. Area and Peripheral Leakage Current

To further analyze the leakage current, the current was decomposed to two components: the area leakage component (I_{RA}) and the peripheral leakage current component (I_{RP}). The measured leakage current can be expressed in terms of the two components:

$I_R = I_{RA} + I_{RP} = A*J_{RA} + P*J_{RP}$

, where A is the junction area, P is the junction perimeter, J_{RA} is the area component leakage current density, and J_{RP} is the peripheral component leakage current density. Note that reverse leakage current density J_R is defined as I_R/A. By measuring the I_R of junctions with different P/A ratios, the slope of the reverse leakage current density J_R versus P/A plot gives the J_{RP} and the Y-axis intersection gives the J_{RA}.

Fig.10-8 shows the J_R versus post activation temperatures for REF, Type-A, and Type-B junctions. Fig.10-9 and 10-10 show the J_{RA} and J_{RP} versus annealing temperature of these devices, respectively. It is observed that neither the area component nor the peripheral component show consistent trend with process conditions. In some case, Type-A or Type-B junctions show higher leakage current than the REF junctions but vice versa in another cases. It is thus concluded that the existence of HfO_2 layer on junction area before S/D implantation has no adverse effect on the junction integrity.

10-3-2 MOS-C Structure

Fig.10-11 shows the Hf distribution of the HfO_2/PE-TEOS structure after ion implantation. Similar to that of the HfO_2/Si structure, the knocked-in Hf only distributed at the very shallow surface. Furthermore, the depth of Hf shows very weak dependence on implantation energy. Fig.10-12 shows the flat-band voltage of all samples with various implantation energies and annealing temperatures. It is observed that at any process conditions, the reference and HfO_2-capped MOS-C have almost identical V_{FB} value. This result indicates that although Hf is knocked-into PE-TEOS oxide, it may not be a charged impurity in oxide so that the V_{FB} is not shifted. Another possible reason about why V_{FB} is not affected is that these Hf atoms distribute too close to the metal electrode such that they have diminished effect on V_{FB} even if they are charged.

At the same implantation energy, the magnitude of V_{FB} decreases with the increase of annealing temperature due to the net elimination of positive charges in the PE-TEOS oxide. These positive charges may exists in the as-deposited PE-TEOS film or be generated by ion

implantation induced damages. The slopes of V_{FB} versus annealing temperature of the reference and HfO_2-capped samples at all of the four implantation energies are very close. This phenomenon implies that the positive charges are irrelevant to the knocked-in Hf atoms.

Fig.10-13 shows the E_{bd} of all samples. It is observed that at the same implantation energy, the E_{bd} of the reference samples and the HfO_2-capped samples are similar, even if after annealing at different temperatures. Since E_{bd} depends on the defects in oxide, we conclude that although hafnium is knocked into field oxide by implantation, it may not cause sufficient charged or defects to affect the field oxide quality.

10-4 Summary

In this chapter, we used p^+n junction diode and MOS capacitor to investigate the effect of post-HfO_2 deposition process on device characteristics. Although hafnium is knocked-into silicon and PE-TEOS oxide, it only locates at the very shallow surface of substrate due to its heavy weight. Both forward ideality factor and reverse leakage current of p^+n junction show that the existence of HfO_2 during BF_2^+ ion implantation does not affect the junction characteristics. Fig.10-14 shows the simulated Hf distribution in Si after As^+ implantation and SIMS measured Hf distribution after annealing. The shallow distribution and negligible thermal diffusion predict that the n^+p junction characteristics will not be affected by the existence of HfO_2 layer although we have no electrical data at this moment. The n^+p junction is still under processing. Measurement on MOS-C structure also shows that the existence of HfO_2 on field oxide does not produce mobile ion and oxide defects.

The diffusivity of hafnium is very low in both silicon and silicon dioxide so that we could not observe the effect of hafnium in this experimental structure. All of these results imply that from the contamination point of view, the HfO_2 out of gate electrode have not to be removed immediately after gate patterning. This conclusion greatly relaxes the constraint on device process integration.

In this chapter, we only examine the contamination issue of post-HfO_2 deposition process. In this case, Hf is introduced into silicon substrate or field oxide during S/D implantation if Hf or HfO_2 remains on wafer surface. Hafnium contamination source from the wet-bench or furnace before HfO_2 deposition are not discussed in this scope. To draw final conclusion on the Hf contamination, the pre-HfO_2 deposition contamination issues must be studied also. This is left as future work.

References

[1]. B. Vermeire, K. Delbridge, V. Pandit, H. G. Parks, S. Raghavan, K. Ramkumar, S. Geha, and J. Jeon, “ The effect of hafnium or zirconium contamination on MOS process,” Advanced Semi. Manufacturing 2002 IEEE/SEMI Conference and Workshop, p.299, 2002.

[2]. J. J. Chambers, A. L. P. Rotondaro, M. J. Bevan, M. R. Visokay, and L. Colombo, “Effect of composition and post-deposition annealing on the etch rate of hafnium and zirconium silicate in diluted HF,” Texas Instruments Incorporated Silicon Technology Research Dallas.

Table 10-1. Summary of the sample identification number for contaminated and reference p+n samples (for all samples with BF_2 dose 2E15)

Type / Annealing temp.	Reference		TypeA		TypeB	
	20kev	40kev	20kev	40kev	20kev	40kev
R850℃	R850a	R850b	A850a	A850b	B850a	B850b
R900℃	R900a	R900b	A900a	A900b	B900a	B900b
R950℃	R950a	R950b	A950a	A950b	B950a	B950b
R1000℃	R1000a	R1000b	A1000a	A1000b	B1000a	B1000b

Table 10-2. Summary of the sample identification number for contaminated and reference of isolation investigation (MOS-C) samples (for all samples with As specie dose 2E15).

Type / Annealing temp.	Reference				Contaminated			
	15kev	20kev	30kev	40kev	15kev	20kev	30kev	40kev
R850℃	R850a	R850b	R850c	R850d	C850a	C850b	C850c	C850d
R900℃	R900a	R900b	R900c	R900d	C900a	C900b	C900c	C900d
R950℃	R950a	R950b	R950c	R950d	C950a	C950b	C950c	C950d
R1000℃	R1000a	R1000b	R1000c	R1000d	C1000a	C1000b	C1000c	C1000d

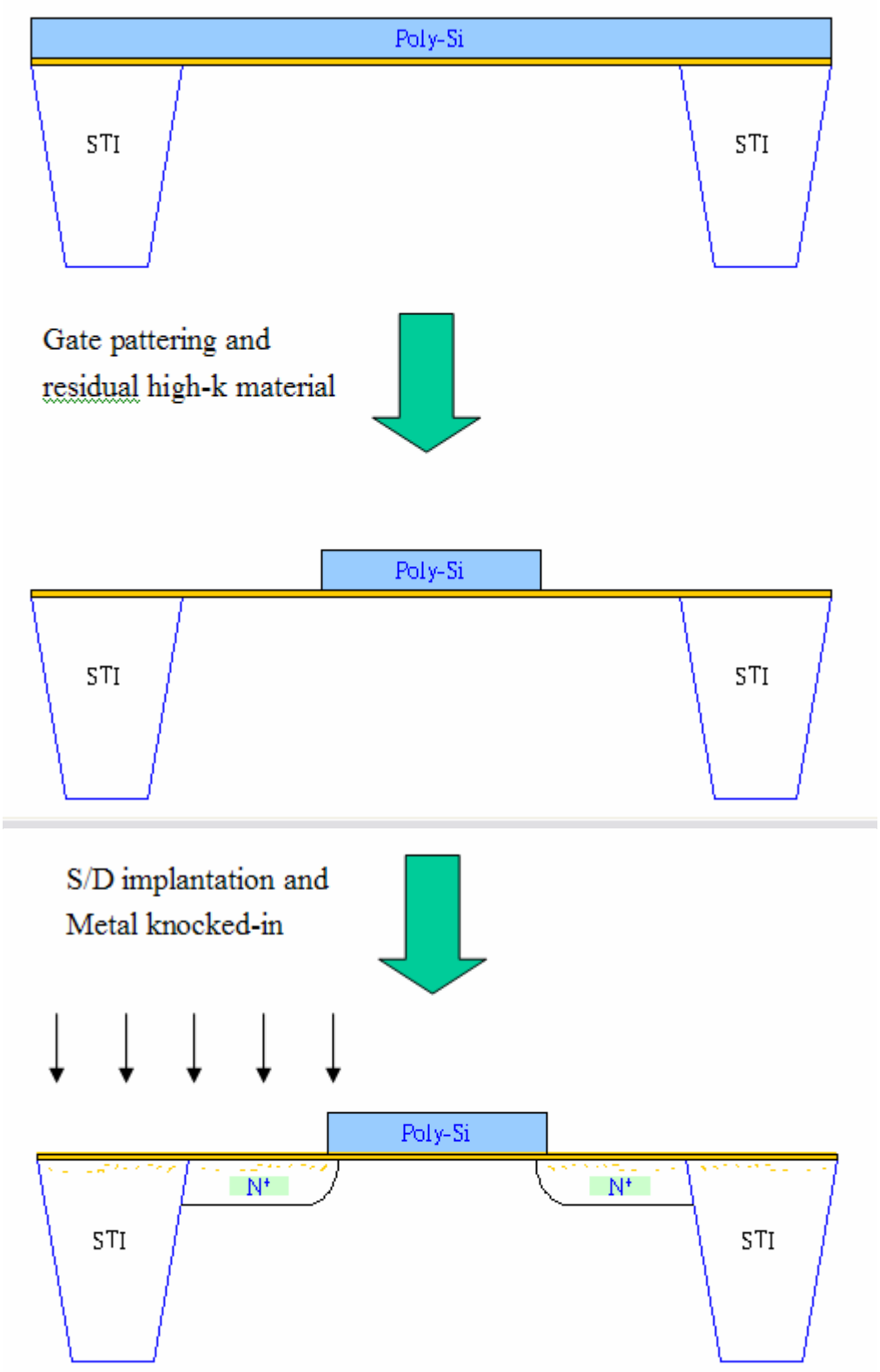


Fig.10-1. Illustrating the metal knocked-into silicon and oxide by implantation.

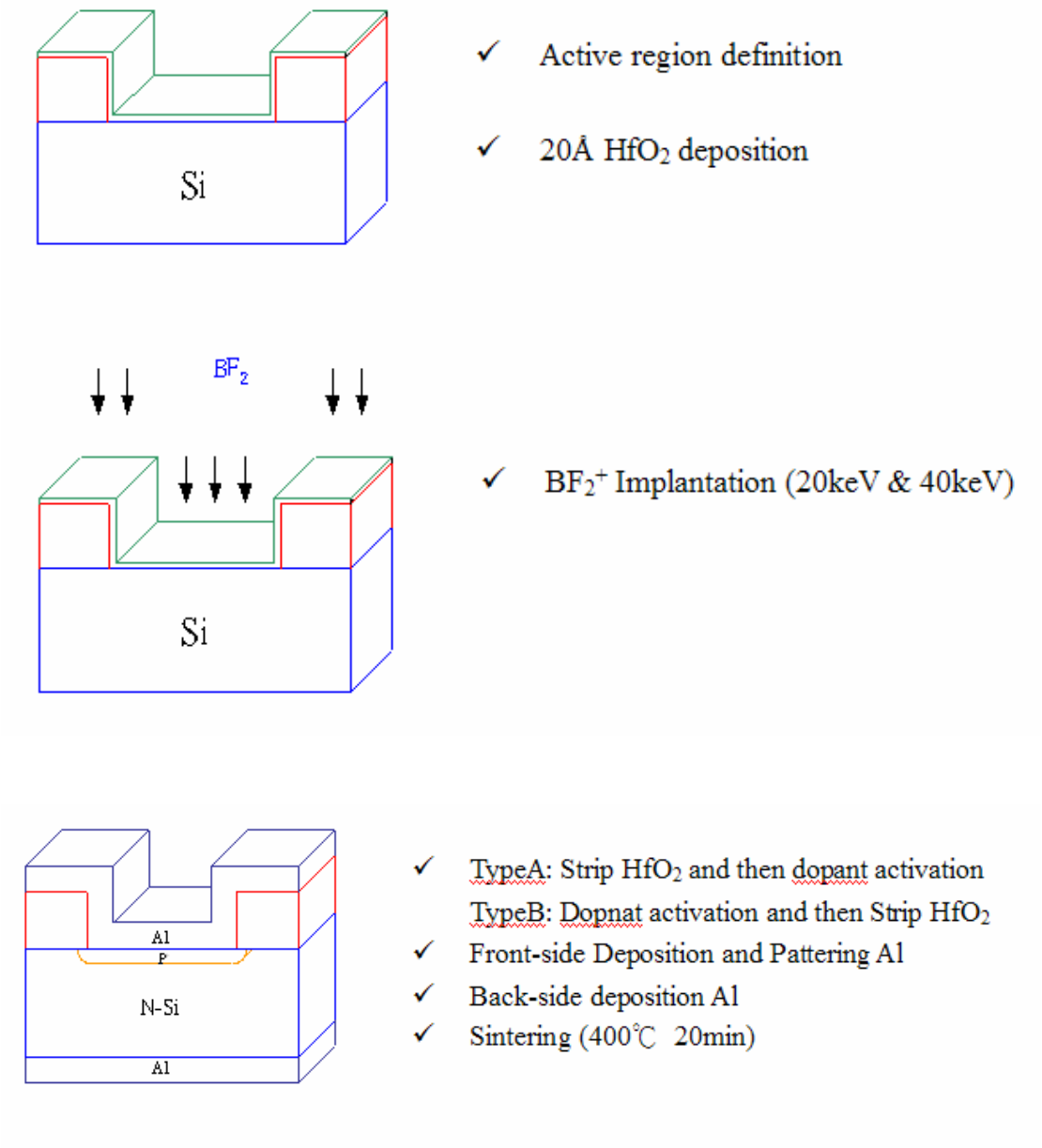


Fig.10-2. The process flow of p^+n junction diode.

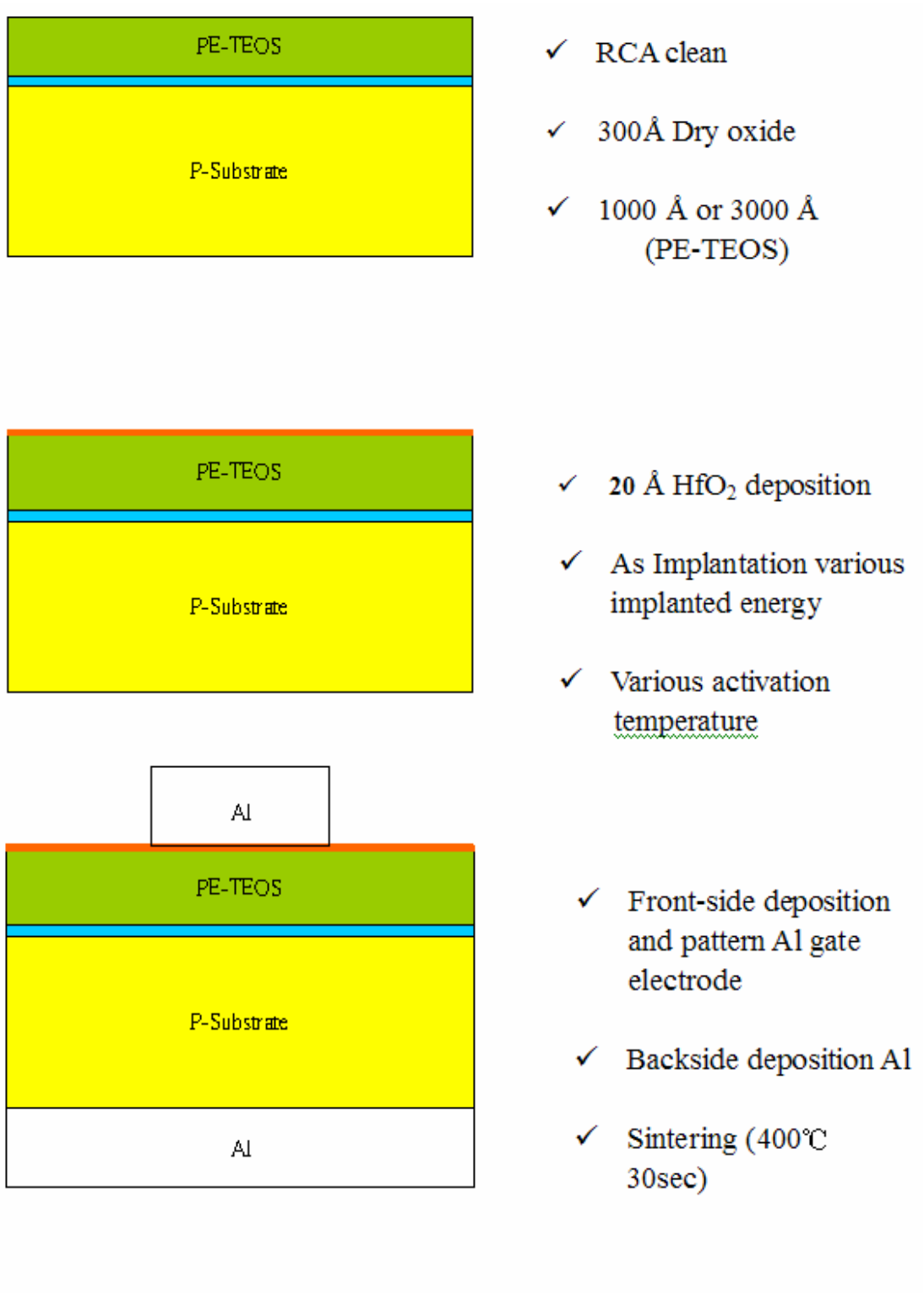


Fig.10-3. The process flow of MOS-C

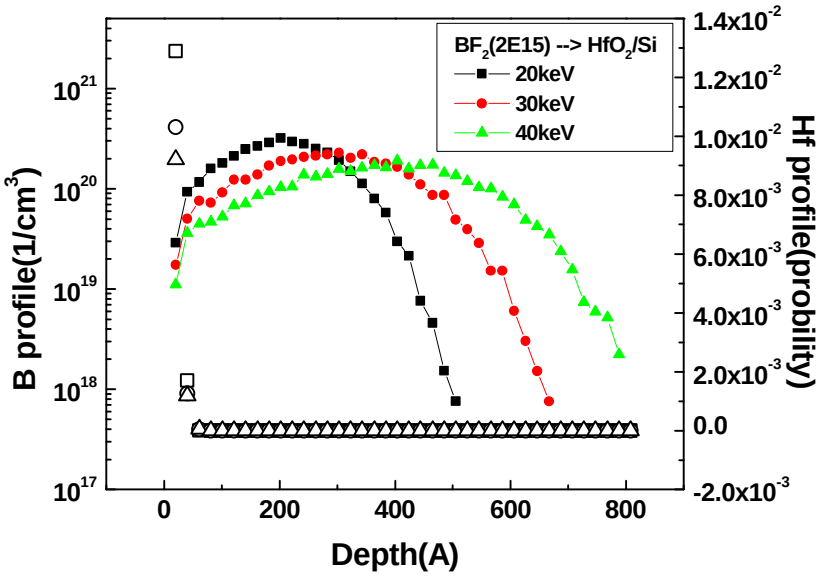


Fig.10-4. The Trim simulation results of B profile with a dosage 2E15(1/cm^2) and knocked hafnium profile.

(Square) Implantation energy 20keV

(Circle) Implantation energy 30keV

(Triangle) Implantation energy 40keV

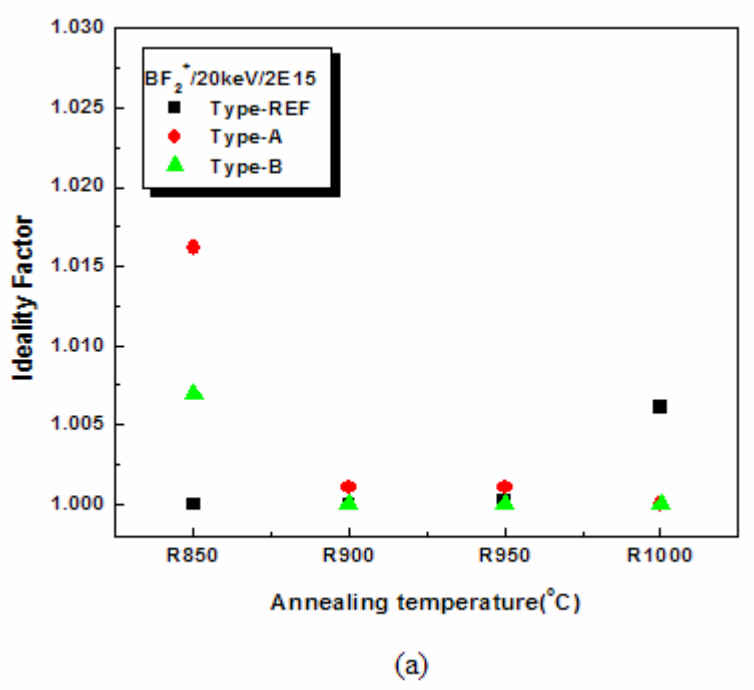


Fig.10-5. Forward ideality factor versus post implantation annealing temperature of the reference sample and the HfO_2 capped samples after BF_2^+ implantation at (a) 20keV, and (b) 40keV to a dose $2x10^{15}$ cm^{-2}.

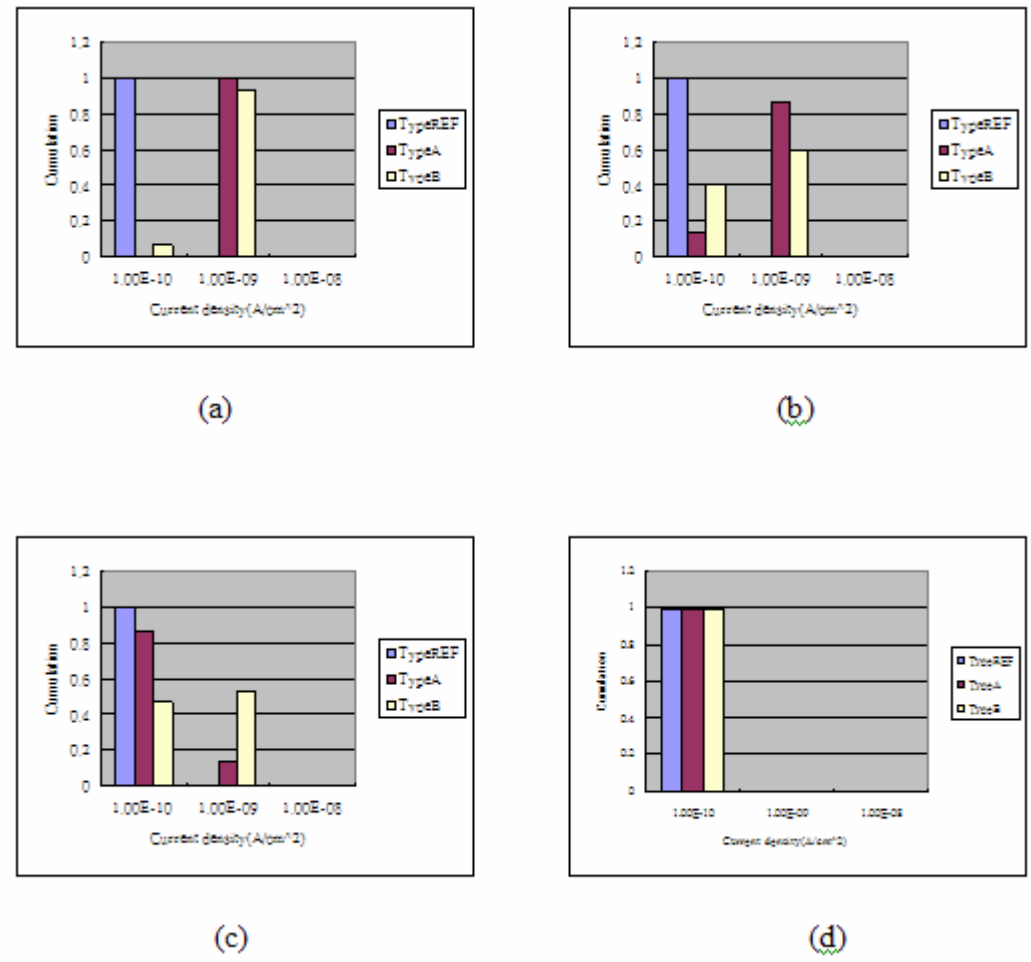


Fig.10-6. Cumulative plots of reverse current density measured at -5 volts of REF, Type-A, and Type-B junctions with implantation energy of 20keV following various activation temperatures: (a) 850℃ 30sec, (b) 900℃ 30sec, (c) 950℃ 30sec, and (d) 1000℃ 30sec

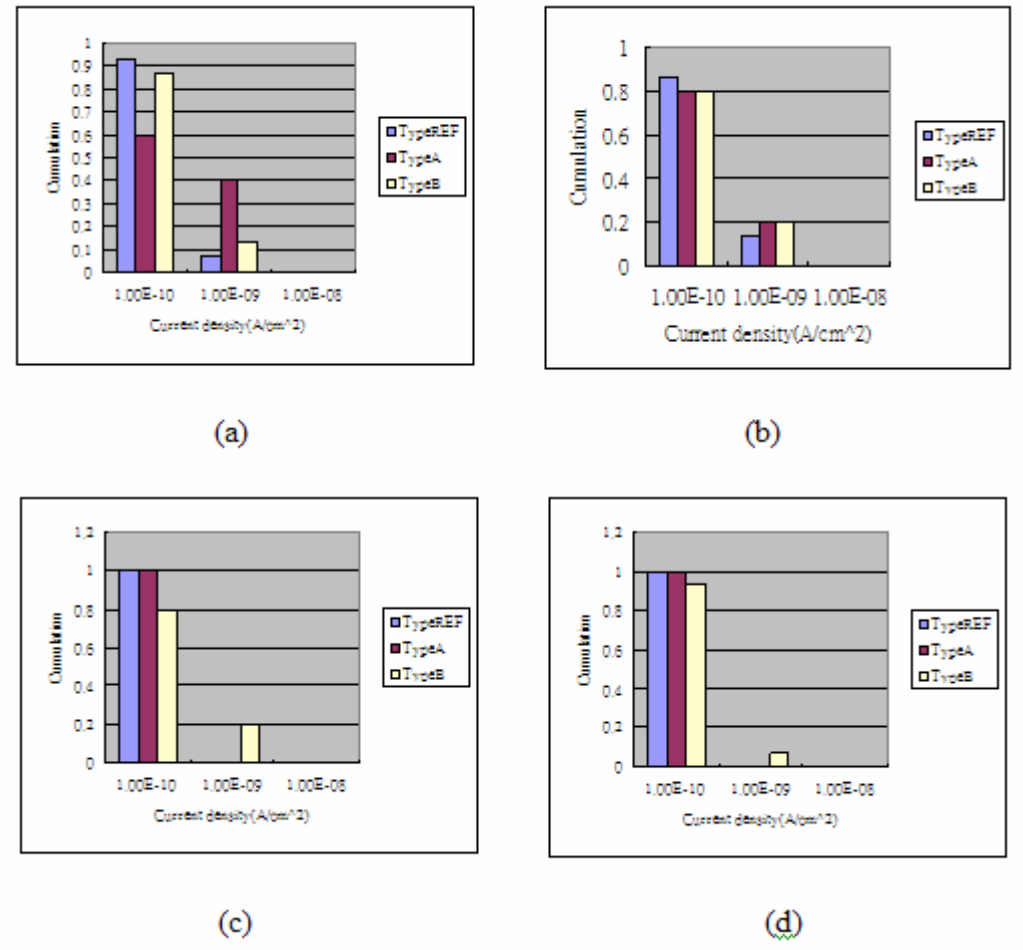
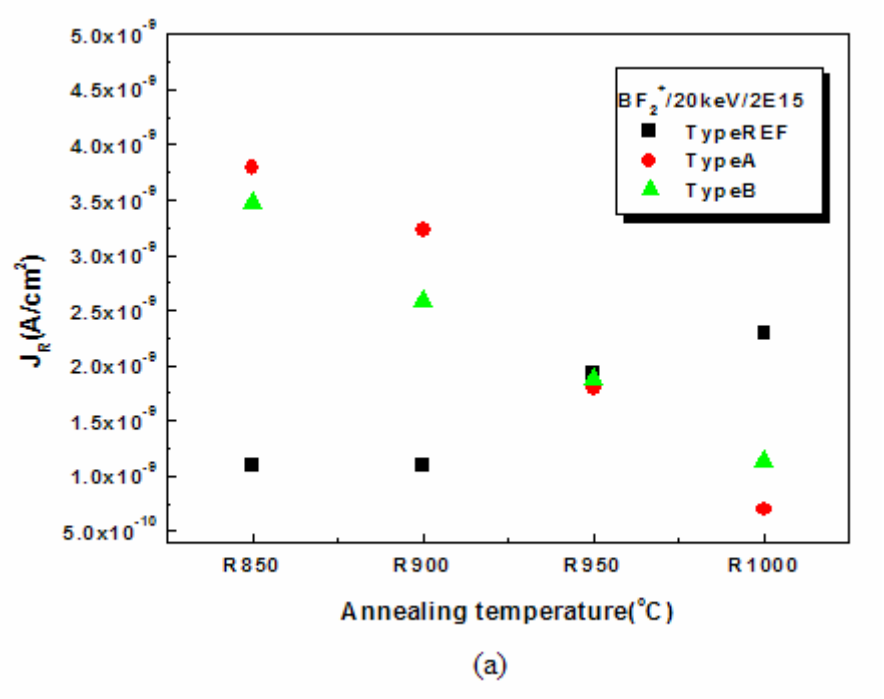
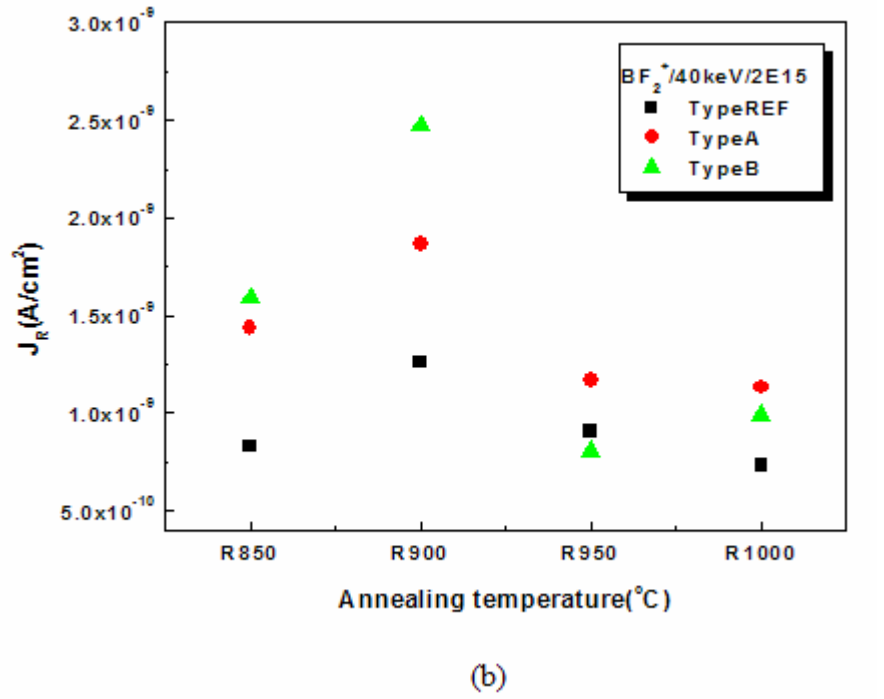


Fig.10-7. Cumulative plots of reverse current density measured at -5 volts of REF, Type-A, and Type-B junctions with implantation energy of 40keV following various activation temperatures: (a) 850℃ 30sec, (b) 900℃ 30sec, (c) 950℃ 30sec, and (d) 1000℃ 30se.



(a)



(b)

Fig.10-8. J_R versus post activation temperatures for REF, Type-A, and Type-B junctions with different BF_2^+ implantation energies (a) 20keV (b) 40keV

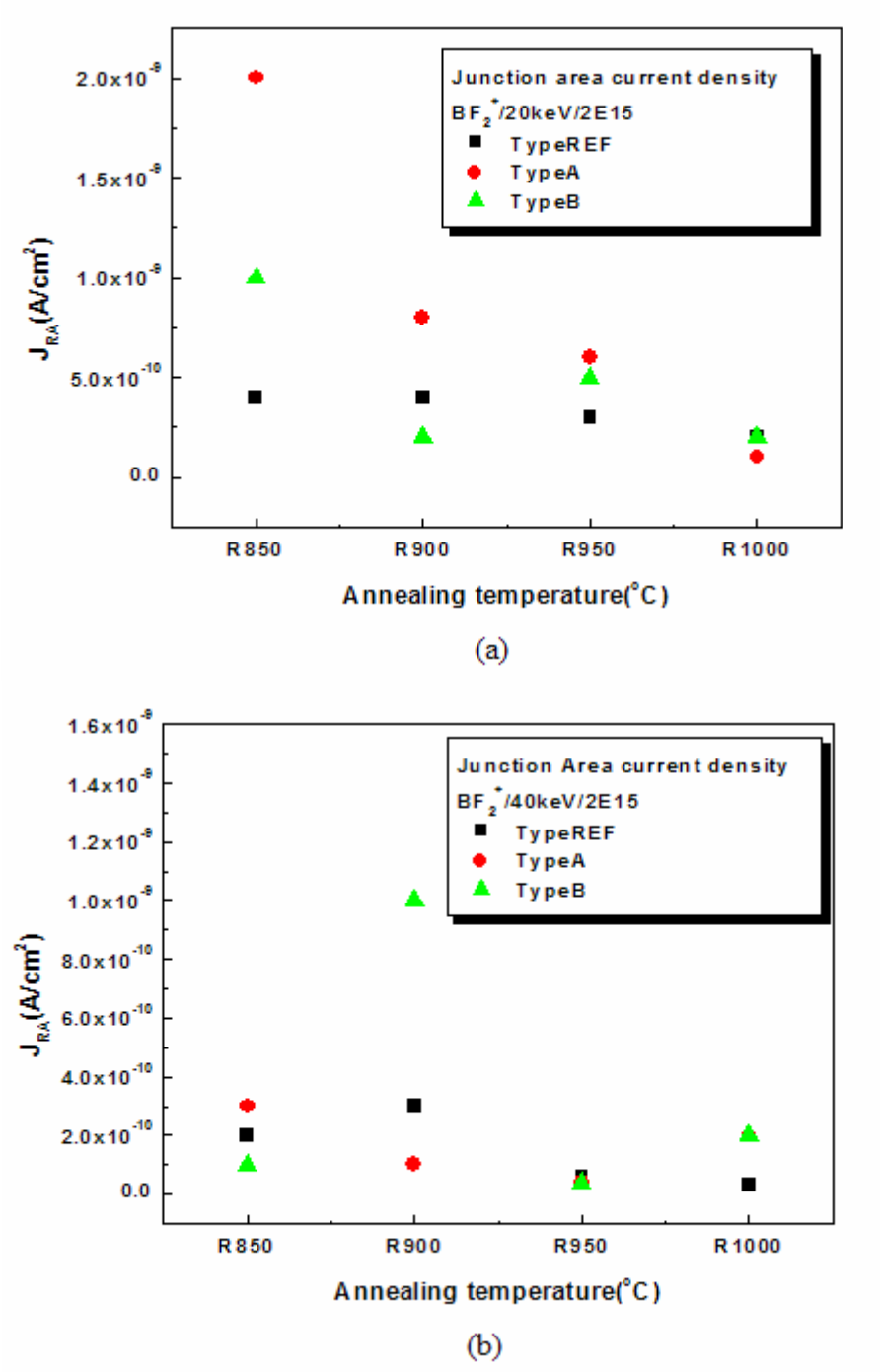


Fig.10-9. Area leakage current density (J_{RA}) versus activation temperatures with different BF_2^+ implantation energies (a) 20keV (b) 40keV

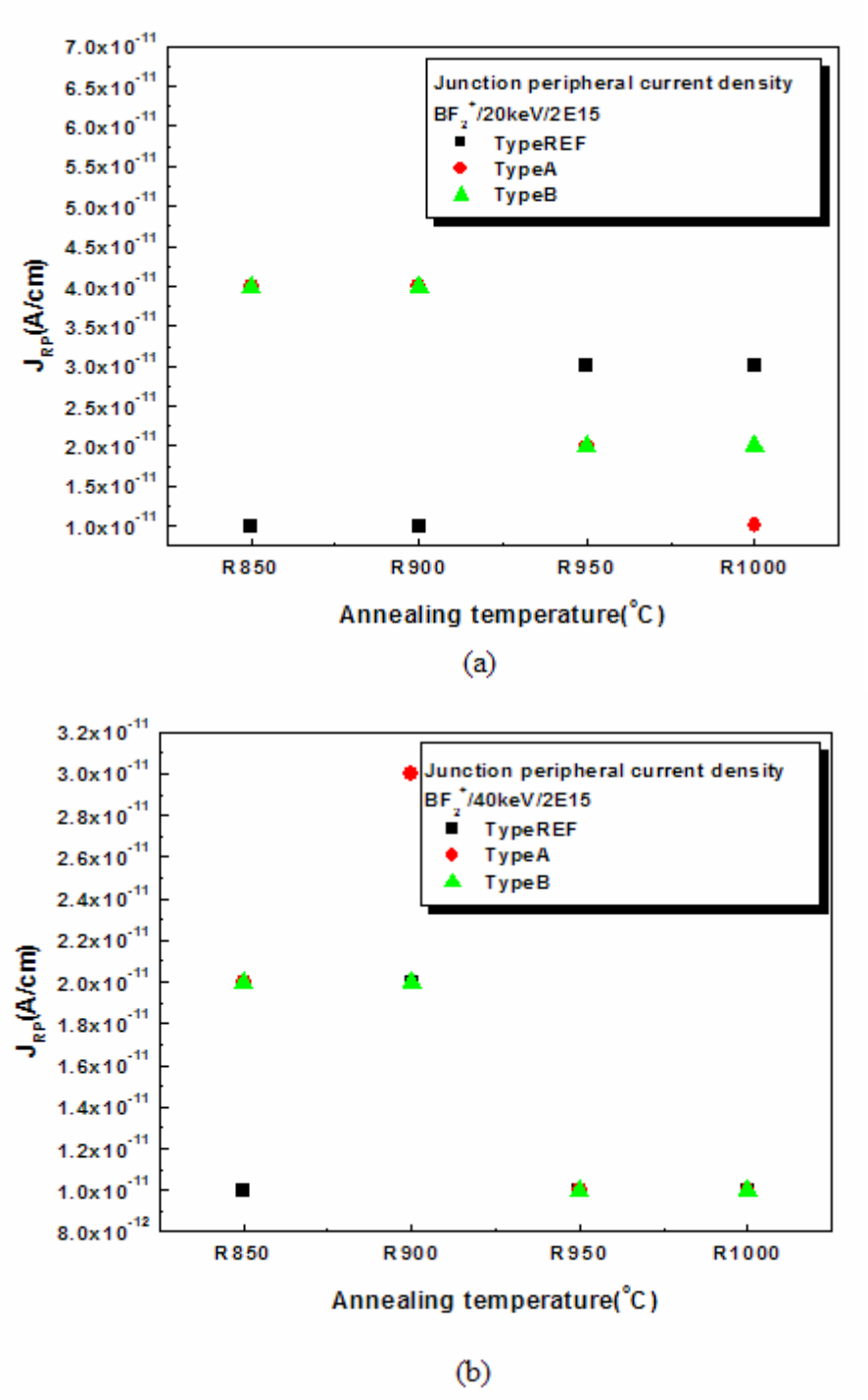


Fig.10-10. Junction peripheral leakage current density (J_{RP}) versus activation temperatures with different BF_2^+ implantation energies: (a) 20keV (b) 40keV

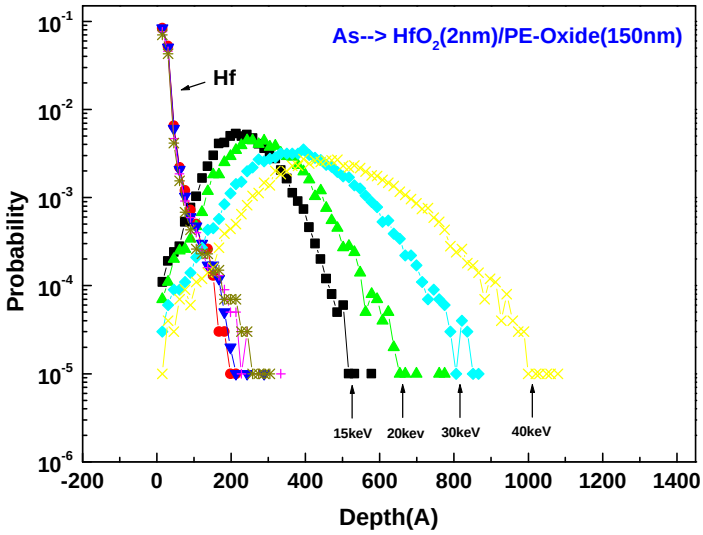


Fig.10-11. Trim simulation results of As and knocked-Hf distribution of the HfO_2/PE-TEOS structure after ion implantation.

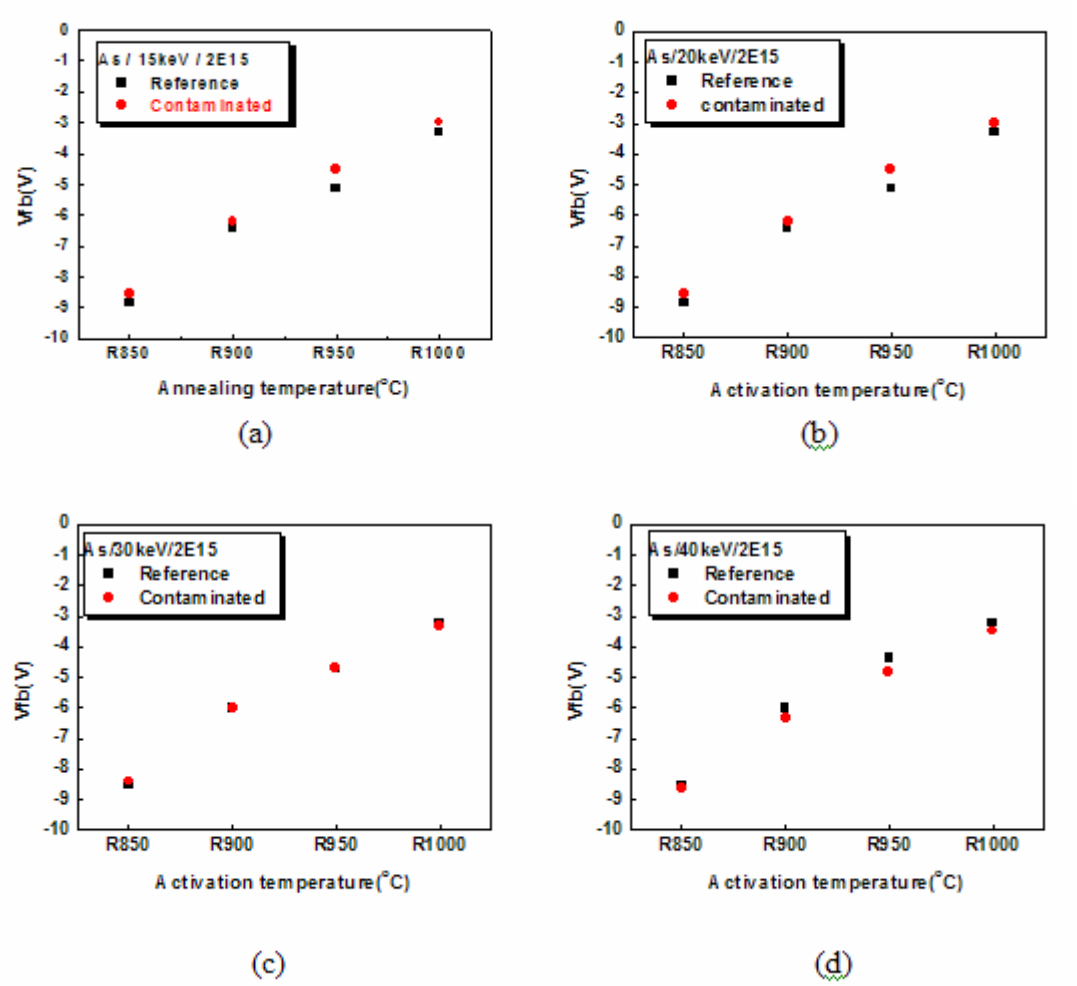


Fig.10-12. Flat-band voltage of all samples with various implantation energies and annealing temperatures. As implantation energies with (a) 15kev , (b) 20kev, (c) 30kev, and (d)40kev to a dose 2E15 cm^{-2}

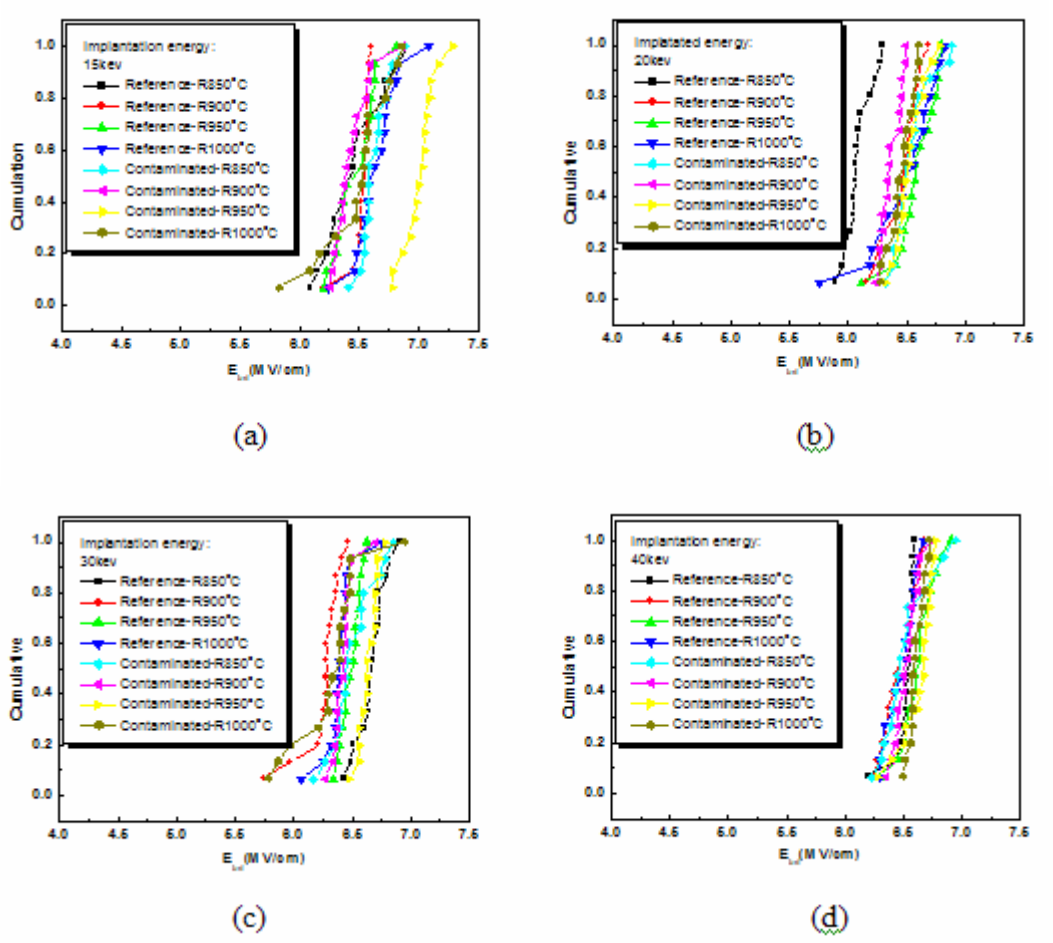


Fig.10-13. Electric field breakdown of the reference and contaminated samples with various activation temperatures at various implantation energies: (a) 15kev, (b) 20kev, (c) 30kev, and (d) 40kev

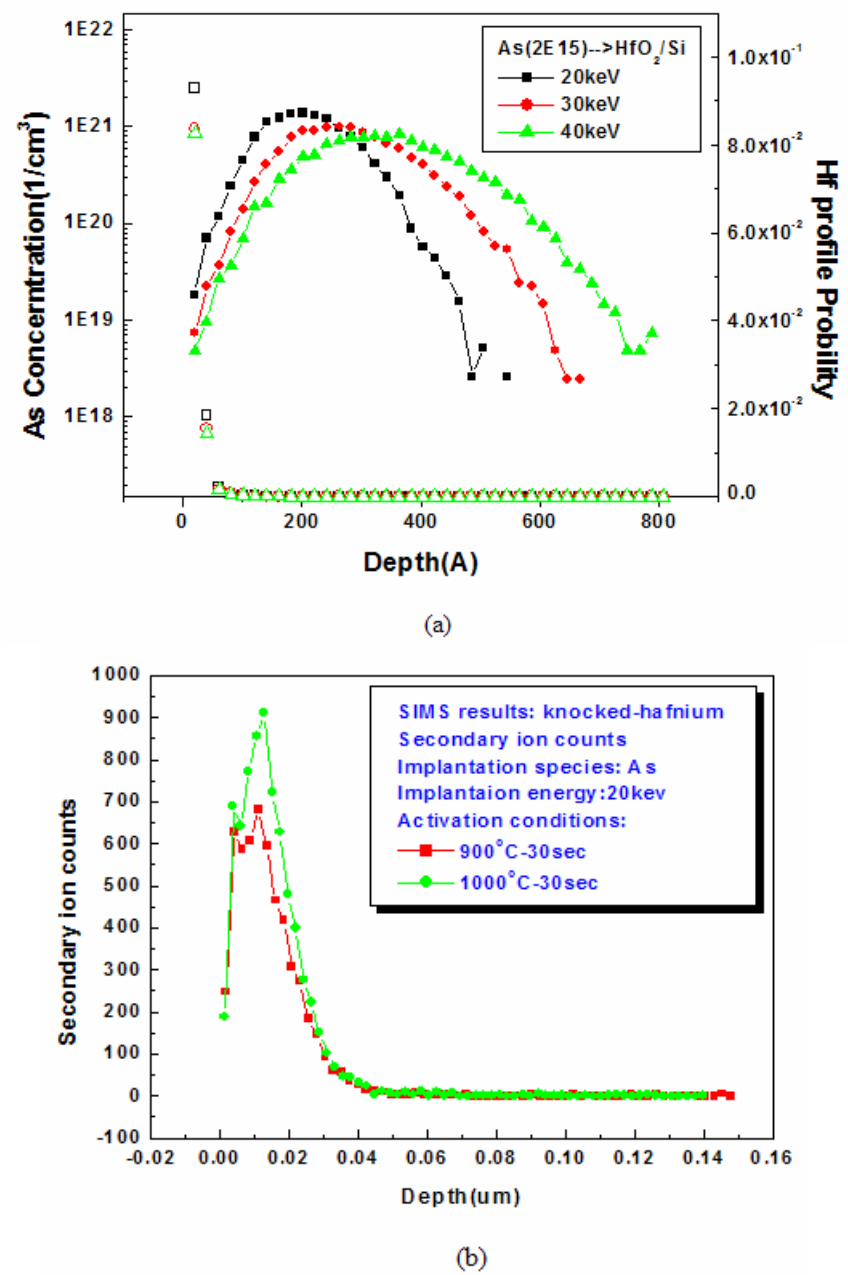


Fig.10-14. Trim and SIMS simulation results of knocked-hafnium by As Implantation. (a)Trim simulation results and (b) SIMS results.

Chapter 11
Wet Etching of HfO_2 Film

11-1 Introduction

As the thickness of conventional SiO_2-based gate dielectrics in MOS devices shrinks below ~15 nm, large leakage current and reliability concerns [1-4] dictate the search for new dielectric materials for the gate stack with dielectric constant higher than that of SiO_2 [5-9]. HfO_2 and HfO_2-based materials are currently under intense consideration because they combine good dielectric property with thermal stability suitable for conventional CMOS process flow [10-14]. Most high-k materials, including HfO_2, belong to metal oxides, and metal contamination issue must be considered. If some high-k materials are still remained on Si wafer after gate patterning, then source/drain extension implantation are followed. It is possible that the knock-on of Hf metal into the source/drain region, thus possibly resulting in p-n junction issue.

On the other hand, it has been reported that the Fringing-field Induced Barrier Lowering (FIBL) effect induces larger off-state leakage current and it is a big concern when high-k dielectrics are employed as gate dielectric. It is also reported that the structure with high-k dielectric under spacer may exhibit severer FIBL effect than the structure without high-k dielectric under spacer [15-17]. Therefore, the removal of the high-k material is necessary after gate patterning because they are very important to determine the device integration scheme. However, after gate patterning, the removal of high-k material will result in a great deal of challenges by dry or wet etching process. For dry etching, high energetic ions may damage the source/drain extension region during over-etching period, thus possibly leading to more than 1-2 nm silicon recess. Therefore, a wet chemistry to etch high-k dielectrics will be advantageous to avoid plasma damage. The as-deposited amorphous films can be etched easily in diluted HF (DHF) solution; as compared to the annealed HfO_2 films [18]. As well known, the samples with high temperature annealing are hardly etched. Fortunately, the annealed-samples subjected to energetic ion bombardment or ion implantation process can be etched easily in DHF solution (1% volume ratio). The etch rate of damaged HfO_2 is the same as the one of as-deposited HfO_2, as if the HfO_2 is again amorphized after damaging [21-22]. Therefore, it seems feasible to remove thermally treated HfO_2 material by using an ion damage/wet etch process.

Although the amorphous as-deposited HfO_2 or the damaged thermally treated HfO_2 can be etched easily in DHF solution, integration of high-k materials into a standard CMOS flow also requires new etch process with high selectivity to CVD oxide used in shallow trench isolation (STI). However, the etch rate of CVD oxide in STI structure is considerably high and leads to very low HfO_2/CVD oxide etching selectivity (HF/DI water volume ratio 1% is used in most literatures) [19-20]. For the lower HF volume ratio (1/100~1/1500), the etch rate and etching selectivity are not yet discussed in detail. In this work, experiments indicate higher etch selectivity can be achieved with HF/DI water volume ratio decreasing. An excellent chemistry adding alcohol to the HF solution has been also provided for high etching selectivity for this topic [20].

How to etch HfO_2 films effectively is studied in this chapter. The HfO_2 films were deposited in a MOCVD system at different temperatures. The films deposited at different temperatures shows different micro-structures. At higher deposition temperature, the HfO_2 film tends to be crystallized. The crystallized film is hard to be etched effectively. On the other hand, the amorphous HfO_2 film deposited at lower temperature may be easier to be etched. After post-deposition annealing (PDA), it also becomes hard to be etched effectively. The ability of the etching process is a critical issue for the application of HfO_2 film as gate insulator. Therefore, the issue of HfO_2 film etching is urgent to be solved. In this chapter, the ability of the HfO_2 etching process combining the ion-implantation step and the wet etching step is studied. It is shown that that the MOCVD HfO_2 film could be etched effectively by the proposed process.

11-2 Experimental Procedure

The starting materials are (100)-oriented silicon wafers. After RCA clean, silicon wafers were put into a MOCVD system for HfO_2 deposition. HfO_2 films were deposited by atomic vapor deposition (AVDTM) on an AIXTRON Tricent system at various substrate temperatures of 400℃, 500℃, and 550℃. Ar gas was employed as carrier gas. The reaction gas was O_2 with 300sccm and the pressure was 1.5mbar. The original thickness (T_{orig}) was set to 25 nm, which was controlled by the pulse number and measured with n&k analyzer. This system is designed for 200mm wafers. In order to handle 150mm wafer, a circular quartz holder with a 200mm outer diameter and 150mm inter diameter is used.

After HfO_2 film deposition, some wafers were implanted with arsenic (As^+) ions. Before ion implantation, trim simulation was used to simulate the doping profiles in order to

determine the experimentation conditions. The As^+ ions were implanted at 15 KeV to a dose of 5x13 cm^{-2}, 5x14 cm^{-2}, and 5x15 cm^{-2}. The heavy As^+ is energized enough to damage the crystalline film and was used to de-crystallized HfO_2 film. After implantation, the thickness was measured by n&k analyzer. Although the optical properties may change after the implant process, the thickness of the implanted sample (T_{imp}) were still measured with the same n&k parameters as given for original sample. HF/IPA (volume ratio: 5/95) solution was then used to wet etch the damaged HfO_2 film. In order to ensure HF/IPA mixed completely, this solution was shocked for 30 minutes and then was used to etch the HfO_2 samples for 2 minutes. The film thickness after the wet etch process (T_{etch}) was measured by n&k analyzer again.

HfO_2 films experienced various PDA temperatures were also studied in this thesis. The original thickness of 400℃ deposited film was set to 50nm and the HfO_2 film was deposited with reaction gas of O_2 of flow rate 500 sccm at 5mbar, while the thickness of 500℃ deposited film was set to 28nm and the film was deposited with reaction gas of O_2 of flow rate 300 sccm at 1.5mbar. After film deposition, PDA process was performed in a RTA system at temperatures of 600℃, 700℃, and 800℃ for 30sec. The thickness after PDA (T_{ann}) was then measured by n&k analyzer. The 400℃ deposited film was damaged using BF_2^+ ions at 25KeV or Ar^+ ions at 20KeV to a dose of 5x13 cm^{-2}, 5x14 cm^{-2}, and 5x15 cm^{-2}, while the 500 ℃ deposited film was damaged using BF_2^+ ions at 13KeV or Ar^+ ions at 11KeV to a dose of 5x13 cm^{-2}, 5x14 cm^{-2}, and 5x15 cm^{-2}. After measuring T_{imp}, HF/IPA (volume ratio: 5/95) solution was then used to etch the damaged HfO_2 film.

In order to further study the etch rate selectivity between implanted and non-implanted samples; samples were patterned by P.R and BF_2^+, As^+, and Ar^+ were chosen to be implantation ions. The P.R. prevents some regions from damage during implantation process. Therefore both implanted and non-implanted sampled could be carried out in the same wafer. After the implantation process as described above, P.R was removed by ACE solution. Then, these samples were also wet etched by HF/IPA (volume ratio: 5/95) solution and inspected by optical microscope.

11-3 Results and Discussions

11-3-1 Effect of Deposition Temperature

Fig.11-1 shows the film thickness after implantation process. The thickness is measured by n&k analyzer. Because the optical properties of HfO_2 film may change seriously with the

heavy implantation dose and the original characteristics of non-implanted HfO_2 films may also change after implantation process, T_{imp} is different from T_{org} and the difference depends on implantation species and dosages. The intention of the implant process is to damage HfO_2 films so that the films could be wet etched efficiently by HF/IPA solution. As shown in Fig. 11-2, the etch rates of the implanted HfO2 films deposited at 500 ℃ and 550 ℃ increases with increase of implantation dose. The etching rate of the 400 ℃ deposited sample is almost independent on implantation dose and is higher than that of all 500 and 550°C deposited samples. The main difference between the 400 ℃ deposited sample and 500 ℃ or 550°C deposited samples is the degree of crystallization, which has been reported in previous chapters. It is proposed that the Hf-O bond is etched by un-dissociated HF. The more amorphous HfO_2 film causes higher wet etch rate due to the more Hf-O dangling bonds and imperfect Hf-O bonds. For the 400℃ deposited amorphous film, there are many Hf-O bonds exists inside; therefore, the wet etch rate is high. In the 500℃and 550℃ deposited films, since there are fewer Hf-O bonds existed inside, the wet etching rate is almost zero. When heavier implant dose gets more disorder of HfO_2 film, the higher wet etching rate could be obtained. However, the higher deposition temperature produces fewer Hf-O bonds, the wet etching rate decreases under the same implant dose.

The similar result is revealed in the experiment of etching rate selectivity. It could support that the implanted samples can be more easily etched by the reaction of Hf-O dangling bonds and imperfect Hf-O bonds with HF radical. For the selectivity experiment, some regions were damaged by the implant ions and some were not. After the wet etching process, if the samples reveal very clear etching pattern, some regions are well etched, and selectivity of sample is defined as excellent. If sample reveals light pattern, the etching rate selectivity is defined as good. If sample reveals almost no pattern, two conditions are possible. One is that both of the implanted and non-implanted regions were well etched. The other one is that both were not etched. To distinguish the two conditions, the thickness of HfO_2 film is checked by n&k measurement. The results are summarized in Table 4-1. The symbols "╳","△" and "ˇ" represent poor selectivity, good selectivity, and excellent selectivity, respectively. For the amorphous structure of 400℃ deposited film, no pattern could be found after the implantation and wet etching process. It's identified that both the implanted and non-implanted regions were well etched. The pattern could be found easily in the 500℃ deposited film since the damaged region has more Hf-O dangling bonds and is easier to be wet etched by the HF/IPA solution. The 550℃ deposited samples also present excellent

selectivity, except for the condition of 5×13 cm^{-2} dose. It is presumably that the insufficient dose cannot produce sufficient damage to the high temperature deposited films to enable wet etching ability. Therefore, the dosage condition should be considered together with the deposition condition of the HfO_2 film.

11-3-2 Effect of PDA Temperature

The thickness change of HfO_2 film after PDA process is shown in Fig.11-3. The negative value shows the thinner film thickness measured after PDA process. It is believed that the loose structure deposited at lower deposition temperature is porous but the structure would become dense after PDA process. Therefore, the thickness change appears. At higher deposition temperature, the thickness of HfO_2 film before and after PDA is almost the same. This observation confirms that the structure of high temperature deposited film is tight. After PDA process, the implantation process was followed. The thickness changes of the 400℃ and 500℃ deposited films were shown in Fig.11-4 and Fig.11-5, respectively, for reference purpose.

In the wet etching rate experiment, the etching rate of the 400℃ deposited film without PDA process is very high. The wet etching rate of 400℃ deposited film is shown in Fig 11-6. As discussed above, Hf-O dangling bonds are repaired with the high temperature process. However, after the implantation process, the film structure is damaged and Hf-O dangling bonds produce. Therefore, with the higher implantation dose, more Hf-O dangling bonds induce higher wet etching rate. On the other hand, with the same implantation dose but different PDA temperature, the higher PDA temperature repairs more Hf-O dangling bonds so that the wet etching rate is lower. This condition is also presented in 500℃ deposited film and is shown in Fig.11-7.

As shown in Fig.11-4 to 11-7, BF_2^+ and Ar^+ exhibit the same effect as As^+ in the wet etching rate experiment. There are also some samples prepared for the selectivity experiment. Table 4-2 shows the outcome of this experiment. The poor selectivity was obtained in 400℃ deposited film due to many Hf-O dangling bonds existed inside the non-implanted region. But in the 500℃ deposited film, less Hf-O bonds exist inside soothe film is quite hard to be wet etched if the implantation process does not proceed.

11-4 Summary and Future Work

Temperature, including deposition temperature and post-deposition annealing temperature, is the most important factor to affect the wet etching behavior of HfO_2 film. The film structure deposited at different temperatures is studied in this chapter and the influence of PDA temperature is also examined. The higher deposition temperature causes fewer dangling Hf-O bonds and higher post-deposition annealing temperature reconstructs the dangling and imperfect Hf-O bonds. Therefore, the wet rate is lower. Fortunately, implantation process can help to degrade Hf-O bonds, and let the HfO_2 films become wet etch-able.

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Table 11-1. The selectivity experiments of different deposited temperature films. The sign " ╳" represents the poor selectivity；the sign " △" represents the good selectivity；the sign " ˇ" represents the excellent selectivity

	5x13 cm^{-2}	5x14 cm^{-2}	5x15 cm^{-2}
400℃ film	╳	╳	╳
500℃ film	ˇ	ˇ	ˇ
550℃ film	△	ˇ	ˇ

Table 11-2. The selectivity experiments of different deposited temperature films. The sign " ╳" represents the poor selectivity；the sign " △" represents the good selectivity；the sign " ˇ" represents the excellent selectivity

		5x13 cm^{-2}	5x14 cm^{-2}	5x15 cm^{-2}
$BF2^{+}$	400℃	╳	╳	╳
	500℃	△	△	ˇ
Ar^{+}	400℃	╳	╳	△
	500℃	△	ˇ	ˇ

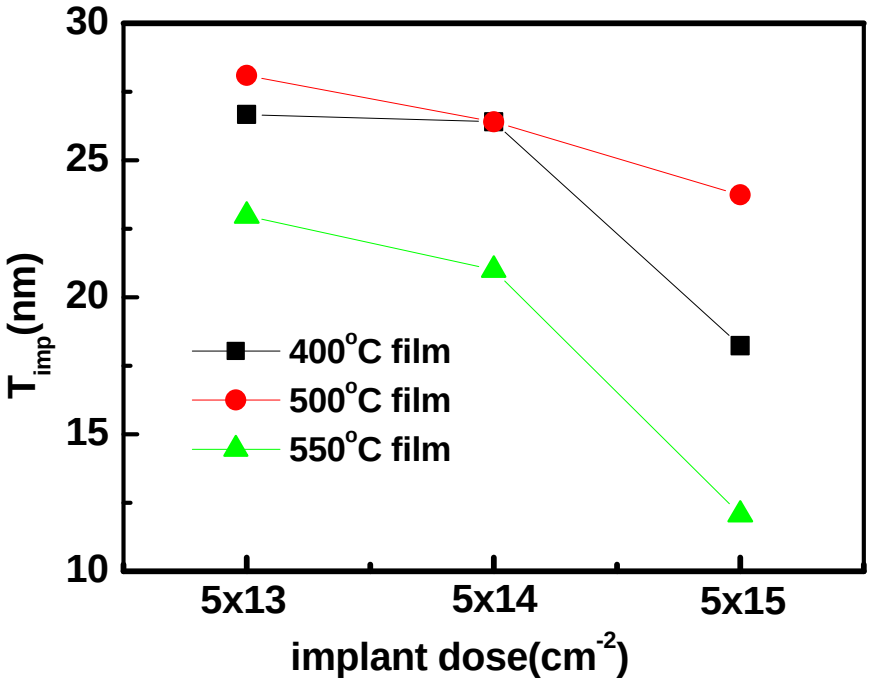


Fig.11-1. The film thickness with different deposition temperature and different implant dose.

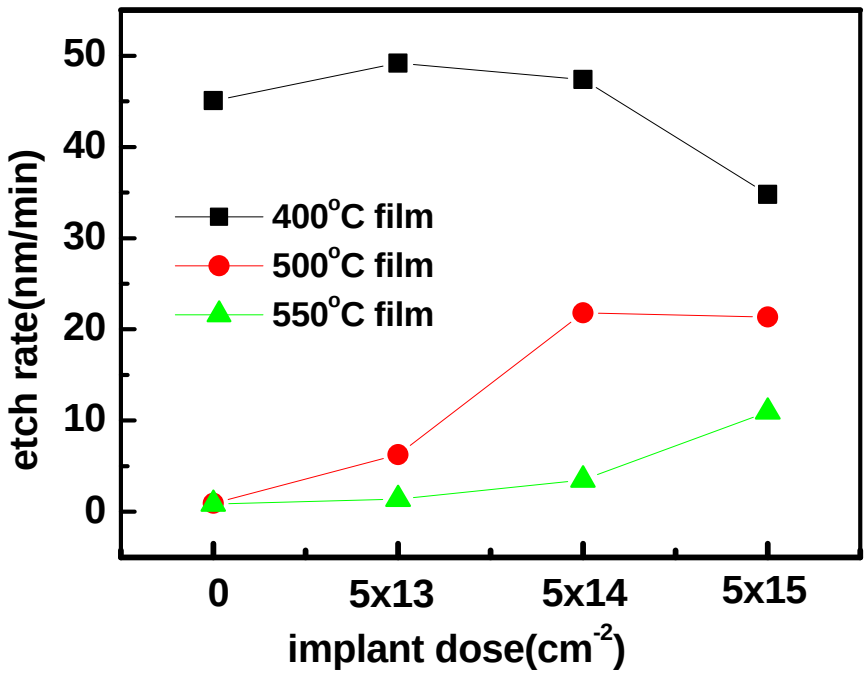


Fig.11-2. The etch rate of HfO_2 film of different deposition temperature and implantation condition.

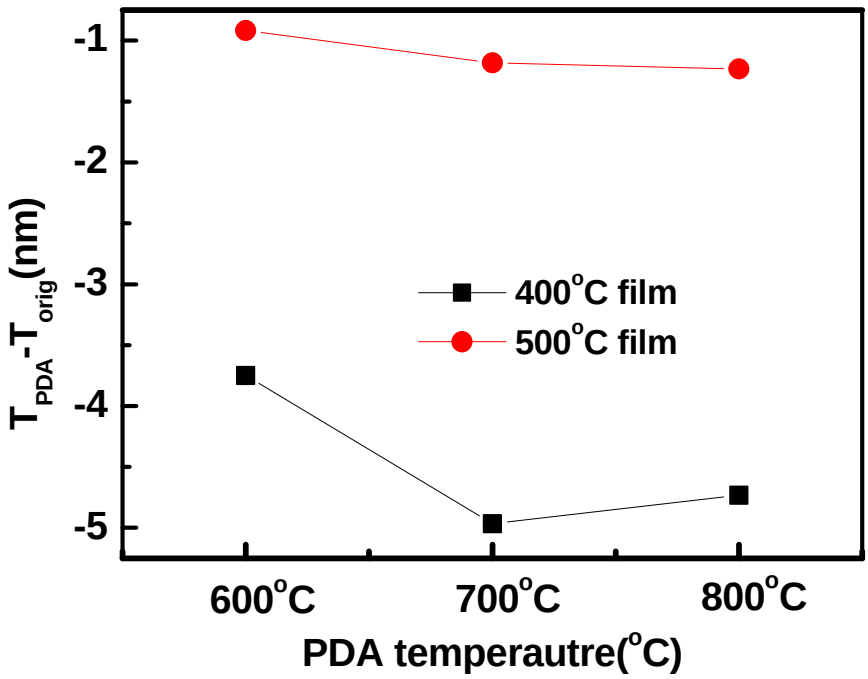
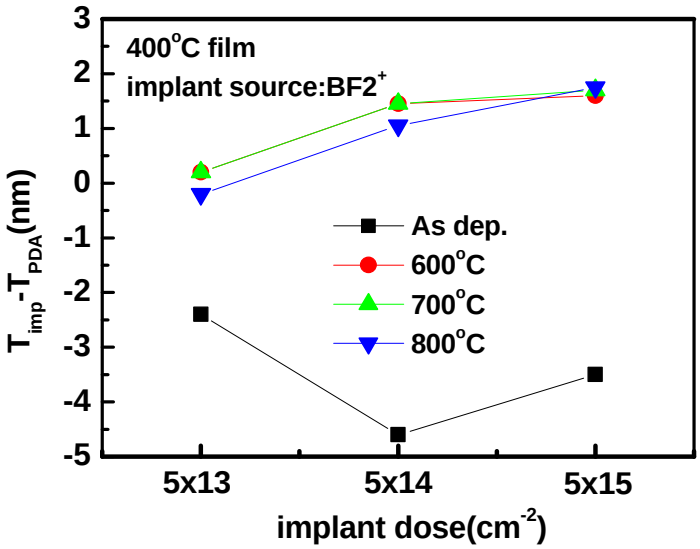
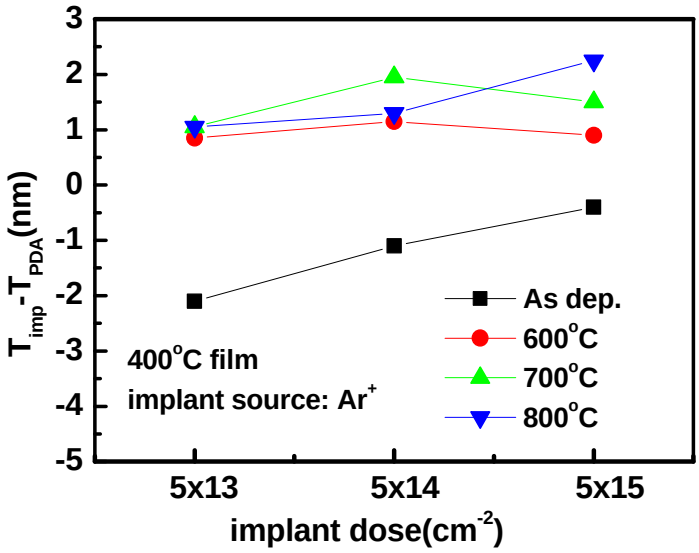


Fig.11-3. Thickness change of HfO_2 film after PDA process.

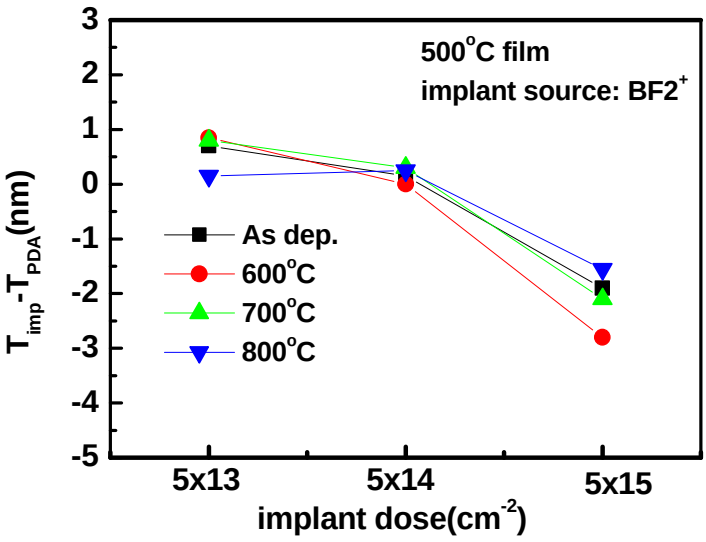


(a)

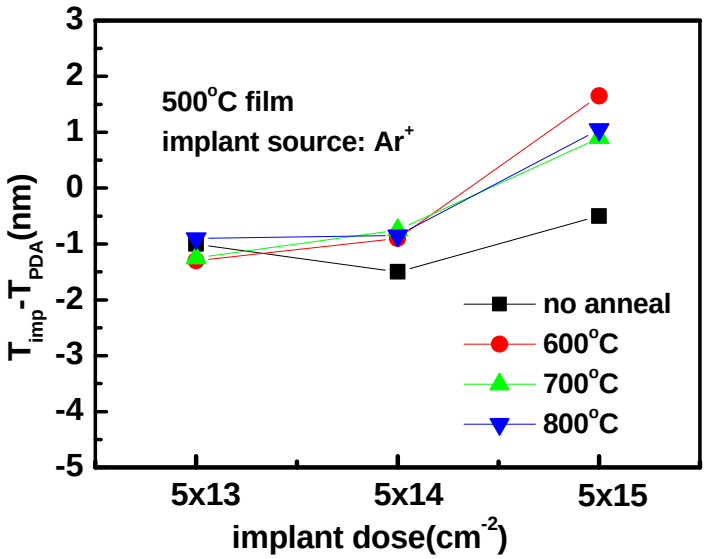


(b)

Fig.11-4. Thickness change of 400℃ film. The implant source is $BF2^+$ in Fig. 11-4(a) and the implant source is Ar^+ in Fig. 11-4(b)

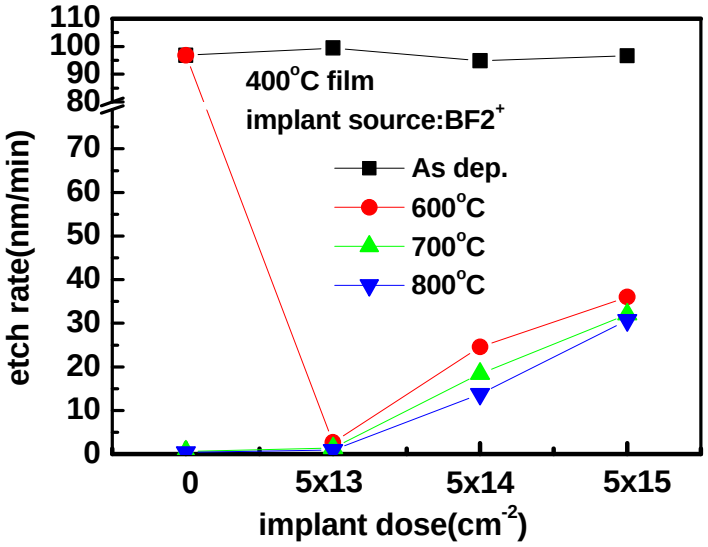


(a)

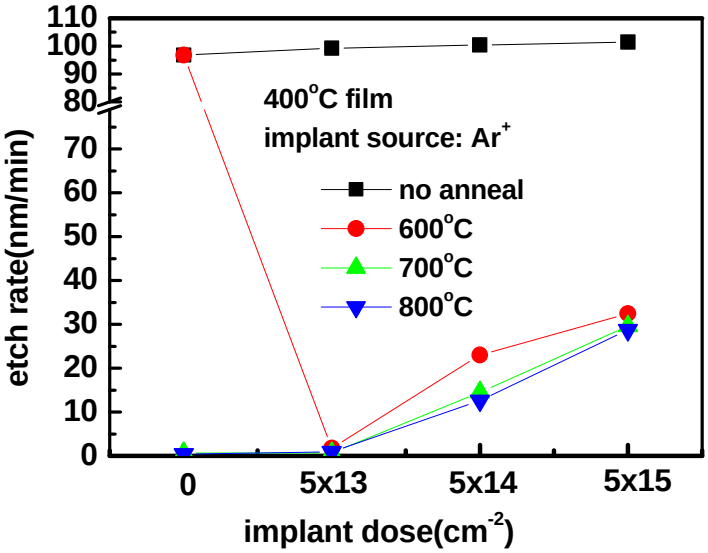


(b)

Fig.11-5. Thickness change of 500℃ film. The implant source is $BF2^+$ in Fig. 11-5(a) and the implant source is Ar^+ in Fig. 11-5(b).

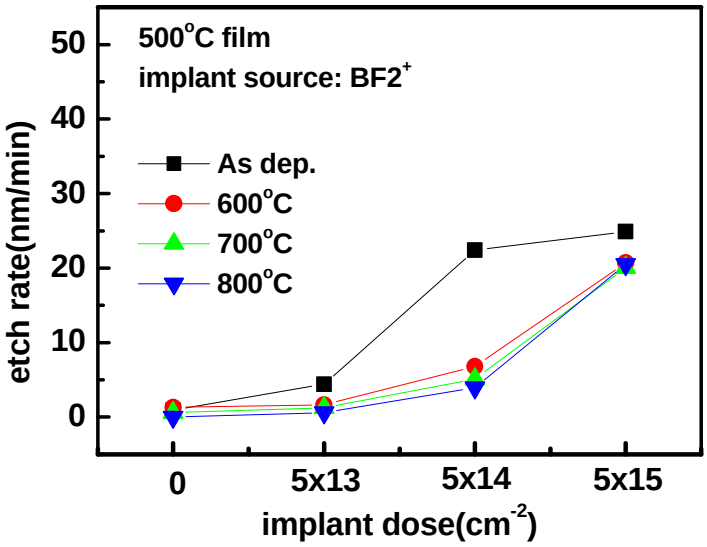


(a)

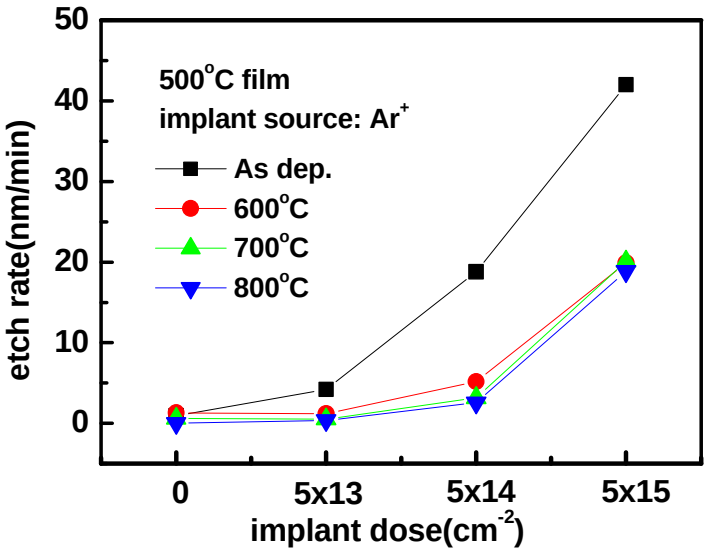


(b)

Fig.11-6. The wet etch rate of 400℃ film. The implant source is $BF2^+$ in Fig. 11-6(a) and the implant source is Ar^+ in Fig. 11-6(b)



(a)



(b)

Fig.11-7. The wet etch rate of 500℃ film. The implant source is $BF2^+$ in Fig. 11-7(a) and the implant source is Ar^+ in Fig. 11-7(b).

Chapter 12
Summary and Conclusions

12-1 Summary

Several important results have been obtained during the execution of this project.

At first, this work explores the characteristics of the binary alloys Ta-Pt and Ta-Ti for gate electrode application. With a proper composition of high and low work function metals, the work function of the metal alloys can be modulated from 4.16eV to 5.05eV continuously. The resistivity of Pt-Ta alloy is high and thermal stress of thick Ta-Pt alloy may generate oxide charges. Therefore, stack structure with a low resistivity and low stress layer as main conducting layer and the proposed alloy layer as work function control layer, for example W/Ta-Pt, is preferred for actual application.

The Ta-Pt alloy with tunable work function is a potentially suitable material for metal gates due to its thermal stability and resistance to the impurities. It could be integrated in the conventional MOSFET process, and the work function does not change by the incorporation of the implantation impurities of arsenic ions, boron ions and phosphorus ions. Therefore, the control of threshold voltage of the alloy-gate MOSFET could be easier, and not be disturbed by the S/D implantation process.

The modulation range of work function can be up to 0.4V from pure Mo to MoN of N/Mo ratio 1.57 and this would be useful for threshold voltage adjustment. In aspect of process temperature, the nitrogen can’t be too much and saturates in order to avoid the affect of thermal stability. The over high sheet resistance seems to be the common problem of nitride and this could be the limiting condition for metal nitride to be the candidate of metal gate. This situation of high resistivity could be solved by stack another layer of low resistance metal upon metal nitride to reduce the sheet resistance. Besides, Fermi level pinning effect was found for the metal gate on HfO_2 dielectric and moved the Fermi level toward the mid-gap of Si. Then Fermi level would be pinned there. This effect caused that the needed value of work function would be larger than theoretical value. But from our work, difference of work functions between MoN-0 and MoN-3 on SiO_2 and HfO_2 doesn’t get affected by oxide layer. So Fermi level pinning effect seems not happen.

The range of work function modulation can be 0.4V~0.5V from pure tungsten metal to

WN_x with the N/W ratio of 1.57. This modulation range has finite effect for the adjustment of threshold voltage. For the process temperature, the content of nitrogen atoms can't be over saturate too much. Otherwise, the thermal stability would be affected. Over high sheet resistance seems to be the common problem of nitride which to be the candidate of metal gate, and this could be solved by stack a layer of low resistance metal upon nitride. Besides, the work function of WN_x on HfO_2 is only 0.1V higher than that on SiO_2. This effect confirmed that Fermi pinning effect occurred. It's a problem worthy to notice and make further research for it.

Using physical vapor deposition technique, it is difficult to totally eliminate the formation of interfacial SiO_2 layer. During reactive sputtering deposition of HfO_2 layer, an interfacial SiO_2 layer thicker than 3 nm would be grown. Such an unusual thick SiO_2 layer is formed due to the enhanced oxidation of O-radicals generated in the sputtering chamber. Adoption of two-step deposition method, the thickness of interfacial SiO_2 layer can be reduced only if the bottom Hf layer is thicker than 5 nm. However, the reduction of effective oxide thickness would be limited. Re-oxidation of Hf film sounds a better choice. A 1.0-1.5 nm thick interfacial SiO_2 layer is still observed. This implies that the traced oxygen in the sputtering chamber plays critical role on the formation of interfacial layer. To conclude, reactive sputtering is not a good method to prepare HfO_2 layer with negligible interfacial SiO_2 layer. Re-oxidation of Hf film is a better choice, but the oxygen content in the sputtering chamber must be well controlled.

The gas injection sequence of MOCVD system affects the formation of interfacial layer at HfO_2/Si interface. In comparison with the Hf-first scheme, the O_2-first scheme results in thicker CET, which accounts for thicker interfacial layer. However, this scheme is still recommended due to the much lower leakage current. To reduce CET to meet the requirement of sub-65nm devices, suitable surface treatment and post deposition processes must be developed. Surface treatment affects the growth of interfacial layer and thus affects the electrical properties. The magnitude of leakage current is in the sequence of RTO-treatment < NH3-treatment < HF-treatment. NH3-treatment results in the thinnest CET among the three surface treatment methods. However, the hysteresis phenomenon of NH3-treatment sample is severer than that of the RTO-treatment samples apparently. Post surface treatment annealing in N_2O ambient or post deposition annealing in N_2 or O_2 ambient can improve the hysteresis problem but the cost is the increase of CET. Within the experimental conditions in this chapter, it is suggest that in terms of the best interface properties and the lowest leakage current density, RTO-treatment is the best choice. However, to achieve the thinnest CET,

NH_3-treatment becomes the most promising method. Higher deposition temperature and purer O_2 ambient is benefit to the leakage current performance under the same CET. By adding N_2O gas, the deposition rate is reduced and the leakage current is increased. As the deposition temperature increases to 500℃, the surface treatment and post deposition annealing temperature play minor role on the leakage current. Higher O_2 flow rate supply more sufficient O2 in reaction chamber is also important deposit high quality HfO_2. According to the above results, the best deposition conditions are recommended as : surface treatment : NH_3-treatment, deposition temperature:500℃, deposition ambient:pure O_2 ambient, O_2 flow rate:500sccm, bas pressure:5mbar.

For the film deposited at low temperature or with insufficient O_2 supply, not decomposed Hf-precursor incorporates into HfO_2 film results in HfO_2 layer increase during PDA. The interfacial layer increases with the increase of PDA temperature. However, its thickness at medium PDA temperature does not increase apparently. Therefore, the leakage current is not dominated by the interfacial layer. After 1000℃ PDA, the interfacial layer increases to around 3 nm so that the current transport is blocked effectively. The interfacial layer is identified as silicate-like material. It must be pointed out that the surface treatment methods employed in this thesis are not efficient enough to suppress the growth of interfacial layer. To further scales down the CET into sub-1nm regime, advanced surface treatment method must be developed.

The most stable state of HfO_2 is crystalline state so that the HfO_2 films tend to crystallize during PDA. Nano-crystals are observed in films deposited at any conditions. For HfO_2 films deposited at low temperature or with insufficient O_2 supply, the nano-crystals are separated by amorphous region and show round shape. It is postulated that the boundary of these nano-crystals contains high concentration impurities especially nitrogen. The HfN-like boundary layer accounts for the leakage current of these samples. Hf-precursor decomposes completely during high temperature deposition, and therefore, with sufficient O_2 supply, the film becomes polycrystalline completely. The lack of high impurity boundary layer results in very low leakage current.

Although the FIBL effect becomes more pronounced as gate length becomes shorter, the I_{off} degradation due to FIBL from drain side will be partly compensated by the FIBS from source side if the spacer length scales down with the gate length. The key factor to affect the FIBL effect is the gate to drain overlap length. Most of the fringing field originating from this region. Since the overlap length must be reduced to control short channel effect, it is expected that the FIBL effect can be further relaxed. Because the overlap length plays important role,

high-*k* material existing under spacer does not affect FIBL apparently if K-value does not exceed 50. This result implies that the most promising high-*k* candidate – HfO_2 can be removed after spacer formation. The device integration can be easier. It is known that stack gate dielectric scheme with a buffer SiO_2 layer between high-*k* dielectric and Si substrate can relax the FIBL effect. This work reveals that a medium K-value buffer layer, for example Hf-silicate, still has the same influence. Conductive spacer is another effective method to reduce FIBL effect but the process is more complicate.

Fully depleted SOI device shows better resistance to FIBL induced I_{off} degradation due to the better control ability of gate electrode on channel surface potential. Simple fully-depleted SOI device can reduce the I_{off} degradation factor to two at L_g=25nm and *k*=100 using stack gate dielectric scheme. It is expected that the ultra-thin body SOI, double gate SOI, and FinFET will exhibit even stronger FIBL effect resistance. Therefore, it is concluded that although FIBL effect can not be eliminated, its impact on device performance is diminished at sub-45nm technology node and beyond under suitable device structure.

Although hafnium is knocked-into silicon and PE-TEOS oxide, it only locates at the very shallow surface of substrate due to its heavy weight. Both forward ideality factor and reverse leakage current of p^+n junction show that the existence of HfO_2 during BF_2^+ ion implantation does not affect the junction characteristics. Fig.10-14 shows the simulated Hf distribution in Si after As^+ implantation and SIMS measured Hf distribution after annealing. The shallow distribution and negligible thermal diffusion predict that the n^+p junction characteristics will not be affected by the existence of HfO_2 layer although we have no electrical data at this moment. The n^+p junction is still under processing. Measurement on MOS-C structure also shows that the existence of HfO_2 on field oxide does not produce mobile ion and oxide defects. The diffusivity of hafnium is very low in both silicon and silicon dioxide so that we could not observe the effect of hafnium in this experimental structure. All of these results imply that from the contamination point of view, the HfO_2 out of gate electrode have not to be removed immediately after gate patterning. This conclusion greatly relaxes the constraint on device process integration.

Experiment indicates that there is more obviously etching selectivity improvement for IPA/HF solution (~80) as compared to DIW/HF solution (~17). Temperature, including deposition temperature and post-deposition annealing temperature, is the most important factor to affect the wet etching behavior of HfO_2 film. The film structure deposited at different temperatures is studied in this chapter and the influence of PDA temperature is also examined. The higher deposition temperature causes fewer dangling Hf-O bonds and higher

post-deposition annealing temperature reconstructs the dangling and imperfect Hf-O bonds. Therefore, the wet rate is lower. Fortunately, implantation process can help to degrade Hf-O bonds, and let the HfO_2 films become wet etch-able.

12-2 Self-Evaluation

In the past three years, two Ph.D students, four graduate students, and 4 under-graduate students involved this project. All of them experienced complete training on the topic of metal gate and high-k dielectric technologies. Among them, three of the four graduate students received their MS degree. Two of them are working toward Ph.D degree now. Parts of the results of this project have been published as three SCI journal papers and 6 conference papers. Another three SCI journal papers are under reviewing procedure. We also applied 9 patents. Two of them have been approved and the other seven are pending. According to these achievements, we conclude that this project is successfully.

Appendix

Published Journal Papers

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[3]. Hsiu-Wei Chang, Bing-Yue Tsui, and Chao-Hsin Chien, "A Study on the Formation of Interfacial Layer during Reactive Sputtering of Hafnium Oxide", in Proc. of the 10th Symposium on Nano Device Technology, pp.32-35, 2003.

[4]. Chih-Feng Huang and Bing-Yue Tsui, "Investigation of Thermal Reliability of Ta-Pt Alloy Metal Gate for Nano- MOSFET Devices", in Proc. of the 11th Symposium on Nano Device Technology, pp.368-371, 2004.

[5]. Li-Feng Chin and Bing-Yue Tsui, "Fringing-Induced Barrier Lowering (FIBL) of sub-30 nm MOSFET", in Proc. of the 11th Symposium on Nano Device Technology, pp.465-468, 2004.

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[2]. **崔秉鉞、黃誌鋒，「金氧半場效電晶體之閘極結構」，中華民國專利**, No. 189815, 2003/11/01 - 2022/09/23, Nov. 2003。

Pending Patents

[1]. **崔秉鉞、黃誌鋒**, **「可降低源極蕭基位障載子注入阻抗的金氧半場效電晶體之結構及其方法」**, **中華民國專利申請中。**

[2]. **謝育和、王志成、蕭世乙、崔秉鉞、康宗貴、黃誌鋒、梁建翔、陶宏遠、彭寶慶、蔡明桓，" 高介電質薄膜之低溫濕蝕刻方法**" , **中華民國專利申請中。**

[3]. Bing-Yue Tsui and Chih-Feng Huang, "Structure of Metal Oxide Semiconductor Field Effect Transistor", U. S. patent pending.

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