行政院國家科學委員會專題研究計畫　成果報告

高效能動態起始電壓絕緣層上矽元件

計畫類別：個別型計畫
計畫編號：NSC92-2215-E-009-070-
執行期間：92 年 08 月 01 日至 93 年 09 月 30 日
執行單位：國立交通大學電子物理學系

計畫主持人：趙天生

計畫參與人員：李耀仁

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行政院國家科學委員會補助專題研究計畫成果報告

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計畫主持人：趙天生
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執行單位：交通大學 電子物理系

中　華　民　國　　93 年　7　月　27 日

高效能動態起始電壓絕緣層上矽元件

High Performance Dynamic Threshold SOI-MOSFETs

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計畫編號：NSC92-2215-E-009-070
執行期間：92 年 8 月 1 日 至 93 年 7 月 29 日
主持人：趙天生 交通大學電子物理系教授

中文摘要

本研究中，吾人要比較在絕緣層上矽製作的 P 型金氧半電晶體，其在 T 型和 H 型結構下，在不同溫度的操作，其熱載子效應對 DT 和傳統的操作有何不同。操作在 DT 模式下的電晶體，其臨界電壓的改變會被壓下來。然而在室溫時，最大的互導和驅動電流卻發現有更惡化的現象，特別是 T 型的電晶體。此種現象可以歸因於電晶體的放大效應和電位的不均勻現象。但是若操作再高溫的時候，因為離子撞擊率的下降，所以可以改善。

Abstract

In this study, we compared the hot carrier effects of T-gate and H-gate SOI pMOSFETs operating under dynamic threshold mode (DT-mode) and normal mode at various temperatures. By operating under DT-mode, the threshold voltage shift is reduced. However, enhanced degradations in maximum transconductance and drive current are observed when operating under DT-mode at room temperature, especially for the T-gate structure. The transconductance enlargement effect for devices operating under DT-mode, together with the non-uniform potential distribution in T-gate structure, are believed to be responsible for the observed enhanced degradations. At elevated temperatures, the hot-carrier-induced degradations are alleviated for devices operating under DT-mode, to levels close to those of the normal mode, due to reduced impact ionization at higher temperature.

Introduction

DTMOS proposed by Assaderaghi et al. [1] was for lower power supply voltage applications. The threshold voltage operating under DT mode is reduced due to the forward biasing of the body, so the current drive can be drastically improved under the on state. Since the device exhibits the same normal-mode V_{TH} in the off state (because V_G=V_{BS}=0), low standby power consumption is maintained. Furthermore, ideal subthreshold slope behavior, and improved short channel effects due to the dynamics substrate bias were also the promising factors for DTMOSFETs. The fabrication of DT-MOSFETs on partially depleted silicon-on-insulator (PD-SOI) MOSFETs is quite attractive for lowering the junction leakage current. In this study, we report the threshold voltage reduction and hot carrier degradation on SOI pMOSFETs at different temperature operating under conventional normal mode and DT mode. Finally, we will propose possible physical mechanisms to explain the results.

Device Fabrication

P-channel MOSFETs were fabricated on 6-in p-type SOI wafers with resistivity of 15-20 Ω-cm, and a top silicon device layer thickness of 200nm. Local oxidation of silicon (LOCOS) was used for device isolation, with the top silicon layer fully oxidized (i.e., the active device layer not covered by

the masking nitride was fully converted into oxide). As^+ implant with an energy of 100 keV and a dose of 1×10^{13} cm^{-2} was performed through a 30nm sacrificial oxide for threshold voltage (V_{TH}) adjustment. After stripping the sacrificial oxide, a final 3.4nm gate oxide was grown in N_2O ambient, followed by a 200nm poly-Si gate deposition. The poly-Si layer was then patterned and etched to define transistor gate length varying from 10.62 μm to 0.8 μm, with a channel width of 100 μm. Shallow S/D extensions were formed by BF_2 implant (10keV, $1\times10^{15}cm^{-2}$). After the formation of TEOS sidewall spacer (200nm), deep heavily-doped source/drain junctions were formed by BF_2 implantation. Afterwards, wafers were annealed by rapid thermal process (RTP) at 1020°C for 20sec. A 550nm TEOS oxide layer was then deposited and etched to form contact holes. Finally, a Ti/TiN/Al-Si-Cu/TiN 4-layer metal was deposited and patterned to complete contact metallization. Electrical characterizations were performed using an HP4156 system. Hot carrier stressing tests were performed using a temperature-regulated hot chuck at temperature ranging from room temperature to 100 ℃.

Results and Discussion

Figure 1a shows the electrical connection under DTMOS operation. Fig. 1b, 1c depict the device layout for H-gate and T-gate structures. Fig. 2 shows V_{TH} degradations for SOI pMOSFETs with different temperature and operating under different modes for H-gate structures. All devices were stressed at $V_G=V_{TH}$, and V_D=-4.5V[2]. It can be seen that the device at room temperature depicts the worst ΔV_{TH} among all splits. Electron trapping appears to be the dominant degradation mechanism at the initial stage of stressing (i.e., before 10^3 seconds) for splits. In contrast, since the observed ΔV_{TH} is negative for all devices above 10^3 sec., this phenomenon indicated positive charges buildup in the gate dielectric layer. The magnitude of ΔV_{TH} for H-gate in DT-mode is smaller (within 4mV), which was almost independent of temperature. However, that under normal was inverse proportional to temperature effects, higher temperature leads lower threshold voltage variation. Fig. 3 shows the comparison of time dependence of G_{mmax} degradation for H-gate. The split at room temperature under DT mode actually depict aggravated linear G_{mmax} degradations. Fig.4 shows G_m between SOI pMOSFETs for different substrate bias and SOI DT-pMOSFETs for H-gate devices. In addition to the decreasing effective electrical filed, G_m operating under DT-mode was enlarged due to the dynamic threshold voltage, about 60% in Fig. 4. During hot-carrier stressing, the carrier mobility μ_p decreases, and the magnitude of G_m degradation was enhanced due to the dynamic threshold voltage. However, the degradation magnitude of all splits under DT mode at high temperature bias stressing (75 ℃ and 100℃) shows alleviating behavior due to maximum lateral electrical field E_m was decreasing at elevated temperature[3]. The effects of temperature on the reduction ratio of threshold voltage under both DT and normal modes are shown in Fig. 5. The reduction ratio of threshold voltage under DT mode was larger than that under normal mode, which could result in larger drain current and smaller transconductance reduction. Therefore, the decrease of threshold voltage with increasing temperature would result in raise of the saturation drain voltage, and then decrease the lateral electrical field E_m. The smaller lateral electrical field E_m resulted in reduction of impact ionization and then decreased the magnitude of ΔV_{TH} and transconductance at elevated temperature. Similar results were also depicted in Fig.6 about the degradation of driving current of SOI pMOSFETs and DT SOI-pMOSFETs for different

temperature ($V_D=V_G$=-0.7V). Fig. 7 shows the comparison of time dependence of G_{mmax} degradation for SOI pMOSFETs for T-gate. The degradation of transconductance under DT mode at room temperature still shows the worse behavior, and improves at elevated temperature due to decreasing lateral electrical field E_m. Furthermore, for devices operating under DT-mode, the T-gate structure depicts larger degradations than the H-gate structure. Fig. 8 depicts the degradation of driving current operating on SOI pMOSFETs and DT SOI-pMOSFETs at different temperature ($V_D=V_G$=-0.7V) for T gate structure.

References

[1]F. Assaderaghi et al., IEEE Electron Dev. Lett., 13, p.510, 1994.
[2]Ru Huang et al., IEEE Trans. Electron Dev, 48, p.1594, 2001.
[3] J.K Lee et al., IEEE Electron Device Lett., 23, p.673, 2002.

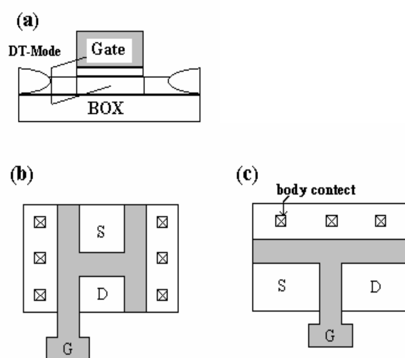


Fig.1 (a) Connections of SOI MOSFETs under T mode (b) T-gate structure (c) H-gate structure

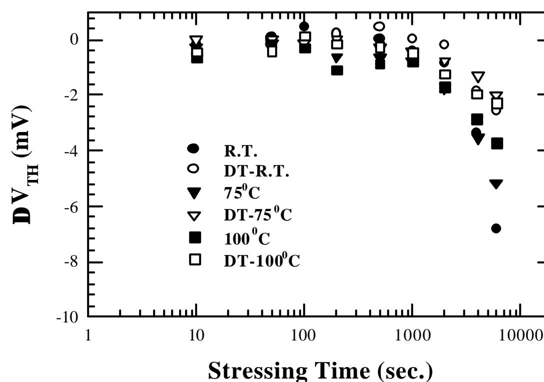


Fig. 2 Stress time dependence of V_{TH} degradation between SOI pMOSFETs and SOI DT-pMOSFETs with different temperatures and operating under different modes for H-gate devices

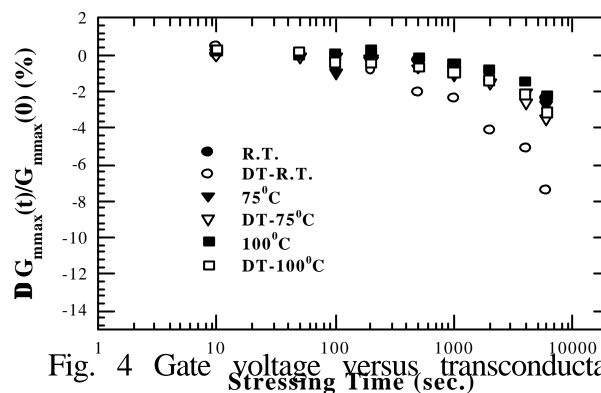
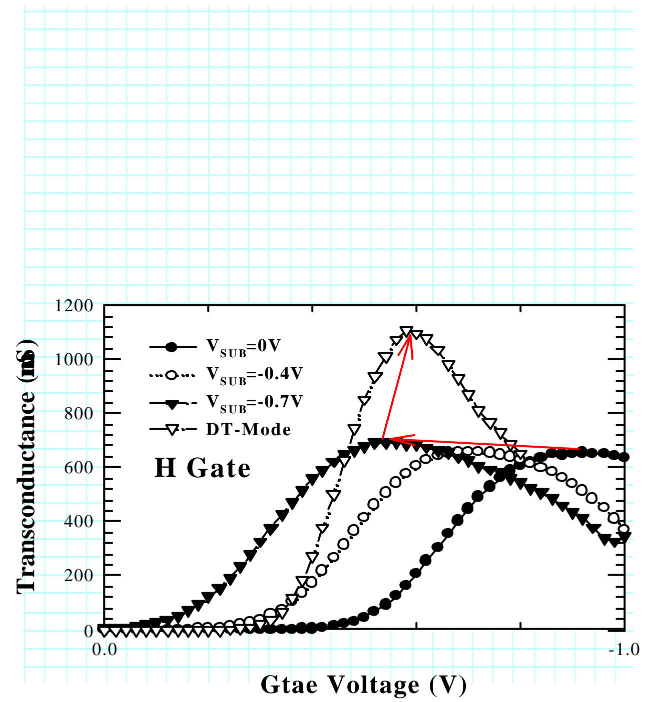


Fig. 3 Linear transconductance (V_D=-0.1V) for 0.8μm H-gate device versus Gate voltage for

Fig. 4 Gate voltage versus transconductance between SOI pMOSFETs for different substrate

Fig. 3 Linear transconductance (V_D=-0.1V) for 0.8μm H-gate device versus. Gate voltage for different stressing time, which devices were stressed at $V_G=V_{TH}$, and V_D=-4.5V.



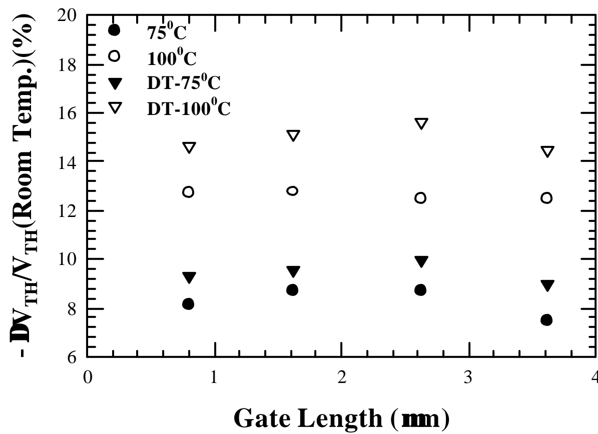
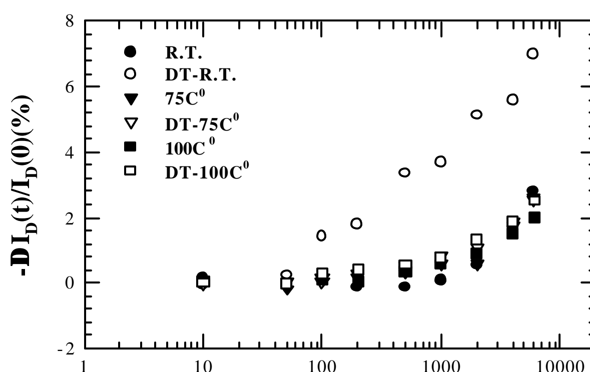
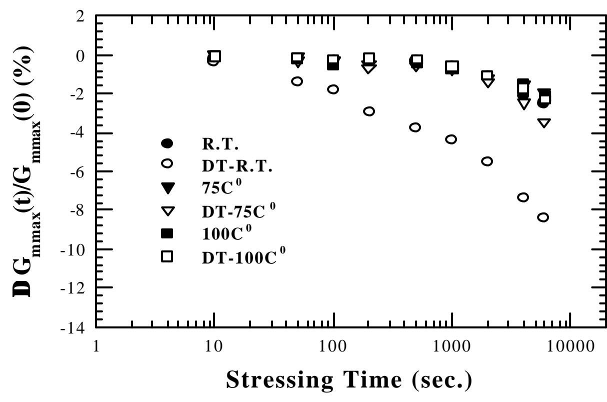


Fig.5 Ratio of threshold voltage reduction of H-gate structure devices versus gate length under both normal and DT modes for different temperature.

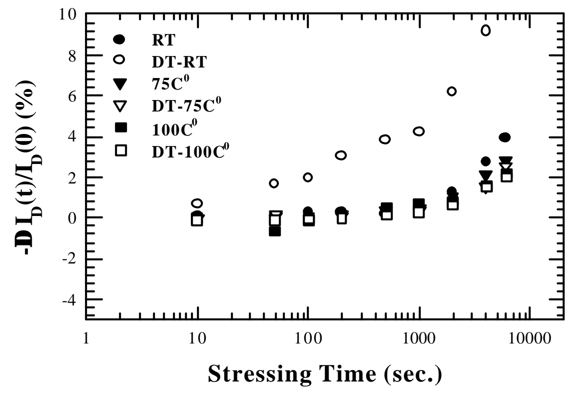
Fig. 4 Gate voltage versus transconductance between SOI pMOSFETs for different substrate bias and SOI DT-pMOSFETs for H-gate devices

Fig. 7 Linear transconductance (V_D=-0.1V) for 0.8μm H-gate device versus. Gate voltage for different stressing time, which devices were stressed at $V_G=V_{TH}$, and V_D=-4.5V.





R.T.
DT-R.T.
75C⁰
DT-75C⁰
100C⁰
DT-100C⁰
D G_mmax(t)/G_mmax(0) (%)
Stressing Time (sec.)



RT
DT-RT
75C⁰
DT-75C⁰
100C⁰
DT-100C⁰
-D I_D(t)/I_D(0) (%)
Stressing Time (sec.)