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行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告 □期中進度報告

超薄閘極氧化層 CMOS 元件軟崩潰效應研究

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摘要

關鍵字：互補金氧半電晶體、絕緣層上覆矽、超薄閘極氧化層、可靠性、軟崩潰、遲滯效應、flicker 雜訊（低頻雜訊）、浮動基極效應、漸進崩潰、漸進崩潰速率

當積體電路製程推進到奈米(sub-100nm)元件世代，絕緣層上覆矽技術的使用將是可行性的替代方案之一。當元件尺寸縮小到 100 奈米時，閘極介電層的等效氧化層厚度必須薄於 20 埃以下。然而，在如此薄氧化層的絕緣層上覆矽元件中，軟式崩潰所引發之可靠性問題將是異常重要。

本研究報告將針對超薄氧化層絕緣層上覆矽金氧半場效電晶體中軟式崩潰所引發之可靠性議題作一系列的探討。首先，在浮動基底極絕緣層上覆矽元件中，吾人知道大量的基底漏電流所造成的基底電位的調變和所導致不可避免的磁滯效應已被廣泛的討論。由於氧化層崩潰將增加基底極的穿隧漏電流，所以在浮動基底極的超薄閘極氧化層絕緣層上覆矽元件中，崩潰位置對臨界電壓磁滯現象的影響將在這部分探討。吾人將發表兩種在關閉狀態的金氧半電晶體中氧化層崩潰增強磁滯現象的模型。吾人所提供的基底充電機制和實驗結果相符。在浮動基底結構下的超薄閘極氧化層部份空乏絕緣層上覆矽金氧半場效電晶體中，軟式崩潰增強的磁滯現象將成為一種嚴重的可靠性議題。

再者，吾人發現在浮動基底絕緣層上覆矽金氧半場效電晶體中通道軟式崩潰導致一種新的低頻汲極電流雜訊退化現象。這種額外的雜訊來源來自於通道軟式崩潰導致大量基底極的價帶電子穿隧電流產生微量的白雜訊放大所致。在超薄閘極氧化層類比絕緣層上覆矽元件中，即使在操作電壓小於一伏特，通道軟式崩潰增加額外的雜訊仍會發生並將成為一個重要的可靠性問題。

最後，直接穿隧效應也會對超薄氧化層的崩潰及元件之毀壞產生影響。一般

來說，元件的毀壞與否是由氧化層崩潰所造成破壞程度所決定，代表破壞程度較低的氧化層漏電流對實際電路應用而言，並不會造成任何操作上的影響。吾人在 p 型超薄氧化層絕緣層上覆矽電晶體中，針對浮動基底極對氧化層崩潰的破壞程度作完整之研究。在 p 型超薄氧化層元件中，吾人發現了正偏壓基底極操作模式下所產生的加速崩潰破壞。當氧化層初崩潰時，高能量的通道電洞在正偏基底極時產生較大的電動加壓電流，進而使得氧化層產生更大的破壞。藉由熱載子光激發實驗及熱電洞在通道能階上的分佈分析，吾人成功地解釋出此基底極偏壓相依性。吾人並預測此種崩潰破壞將對浮動基底超薄閘極氧化層絕緣層上覆矽 p 型金氧半場效電晶體產生新的可靠性議題。

Abstract

Keywords: CMOS, SOI, ultra-thin oxide, reliability, soft breakdown, hysteresis, flicker noise (low frequency noise), floating body effect, progressive breakdown, breakdown progression rate

The silicon-on-insulator (SOI) technology is a promising candidate of IC manufacture required for sub-100nm CMOS devices. As device size shrinks below 100nm, the effective oxide thickness of gate dielectric must scale below 20Å. While, a great reliability concern induced by soft breakdown (SBD) in such thin oxides SOI devices is being aroused.

The objective of this report is to investigate soft breakdown induced reliability issues in such ultra-thin oxide SOI MOSFETs. First of all, substrate leakage current has been known to cause substrate bias variation and induce unavoidable hysteresis effects in floating body SOI devices. Since oxide breakdown can enhance substrate tunneling leakage current, the impact of breakdown location on threshold voltage hysteresis in ultra-thin oxide SOI devices is investigated in this part. Two breakdown enhanced hysteresis modes in off-state CMOS are identified. The proposed body charging mechanisms are verified by our measurement results. The SBD enhanced

hysteresis effect would be a serious reliability subject in ultra-thin oxide MOSFETs with floating body configuration.

Moreover, a new low frequency drain current noise source in floating body SOI nMOSFETs caused by channel soft breakdown is studied. The excess noise originates from channel soft breakdown enhanced valence band electron tunneling and the amplification by the small white noise of the substrate current. The c-SBD enhanced excess noise may occur even with supply voltage less than 1.0V and would be an important reliability problem in analog applications.

Finally, a large direct tunneling current can decrease oxide time-to-breakdown and limit oxide further scaling. Actually in most circuits, the failure criterion is determined by the hardness of oxide breakdown. In this part, floating body enhanced breakdown progression in ultra-thin oxide SOI pMOS is proposed. The enhanced progression is attributed to the increase of hole tunneling current resulting from breakdown induced channel carrier heating. The substrate bias dependence of post-breakdown hole tunneling current is confirmed through the calculation of channel hole distribution in sub-bands. This observed phenomenon is significant to ultra-thin gate oxide reliability in floating body SOI pMOSFETs.

Contents

Figure Caption

Table Caption

Chapter 1
Introduction

Gate oxide thickness scaling has been recognized as one of major keys in CMOS device scaling. With the device shrinkage, gate oxides below 2 nm are needed for sub-100nm CMOS technology. It is amazing that such thin oxide doesn't suffer much from extrinsic factors such as defect density, surface roughness and uniformity control. The physical limitation of oxide thickness is caused by quantum-mechanical tunneling of carriers. The direct tunneling current increases exponentially by about one order of magnitude for every 2~3Å reduction in oxide thickness [1.1]. Large tunneling currents with device scaling make oxide breakdown play an important role in reliability issues. Additionally, silicon-on-insulator (SOI) CMOS has been emerged as one promising solution to increase the performance of CMOS over that offered by simple scaling.[1.2,1.3] In bulk CMOS, the oxide soft breakdown (SBD) just increases the tunneling leakage current and does not disrupt circuit operation.[1.4] In fact, this unnecessary leakage current not only causes increased power dissipation but also may bring about some reliability subjects such as hysteresis effects, noise degradation and oxide breakdown in ultra-thin oxide SOI CMOS devices.

Partially Depleted (PD) SOI MOSFETs have the advantages in better threshold voltage control and easier fabrication process than fully depleted SOI MOSFETs. However, the floating body configuration of PD SOI MOSFETs has aroused several serious problems in device characteristics. An excess substrate leakage current can charge the substrate and cause annoying hysteresis effects. The SBD enhanced substrate tunneling leakage current may make the hysteresis effects more serious in PD SOI CMOS. The influence of SBD location on hysteresis effects in PD SOI MOSFETs will be investigated in various device operation modes.

High performance SOI MOSFETs have been the primary platform of RF and microwave

analogy circuits due to reduced junction capacitance and also due to the benefits of a high receptivity substrate.[1.5,1.6] Low-frequency noise is a key design constraint and an important figure-of-merit in analogy MOS circuits. Moreover, unwanted floating-body effects including the excess low-frequency noise have been extensively studied for SOI MOSFETs.[1.7,1.8] In this thesis, we will explore the noise properties of PD SOI MOSFETs in different SBD modes. The impact of SBD location on low frequency noise in SOI devices will be investigated in this thesis, too.

Time dependence dielectric breakdown (TDDB) is an important reliability index of ultra-thin gate oxide. Although stress oxide field of SOI MOSFETs is not varied by floating body induced forward substrate bias, the negative substrate bias may enhance the pMOS breakdown progression.[1.9,1.10] The comparison of breakdown hardness in SOI and bulk pMOSFETs will be discussed in this thesis. Our result shows that oxide breakdown rate is enhanced in SOI devices. This points toward that SBD will be an urgent reliability issue in ultra-thin PD SOI MOSFETs.

Organization of This Report

This report is organized into five chapters.

Following the introduction, the impact of oxide soft breakdown location on threshold voltage hysteresis in PD SOI MOSFETs with an ultra-thin oxide is investigated in Chapter 2. Two breakdown enhanced threshold voltage hysteresis modes are identified. In a drain-edge breakdown device, excess holes resulting from band-to-band tunneling flow to the floating body, thus causing threshold voltage variation in drain bias switching. In contrast, in a channel breakdown device, enhanced threshold hysteresis is observed during gate bias switching because of increased valence band electron tunneling. Our findings reveal that soft breakdown enhanced hysteresis effects can be a serious reliability issue in ultra-thin oxide SOI devices with floating body configuration.

In Chapter 3, a new low frequency noise degradation mode in nMOSFETs due to breakdown enhanced floating body effect is proposed. In a channel breakdown device, a noise overshoot phenomenon is observed in the ohmic regime. It is characterized by a peak in drain current noise spectral density versus the operation gate voltage, whereby the peak amplitude can be about one order of magnitude higher than the background 1/f noise. In addition, it is shown that the corresponding spectrum has a Lorentzian shape. The origin of this excess noise is due to c-SBD enhanced valance band electron tunneling induced amplification of the substrate shot noise. The excess low frequency noise model in SOI MOSFETs is also proposed. The findings indicate that c-SBD enhanced drain current noise can be a reliability issue in PD analog SOI CMOS circuit.

In Chapter 4, enhanced oxide breakdown progression in ultra-thin oxide SOI pMOS is observed, as compared to bulk devices. The enhanced progression is attributed to the increase of hole stress current resulting from breakdown induced channel carrier heating in a floating-body configuration. Numerical analysis of hole tunneling current and hot carrier luminescence measurement are performed to support our proposed theory. This phenomenon is particularly significant to the reliability of floating body SOI pMOS with thinner oxides and lower gate voltage. Conclusions are finally made in Chapter 5.

Chapter 2
Soft Breakdown Enhanced Hysteresis Effects in Ultra-Thin Oxide SOI MOSFETs

2.1 Introduction

Silicon-on-insulator (SOI) technology has emerged as a promising technology for system-on-a-chip applications, which require high-performance complementary metal-oxide-semiconductor (CMOS) field effect transistors (MOSFETs), low power, embedded memory, and bipolar devices. The primary feature of a MOSFET with SOI configuration is that the local substrate of the device is floating electrically, and thus the substrate-source bias (V_{BS}) is not fixed. As V_{BS} changes, the device threshold voltage (V_t) will change due to the body effect. This "instability" in V_t resulting from floating body configuration becomes one of the most challenging tasks in bringing SOI devices into mainstream applications.[2.1-2.4] One manifestation of the V_t variation is the hysteresis effect. The V_t hysteresis as a result of various floating body charging/discharging mechanisms has been widely investigated.[2.2-2.4] In this work, the influence of gate oxide breakdown position on hysteresis effects in ultra-thin oxide partially-depleted (PD) SOI MOSFETs will be explored.

Several causes of V_t hysteresis in PD SOI MOSFETs have been proposed.[2.5-2.8] Boudou et al [2.5] reported that V_t hysteresis could be caused by positive feedback of impact ionization due to long time constants associated with body potential charging. Chen et al [2.6] showed that at high drain biases the floating body effect can lead to hysteresis in the sub-threshold I_{ds}-V_{gs} characteristics even when the gate is biased well below its threshold voltage. Fung et al [2.7] found that in ultra thin gate oxide devices the gate-to-body tunneling current modulates the body voltage and induces a hysteresis effect. All the above works investigate the hysteresis phenomenon in PD SOI MOSFETs without considering gate oxide

soft breakdown (SBD). Recent studies [2.9-2.13] showed that in bulk CMOS the impact of gate oxide SBD is only manifested in a noticeable increase in gate leakage current without degrading other device characteristics in operation. Crupi et al [2.14] showed that at high gate voltages the substrate current steeply increases after SBD due to localized effective thinning of gate oxide. Chan et al [2.15] presented that in thinner oxides the post-SBD gate induced drain leakage (GIDL) current increases significantly because of the enhancement of band-to-band tunneling. Although the dependence of these excess substrate currents on the location of a SBD spot was widely explored, the influence of SBD location on V_t hysteresis in SOI devices has been rarely investigated.

2.2 Device Structure and Characterization

The devices in this work were made with a 0.13μm standard CMOS process on p-type PD SOI substrate. The gate oxide was grown with rapid plasma nitridation (RPN) process. The gate length is 0.13μm, the gate width is 10μm and the oxide thickness is 1.6nm. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this chapter, all devices were stressed at high constant gate voltage with the source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection was chosen to be 10μA. After breakdown, the device on-state characteristics were checked and no difference was observed.

The breakdown position was examined by using the method proposed by Degraeve et al.[2.16] Table 2.1 shows the ratio of I_d to (I_s+I_d) before and after SBD in four SOI devices. The measurement is in accumulation region and $|V_g|$=1.5V and $V_d=V_s$=0V. A significant increase of $I_d/(I_s+I_d)$ in device B and device D indicates that breakdown is located at the drain edge, while in device A and device C the moderate change in $I_d/(I_s+I_d)$ implies that the SBD position is in the channel. Aside from $I_d/(I_s+I_d)$, $I_b/(I_s+I_d)$ was measured (also shown in Table

2.1). In the channel SBD (c-SBD) devices, the valence band tunneling leakage in the channel region (I_b) was enhanced, resulting in a larger $I_b/(I_s+I_d)$. In the case of edge SBD (e-SBD), the breakdown was above the drain edge. As a result, the tunneling leakage current in the channel region remains almost the same as in pre-SBD, and the increased edge leakage current makes I_s+I_d larger and thus a smaller $I_b/(I_s+I_d)$. In short, the results in Table 2.1 shows that we can use the change of $I_d/(I_s+I_d)$ or $I_b/(I_s+I_d)$ to determine the breakdown location in the channel or in the drain edge region.

By utilizing the above technique, the device electrical behaviors in c-SBD and e-SBD devices were characterized. In Fig. 2.1, the gate current and the substrate current as a function of V_g in a fresh, a c-SBD, and an e-SBD nMOSFET were compared. The result shows that the substrate current increases drastically after c-SBD, but has little change after e-SBD. The substrate current at a positive gate bias is attributed to valence electron tunneling from the channel to the gate. The generated holes left behind in the channel then flow to the substrate. This tunneling process is unlikely to occur in the n^+ drain region since the valence-band edge of the n^+ drain is aligned with the band-gap of the n^+ poly-gate. Thus, I_b is enhanced significantly at a positive gate bias in a c-SBD device due to localized effective oxide thinning [2.14, 2.17-2.18] while I_b in an e-SBD device is nearly unchanged. Fig. 2.2 shows the drain bias dependence of the GIDL current before and after SBD. The substrate current has an apparent increase after edge SBD. This is because at a high drain bias the I_b comes from electron band-to-band tunneling in the drain depletion region and the generated holes flow to the substrate. Since the electrical field in the drain region becomes stronger after e-SBD due to effectively oxide thinning, the GIDL (I_b) in an e-SBD device is enhanced. The same phenomena in p-MOSFETs are also observed and the result is shown in Fig. 2.3.

2.3 Modes of SBD Enhanced Hysteresis

Two modes of SBD enhanced body potential alteration are proposed. Fig. 2.4 illustrates two floating-body charging processes in c-SBD and in e-SBD SOI nMOSFETs.[2.19-2.20] In a c-SBD device with a positive gate bias (Fig. 2.4(a)), valence band electron tunneling from the channel to the gate is increased after SBD. The generated holes flow to the body and raise the body potential. Fig. 2.4(b) shows the drain-induced floating-body charging in an e-SBD nMOSFET. Since the breakdown path is in the drain edge, the GIDL current increases due to a stronger band bending in the n^+ drain region, thus raising the body potential at a high drain bias. On the contrary, the GIDL current does not change in a c-SBD device. Likewise, Fig. 2.5 shows two possible floating-body charging processes in pMOSFETs. Due to the above two charging processes, we conclude that the body potential of both nMOSFET and pMOSFET can be modified either during gate switching or during drain switching depending on the location of a SBD spot.

2.4 Results and Discussion

Fig. 2.6 shows the I_{ds}-V_{gs} hysteresis in a PD SOI nMOSFET before and after c-SBD. The measurement drain bias is 0.1V. The gate bias is swept from 0V to 1.3V and then is reversely swept from 1.3 to 0V. Note that (i) the sub-threshold hysteresis before SBD is insignificant and (ii) the post-SBD hysteresis is induced by gate bias sweep in this device. The corresponding body potential fluctuation in gate bias sweep is shown in Fig. 2.6. The arrow in the figure indicates the direction of bias sweep. After c-SBD, the body potential begins to rise when the V_g amplitude is above 0.8V. The gate switching induced body potential variation can be as large as 0.3V in this case. The pre-SBD body potential hysteresis at the same switching amplitude is less than a few tens of milli-volts. The c-SBD induced V_t hysteresis is also observed in a pMOSFET. The measurement data are not shown here.

In an e-SBD device, although gate enhanced hysteresis is not observed, drain sweep induced hysteresis in sub-threshold leakage current is remarkable (Fig. 2.7). In this figure, the measurement V_{gs} is 0V and the drain bias is swept from 0V to 1.3V and then reversely swept back. The body potential variation is shown in Fig. 2.7, too. The e-SBD enhanced hysteresis effect is clearly shown in this figure. It should be noted these breakdown-induced hysteresis effects occurs in off-state rather than in on-state where hot carrier impact ionization has been reported as a responsible charging mechanism.[2.5]

The relationship between the magnitude of sweep voltage and the body potential hysteresis in the two SBD modes is investigated. In nMOSFETs, the degree of hysteresis in terms of the body potential variation versus the amplitude of the sweep voltage is shown in Fig. 2.8 for gate bias sweep and in Fig. 2.9 for drain bias sweep. The hysteresis voltage is defined as the maximum substrate charging voltage during the sweep. In gate bias sweep (Fig. 2.8), the c-SBD device shows an increased hysteresis voltage while the hysteresis voltage of the e-SBD device is almost unchanged. In contrast, the e-SBD device shows a larger hysteresis voltage in drain bias sweep (Fig. 2.9). Similar results in pMOSFETs are presented

in Fig. 2.10 for gate bias sweep and in Fig. 2.11 for drain bias sweep. From our characterization, we found SBD induced hysteresis effect may become appreciable even when the supply voltage is below 0.8V.

The impact of SBD enhanced body charging effect in CMOS operation is described as follows. Fig. 2.12 illustrates the dominant V_t hysteresis modes in a SOI CMOS inverter. Hot carrier (HC) induced floating body charging occurs in on state [2.1,2.5] and it is dominant only when the inverter is during switching. On the other hand, floating body charging takes place in c-SBD (e-SBD) nMOSFETs and e-SBD (c-SBD) pMOSFETs when the input signal is at high (low) state. Since the soft breakdown induced body charging is in the off state, the time for charging can be much longer than the on-state HC caused body charging. Our study reveals that SBD in PD SOI MOSFETs not only increases leakage current but also affects circuit stability.

2.5 Summary

The significance of soft breakdown position to V_t hysteresis in PD SOI CMOS devices has been evaluated. Two SBD enhanced hysteresis modes in off-state CMOS are identified. The dominant floating body charging mechanism is valence band tunneling in c-SBD devices and band-to-band tunneling in e-SBD devices. The SBD enhanced hysteresis effect may occur even with supply voltage less than 1.0V and would be a serious reliability concern in ultra-thin oxide PD SOI circuits.

acc. region	nMOSFET		pMOSFET	
	device A (c-SBD)	device B (e-SBD)	device C (c-SBD)	device D (e-SBD)
I_d/I_s+I_d before SBD	0.5078	0.5297	0.5174	0.5251
I_d/I_s+I_d after SBD	**0.4482**	**0.9957**	**0.1368**	**0.9387**
I_b/I_s+I_d before SBD	0.0287	0.0178	0.3202	0.1163
I_b/I_s+I_d after SBD	**0.1426**	**0.0001**	**10.8680**	**0.0102**

Table 2.1The ratio of $I_d/(I_s+I_d)$ and $I_b/(I_s+I_d)$ before and after soft breakdown in four SOI MOSFETs. The measurement is in the accumulation region and V_g= |1.5V|, $V_d=V_s$=0V.

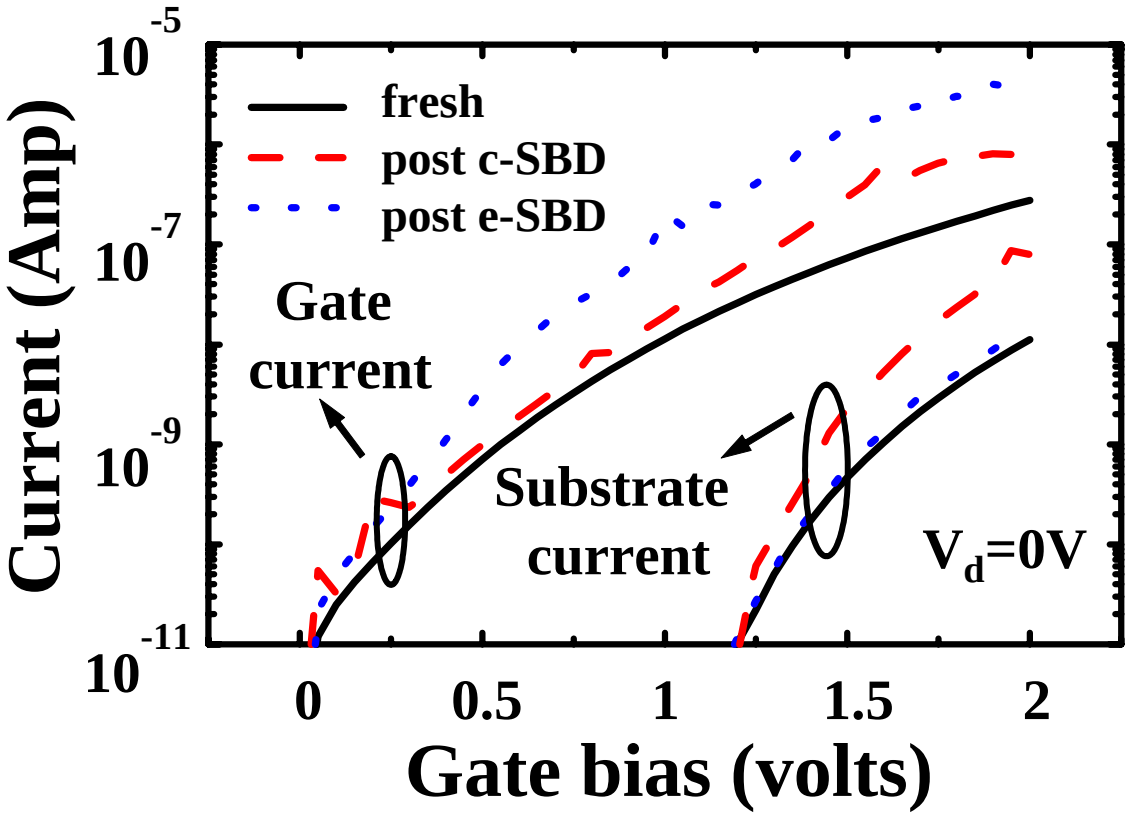

Fig.2.1 Gate current and substrate current versus gate bias in nMOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

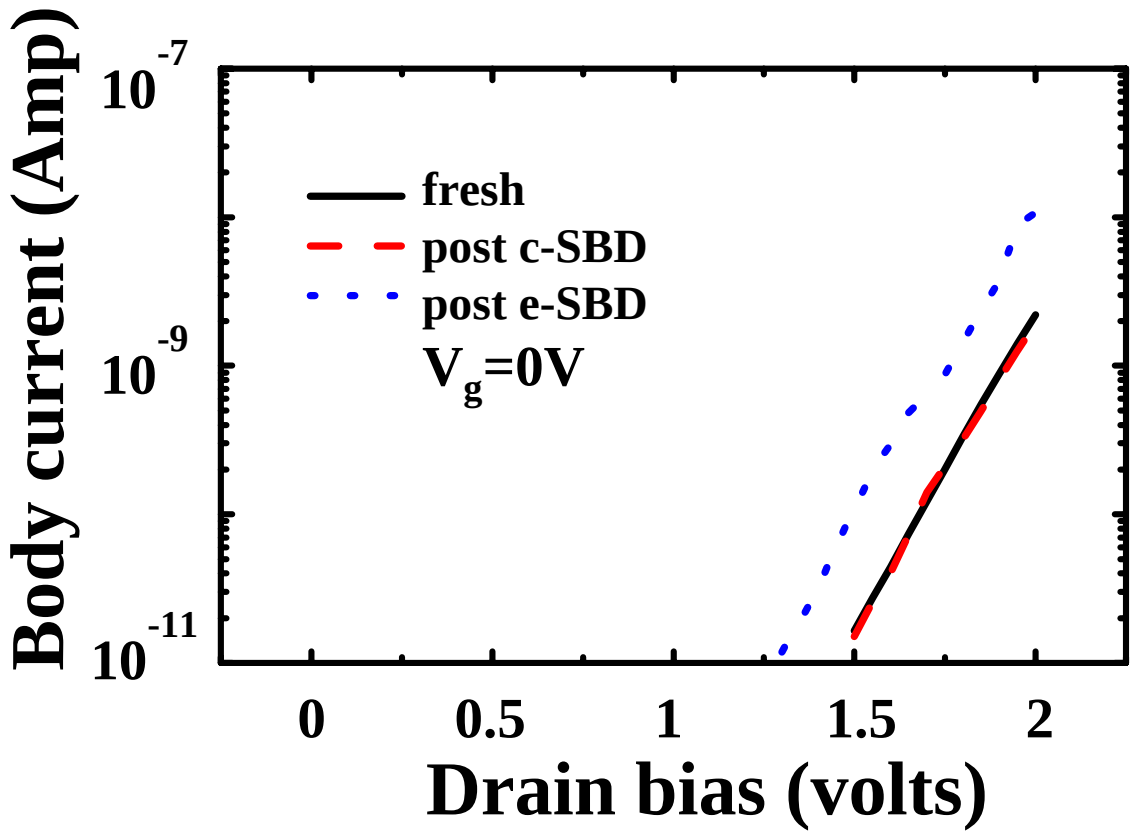

Fig.2.2 Body current versus drain bias in nMOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

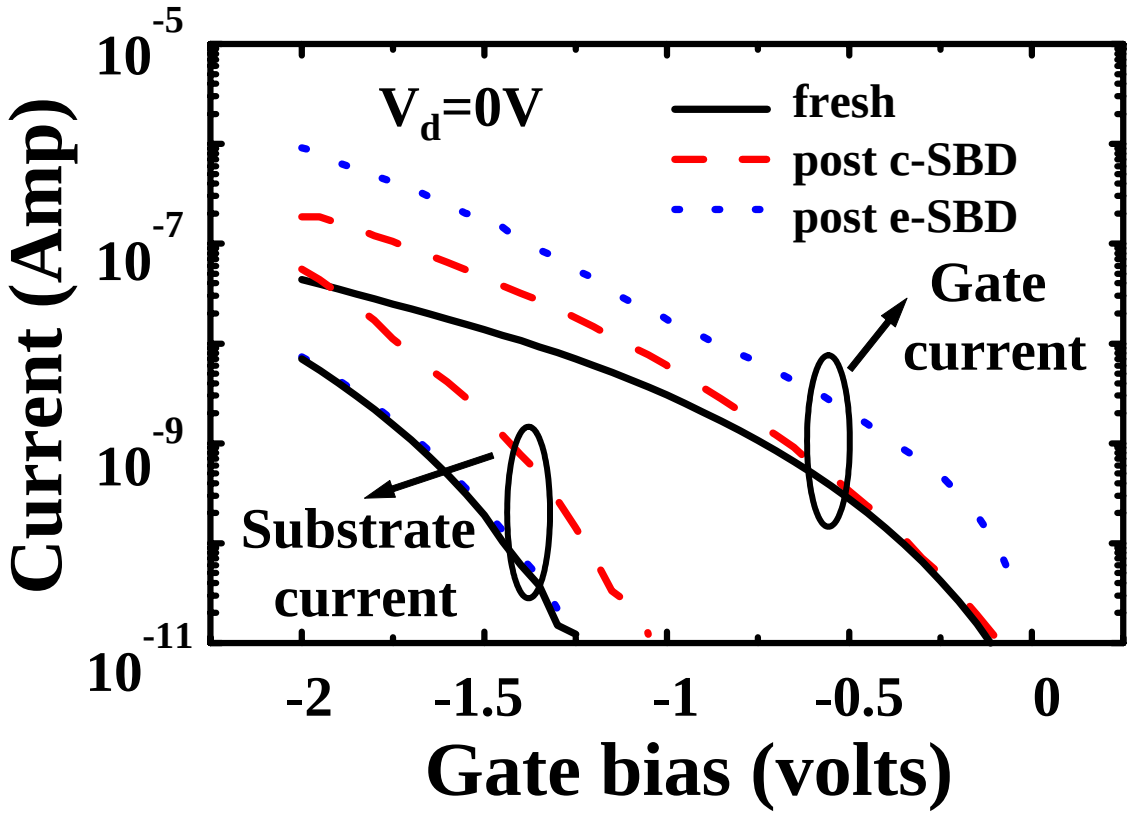

Fig.2.3 Gate current and substrate current versus gate bias in pMOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

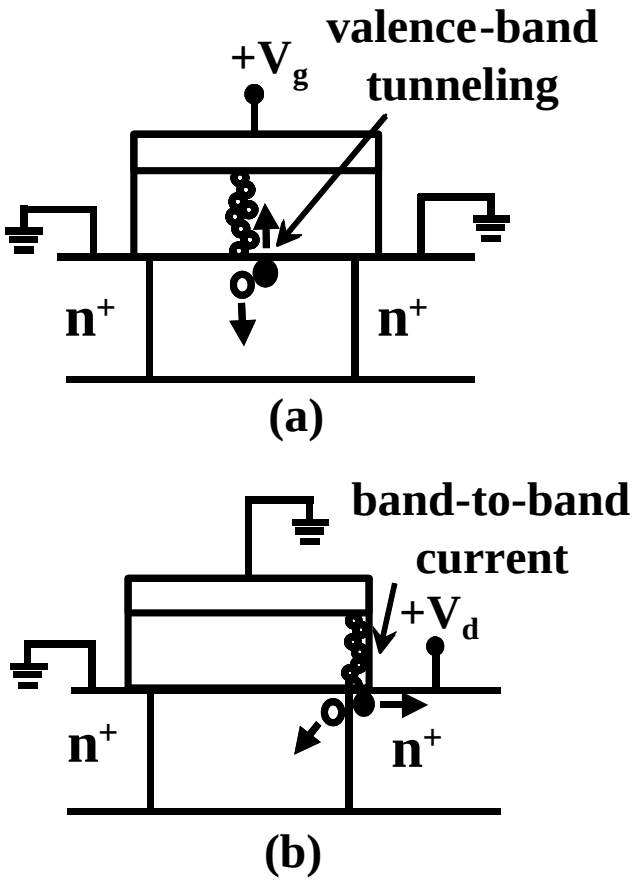

Fig.2.4 Illustration of two soft-breakdown enhanced floating-body charging processes in SOI nMOSFETs. (a) soft breakdown in the channel region and hole creation due to valence band electron tunneling; (b) soft breakdown in the drain region and enhanced GIDL current.

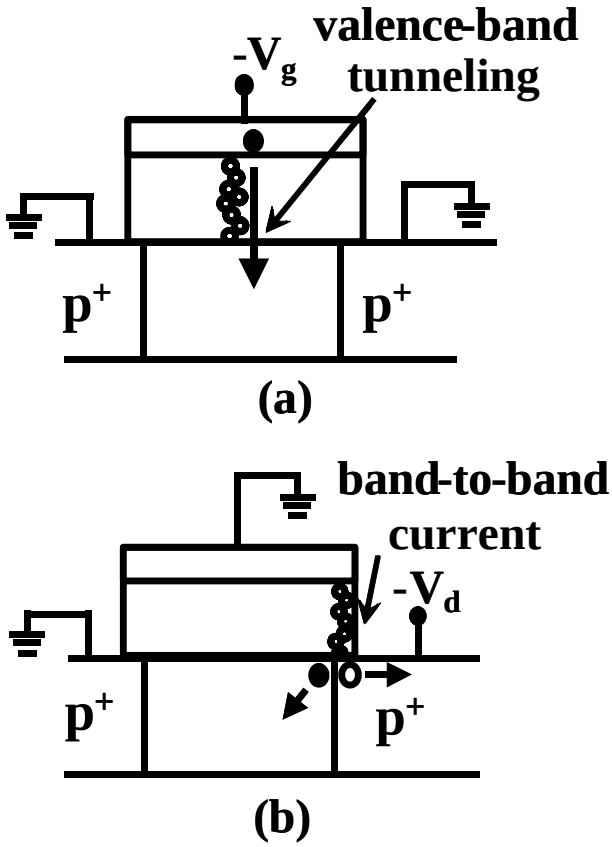

Fig.2.5 Illustration of two soft-breakdown enhanced floating-body charging processes in SOI pMOSFETs. (a) soft breakdown in the channel region and valence band electron tunneling from poly-gate to the floating body; (b) soft breakdown in the drain region and enhanced GIDL current.

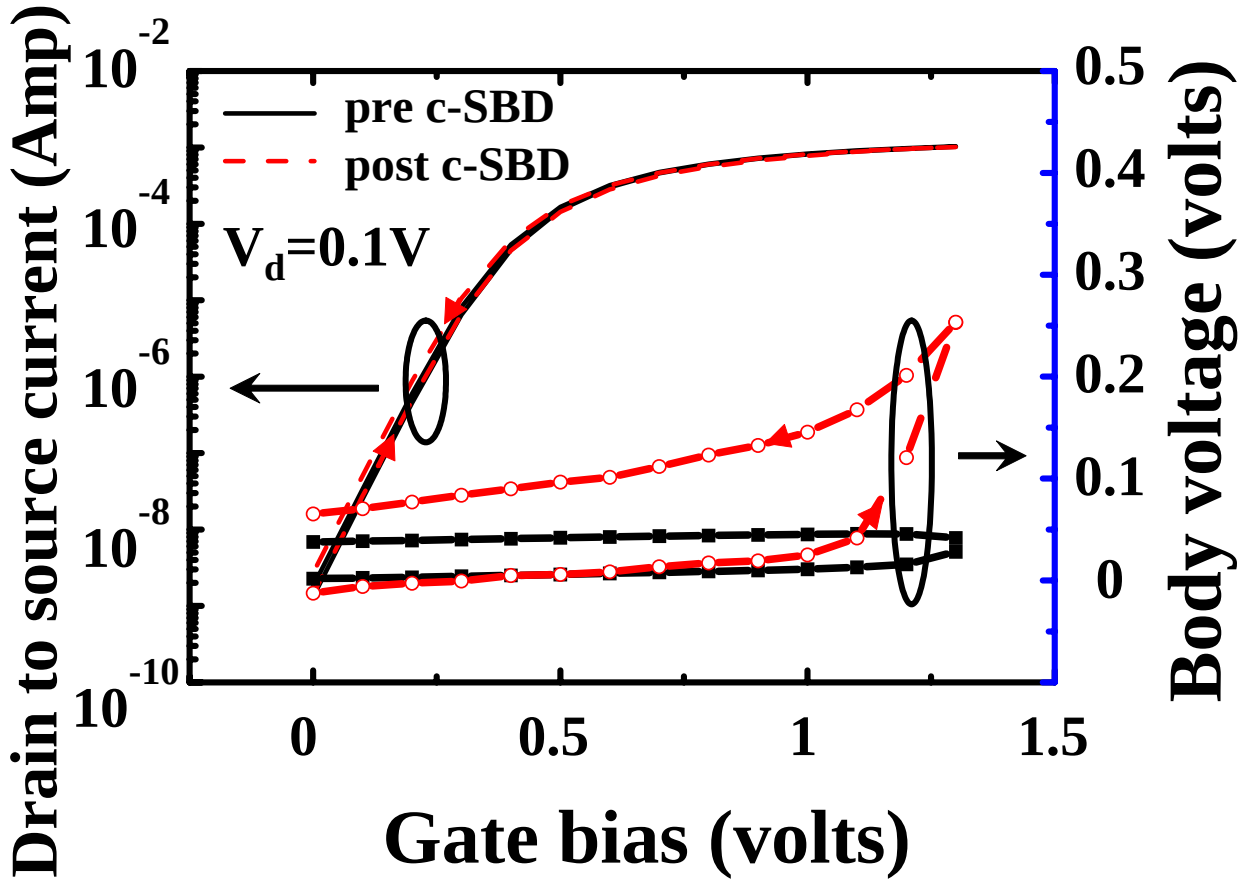

Fig.2.6 Hysteresis in I_{ds} and corresponding floating-body potential versus V_g in a c-SBD SOI nMOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0V to 1.3V.

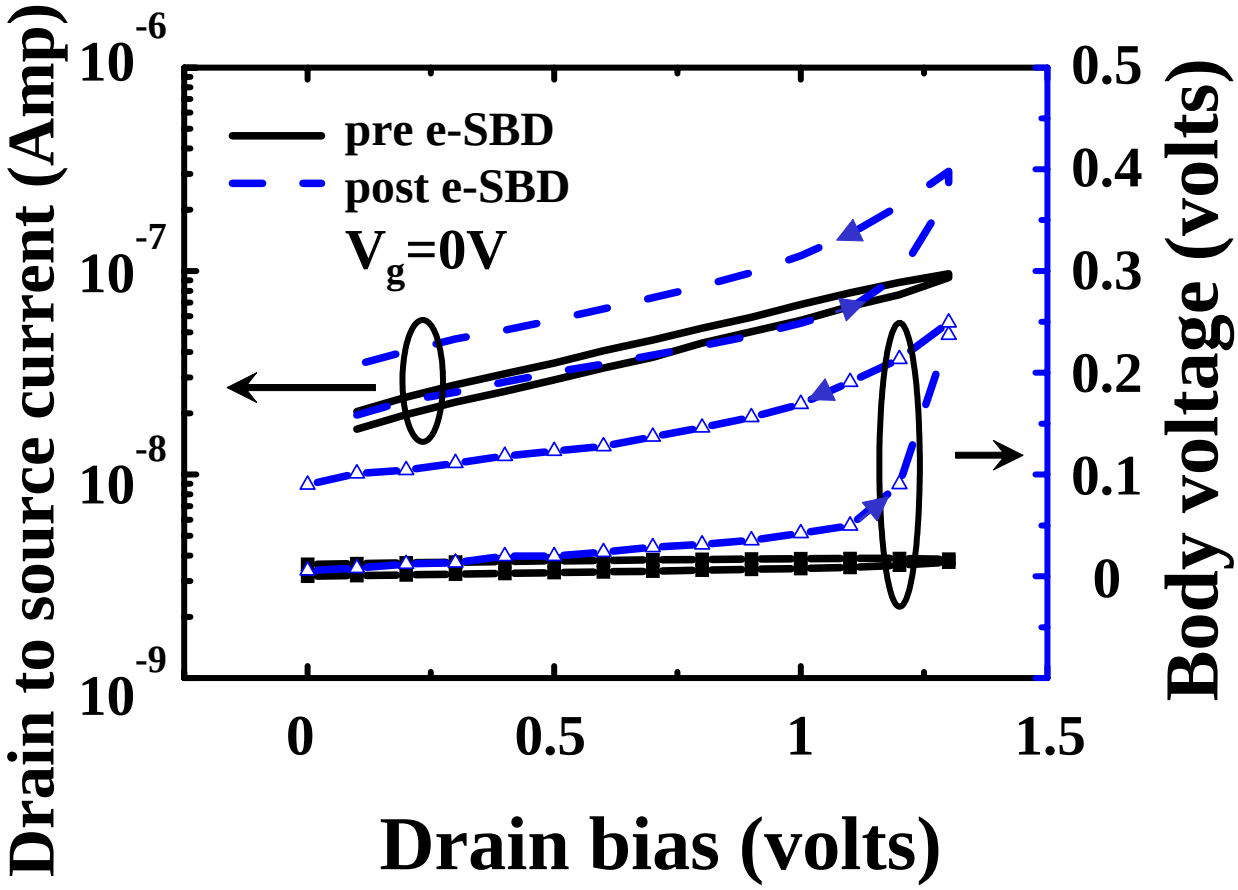

Fig.2.7 Hysteresis in sub-threshold current and corresponding floating-body potential in an e-SBD SOI nMOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0V to 1.3V.

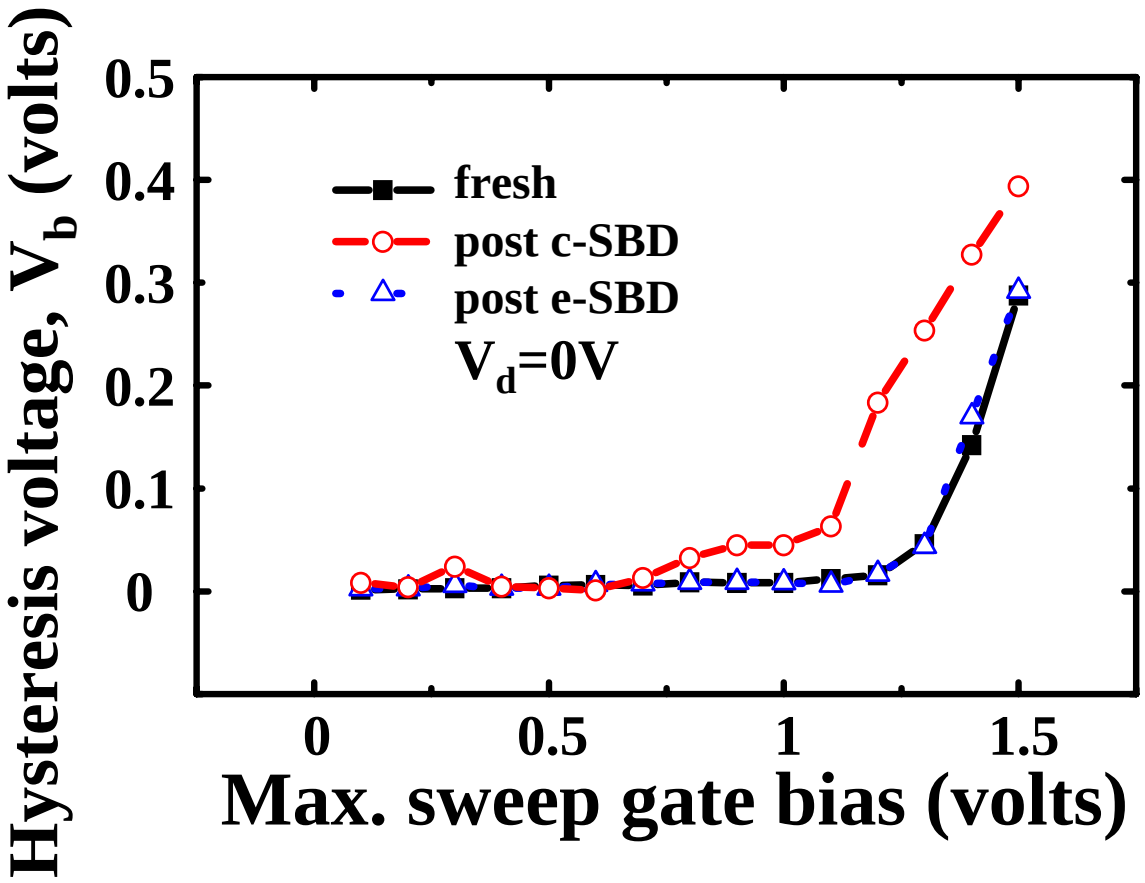

Fig.2.8 The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI nMOSFETs. V_d=0V.

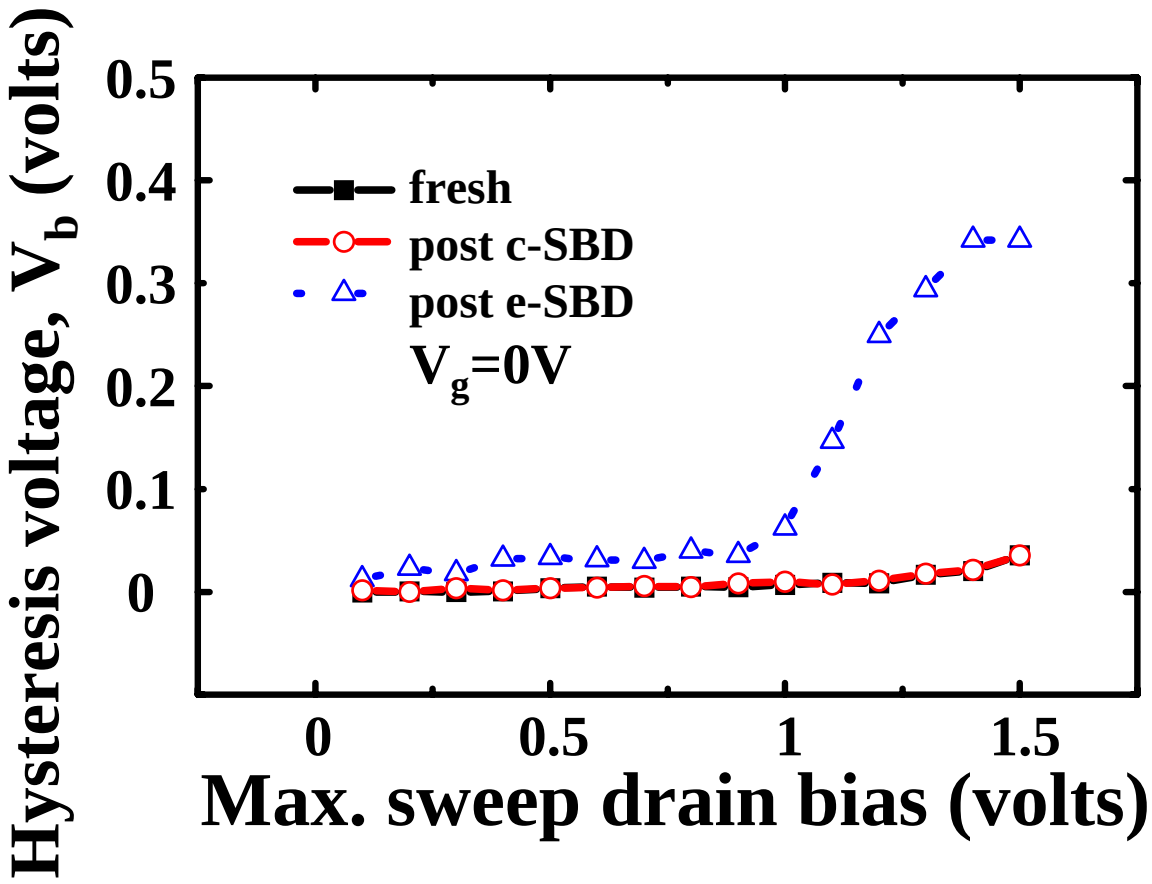

Fig.2.9 The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI nMOSFETs. V_g=0V.

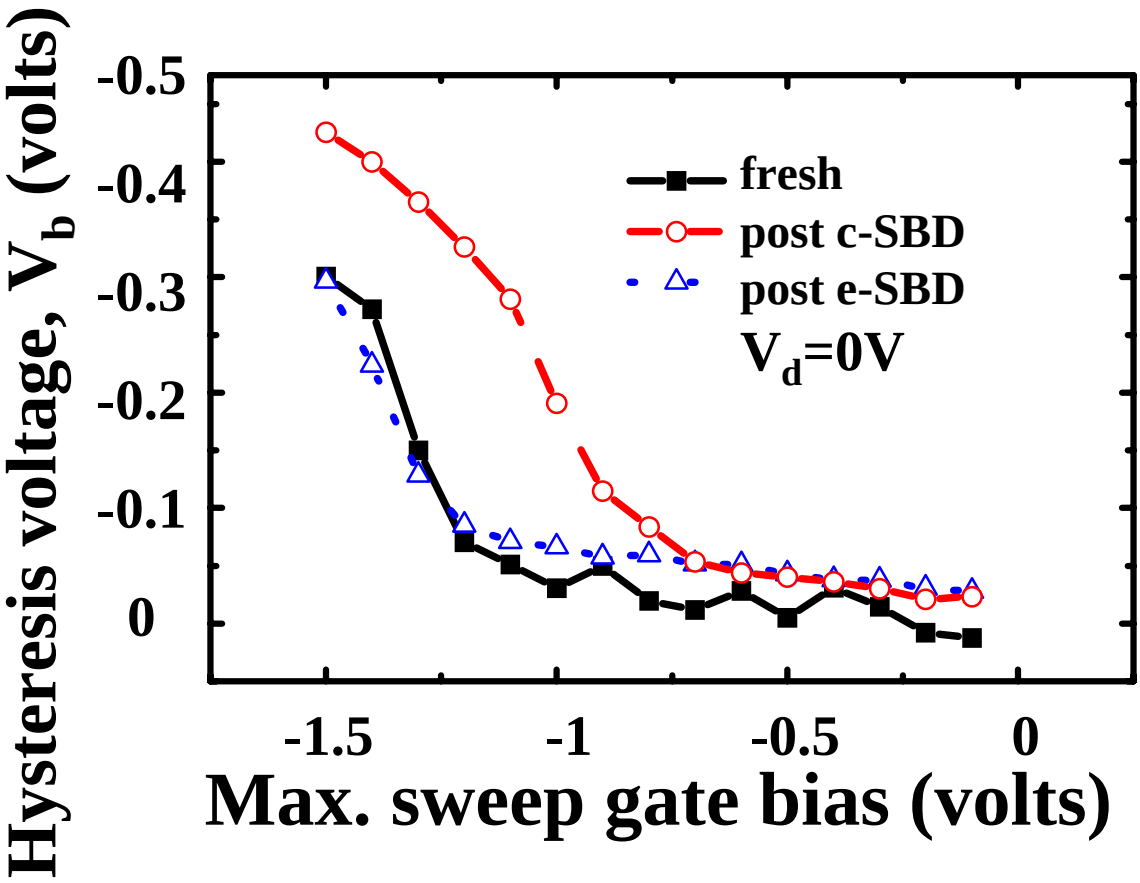

Fig.2.10 The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI pMOSFETs. V_d=0V.

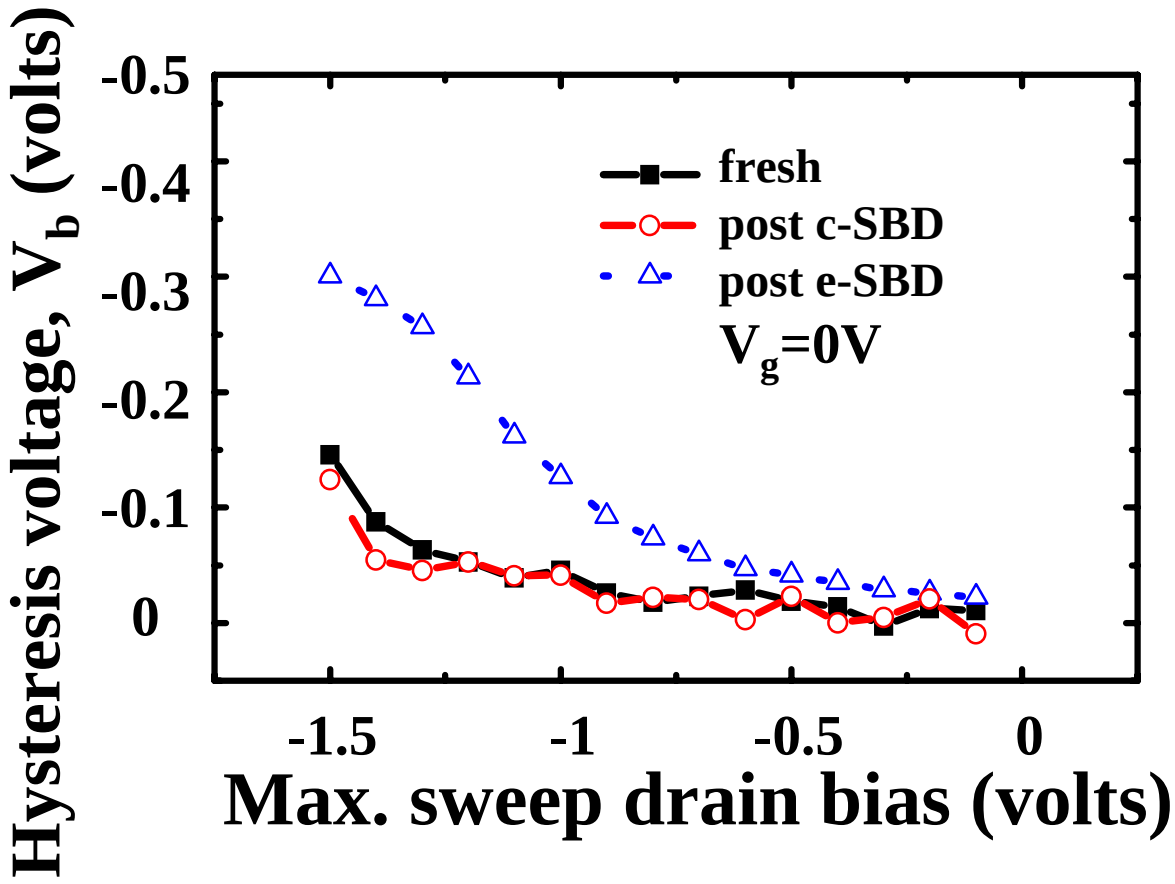

Fig.2.11 The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI pMOSFETs. V_g=0V.

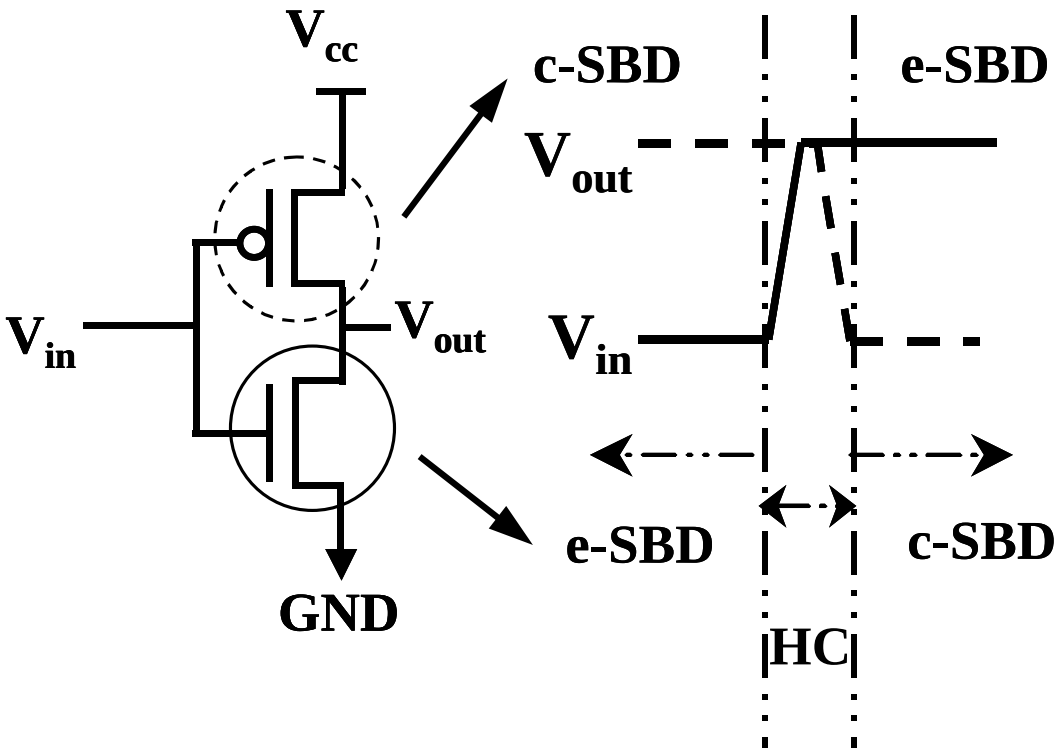

Fig.2.12 Illustration of dominant V_t hysteresis modes in the switching of an SOI CMOS inverter.

Chapter 3
Soft Breakdown Enhanced Excess Low-Frequency Noise in Ultra-Thin Oxide SOI n-MOSFETs

3.1 Introduction

Silicon-on-insulator (SOI) technology also has regarded as a hopeful technology for system-on-a-chip applications, which require high-performance, low power, fully integrated RF, and mixed-signal circuits.[3.1-3.5] However, the troublesome floating-body effect (FBE) in PD SOI MOSFETs leads to kink in drain current characteristics as well as some undesirable transient effects.[3.1-3.4] FBE also gives rise to excess low-frequency noise with a Lorentzian-like spectrum in floating body PD SOI devices, posing a serious problem for base band signal processing system.[3.6-3.9] The observed Lorentzian shaped noise is caused by white thermal noise (Nyquist or shot) sources associated with the generation and removal of body charge.[3.6] The Lorentzian signature is obtained through the trans-impedances coupling these internal white noise sources to the terminals of the SOI device.[3.7] Several causes of the Lorentzian-like spectrum in SOI MOSFETs have been proposed. The origin of these floating body noises could be related to high drain bias induced impact ionization current and large gate bias induced valance band electron tunneling through the ultra-thin gate oxide.[3.9-3.10] Chapter 3 has pointed out that soft breakdown enhanced substrate tunneling current would induce threshold voltage (V_t) hysteresis effects in PD SOI MOSFETS.[3.11] The aim of this chapter is to describe the impact of soft breakdown location on the excess low-frequency noise for SOI devices with floating body configuration.

In the beginning, the excess noise model in PD SOI MOSFETs is introduced. Then, the kink effect in ultra-thin oxide floating body SOI n-MOSFETs is studied, which would induce excess low frequency noise. After that**,** the impact of soft breakdown location on drain current noise in ultra-thin oxide SOI n-MOSFETs is investigated. In a channel breakdown device, a

noise overshoot phenomenon is observed in the ohmic regime. It is characterized by a peak in current noise spectral density versus the operation gate voltage, whereby the peak amplitude can be about one order of magnitude higher than the background flicker noise. The origin of this excess noise is believed due to soft breakdown (SBD) enhanced valance-band electron tunneling and thus induced floating body effect. The findings indicate that channel SBD enhanced drain current noise can be a reliability issue in PD analog SOI CMOS circuit.

3.2 Excess Low-Frequency Noise Model in SOI MOSFETs

The major noise sources of an SOI MOSFETs operating in strong inversion are shown in Fig. 3.1. There are two noise sources associated with the conducting channel. One is flicker (1/f) noise which contributes to the low-frequency noise, the other is thermal noise which dominates at high frequency. In addition to the noise in the channel, there are two shot noise sources associated with the floating-body, which are due to the impact ionization current and the body-source diode current, respectively. In bulk MOSFET, only 1/f noise can be observed at low-frequency. However, excess noise is found in floating-body PD SOI MOSFET. The excess noise originates in the two shot noises. Although the shot noises are small in magnitude compared with flicker noise, they are amplified by FBE and give rise to the excess low-frequency noise in PD SOI MOSFET. The low-frequency noise in floating-body PD SOI MOSFET's includes white noise, flicker noise and the FBE-induced excess noise.

A. White Noise

The white noise component originates from thermal random motion of carriers in the channel.

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B. Flicker Noise

Flicker noise is a fluctuation in conductance with a power spectral density proportional to

$1/f^{\beta}$, where β is close to unity so that flicker is normally called 1/f noise. There is no consensus to the origin of the 1/f noise, it is very likely that there exist more than one mechanism giving rise to the same noise characteristics. According to McWhorter's number fluctuation theory [3.12], 1/f noise is attributed to the trapping and de-trapping processes of the charges in the oxide traps close to the Si–SiO_2 interface. Hooge's empirical model [3.13], however, considers the 1/f noise as a result of carrier mobility fluctuation due to lattice scattering. It has been reported that both the carrier number fluctuation and the mobility fluctuation are possible mechanisms which lead to the 1/f noise in MOSFET's [3.14-3.15]. Hence, for the 1/f noise, a correlated noise model [3.14] which incorporates both mechanisms is applied

$$S_{id-1/f} = \frac{kTqI_{ds}\mu_{eff}}{\gamma f L_{eff}^{\ 2}} \int_0^{V_{ds}} \frac{N_t(E_f)}{N} (1+\alpha\mu_{eff} N)^2 \, dV \tag{3.1}$$

where

$S_{id-1/f}$	1/f noise current spectral density;
I_{ds}	drain current;
μ_{eff}	effective mobility;
γ	attenuation coefficient of the electron wave function in the oxide;
L_{eff}	effective channel length of the device;
V_{ds}	drain bias;
$N_t(E_f)$	oxide trap concentration around the quasi-Fermi level along the channel;
N	carrier concentration along the channel;
α	lattice scattering coefficient.

C. Excess Low Frequency Noise

The excess low-frequency noise is specific to PD SOI MOSFET's associated with the floating-body effect (FBE). The noise small-signal equivalent circuit shown in Fig. 3.2(a) can explain the mechanism underlying the excess low-frequency noise [3.6]. The shot noise results from the impact ionization current (I_{ii}):

$$S_{ib1} = M \cdot 2qI_{ii} \tag{3.2}$$

where **M** is a multiplication factor [3.16]. Impact ionization current exhibits shot noise because only the carriers with sufficient kinetic energy can generate electron-hole pairs. The second noise source is associated with the body-source diode current ($\mathbf{I_{bs}}$) where carriers have to overcome the built-in potential barrier:

$$S_{ib2} = 2qI_{bs} \tag{3.3}$$

The two noise current flow through the body-ground impedance (c_{eq} and r_{eq}), leading to a fluctuation in body potential:

$$S_{vb} = S_{ib} \cdot |\, z_b \,|^2 = S_{ib} \cdot |\, (\frac{1}{r_{eq}} + j\omega c_{eq})^{-1} \,|^2$$

$$= S_{ib} \cdot \frac{r_{eq}^{\ 2}}{1 + (\frac{f}{f_c})^2} \tag{3.4}$$

where

$$S_{ib} = S_{ib1} + S_{ib2} \quad \text{and} \quad f_c = \frac{1}{2\pi \cdot r_{eq} c_{eq}}$$

The equivalent body-ground resistance r_{eq} is equal to the small-signal resistance of the body-source junction. The equivalent body-ground capacitance c_{eq} can be modeled as the sum of all the capacitance seen from the body. The schematic for r_{eq} and c_{eq} is shown in Fig. 3.2(b). And, the fluctuation in the body potential modulates the threshold voltage of the device:

$$S_{vth} = S_{vb} \cdot (\frac{\partial V_{th}}{\partial V_{bs}})^2 \tag{3.5}$$

Due to the fluctuation in $\mathbf{V_{th}}$, the excess drain current noise is given by:

$$\begin{aligned} S_{id-excess} &= S_{vth} \cdot (\frac{\partial I_{ds}}{\partial V_{th}})^2 \\ &= \frac{(M+1) \cdot 2qI_{ii} g_{mb}{}^2 r_{eq}{}^2}{1+(\frac{f}{f_c})^2} \end{aligned} \tag{3.6}$$

where $\mathbf{g_{mb}}$ is the body trans-conductance. The excess noise shows a Lorentzian power spectrum, which is characterized by a constant plateau at low frequency and a $1/f^2$ roll-off at higher frequencies.

Since white noise, 1/f noise and excess noise are uncorrelated, the total spectrum density of low-frequency drain current noise is the sum of the three components (Fig 3.3):

$$S_{id-total} = S_{id-1/f} + S_{id-excess} + S_{id-white} \tag{3.7}$$

To verify the proposed low-frequency noise model, the noise measurement is conducted according to the setup shown in Fig. 3.4. The DC bias to the DUT is supplied by the Berkeley Technology Associate BTA9603 Noise Analyzer, which eliminates the residual noise in the bias voltages generated by HP4155C Semiconductor Parameter Analyzer. The noise current of the DUT is amplified by the low-noise amplifiers in BTA9603 before being applied to the Stanford Research SR780 Network Signal Analyzer (bandwidth: dc to 100 kHz) for FFT (fast Fourier transform). A computer installed with Noise Pro is used to automatically control the whole measurement.

3.3 Kink Effect Induced Excess Low-Frequency Noise

The SOI devices in this chapter were made with a 0.13μm standard CMOS process on p-type silicon substrate. Fig. 3.5 shows ours measured I_d-V_d characteristics of SOI n-MOSFETs (W/L = 10 μm/0.18 μm) with floating body and grounding body. Gate is biased at 0.9V. The kink effect is obviously observed in a floating body n-MOSFET and not in an n-MOSFET with body grounded. Due to the impact ionization current, electron-hole pairs are created at the drain end. Then, the holes go to the floating body, which induce the variation of body potential. At the kink point where the body potential sufficiently increases, threshold voltage drops and thus causes an increase of the drain current. The phenomenon in the floating body n-MOSFET consists with others results in PD SOI MOSFETs.[3.6] The excess noise is also found in floating body PD SOI MOSFET as the drain bias is above the kink voltage.

In Fig. 3.6, normalized noise power spectrum density in an n-MOSFET with body floated is measured at gate biased 0.9 V, and drain biased 0.5V、1.0V、1.2V、1.3V、1.4V、1.6V. Fig. 3.6 shows that the excess noise is not observable in the curve corresponding to the linear regime operation. As drain biases is above the kink onset voltage, the normalized noise power spectrum exhibits a plateau up to the characteristic frequency $f_c = 1/(2\pi \cdot r_{eq} c_{eq})$ before a $1/f^2$ roll-ff sets in. Furthermore, a typical Lorentzian shift to lower plateau and higher cut-off frequency is observed due to the increase of impact ionization current with the drain bias. Because the r_{eq} decreases with increasing drain voltage, a larger drain bias gives rise to a higher f_c but a smaller noise magnitude.

Additionally, Fig. 3.7 shows that normalized noise power spectrum density in an n-MOSFET with body grounded. Fig. 3.7 manifests that only flicker noise is exhibited at drain biased from linear regime to saturation regime. That is, the excess noise can be effectively eliminated, as body contact is grounded. Fig. 3.8 illustrates that the normalized drain current noise initially increases with the drain voltage and reaches a peak when the kink

point appears for a given frequency. This is when the device switches from linear operation regime to the regime around the kink point with the increase of the drain voltage.

The low-frequency noise in floating-body PD SOI MOSFETs is composed of 1/f noise and shot noise-induced excess noise. High drain bias gives rise to impact ionization current which flows through the floating-body to the source terminal. The shot noise causes fluctuation of body potential and threshold voltage, and consequently leads to excess noise in drain current. The RC network of the body in floating-body PD SOI MOSFETs amplifies and filters the shot noise, giving rise to a Lorentzian-like spectral density in noise. The noise peaks around the kink onset voltage for a given frequency. These experimental results consisted with previous mentioned noise model.

3.4 Channel Soft Breakdown Enhanced Excess Low-Frequency Noise

The gate length of this section is 0.13μm, the gate width is 10μm and the oxide thickness is 1.6nm. All devices were stressed at high constant gate voltages with the source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection was chosen to be 10μA. After breakdown, the device on-state characteristics were checked and no difference was observed. Similarly, from others' study, [3.17-3.21] the impact of the gate oxide SBD is only a noticeable increase in leakage current without degrading any on-state device performance in operation.

The breakdown position was examined by using the method given in Chapter 2.[3.22] The measurement gate bias is V_g=-1.5V and V_d=V_s=0V in the accumulation region. A significant increase of I_d/I_s+I_d in device indicates that breakdown is located at the drain edge, while the moderate change in I_d/I_s+I_d implies that SBD position is in the channel. By utilizing the aforementioned technique of examining the breakdown location, the device electrical behaviors before and after various soft breakdown modes could be characterized. In Fig. 4.9, the gate current and substrate current as a function of V_g in fresh, channel-SBD, and edge-SBD n-MOSFETs were compared.

This comparison indicates that the substrate current increased drastically in channel-SBD devices, but the change in edge-SBD devices was negligible. The substrate current at a positive gate bias is attributed to channel hole creation resulting from valence-band electron tunneling from Si substrate to the conduction band of the poly gate. The tunneling process is unlikely to occur in the n^+ drain region since the valence-band edge of the n^+ drain is aligned with the band-gap of the n^+ poly-gate. Thus, these findings support the viewpoint that the post c-SBD I_b is enhanced largely at a positive gate bias due to a localized effective oxide thinning [3.23-3.25] while I_b is nearly unchanged after e-SBD. The results provide direct experimental evidence that channel soft breakdown may induce a substrate leakage current increase in device operation, especially at a high gate bias.

According to the above results, c-SBD enhanced substrate tunneling current in PD SOI MOSFETs is proposed as a new body-charging mode.[3.11,3.26-3.27] To further illustrate this point; the low frequency drain noise spectrums of SOI nMOSFET before and after both SBD modes are shown in Fig. 3.10. The measurement drain bias is 0.1V and the gate bias is 1.2V. The pre-BD noise characteristics of 1.6 nm gate oxide nMOSFET were dominated by a 1/f-like flicker noise component without other noise component of linear kink effect.[3.28] Suitable channel engineer process can eliminate the excess floating body noise of SOI device in advanced 0.13μm generation SOI technologies.[3.8,3.10] An additional Lorentizian-like spectrum appears only when both channel soft breakdown occurs and body contact is floated. As body contact is grounded, the excess noise can be effectively eliminated. The excess noise is also not observable in e-SBD devices. It indicates that the additional body charge injection of c-SBD devices not only enhances the V_t hysteresis effect but also degrades the LF noise spectrum.

Now, we would further investigate the gate bias dependence of the c-SBD induced excess floating body noise. Fig. 3.11 shows the normalized noise spectra of a floating body c-SBD SOI nMOSFETs under different gate biases. We observed a typical Lorentzian shift to lower plateau and higher cut-off frequency due to the valance band electron current increase with the gate bias. At V_g=1.6V, only 1/f noise is observed. In fact, we believe there is still a Lorentzian in this case but shifted to lower frequency, below our measurement capability. Note that the normalized 1/f noise remains almost constant over measurement gate bias in this ohmic region. This could be associated with the number fluctuation dominated in this measurement.[3.29-3.30] The excess noise of a c-SBD SOI devices with floating body shows similar behaviors to the excess noise induced by the kink effect in section 3.3.

Fig. 3.12 illustrates that for a given frequency, the normalized drain current noise of c-SBD floating body SOI devices initially increases with V_g and reaches a peak when gate bias is 1V. This phenomenon is consistent with other research claiming that the RC network of

the body in floating-body PD SOI nMOSFET's amplifies and filters the shot noise of substrate current, giving rise to a Lorentzian-like spectral density in noise.[3.6-3.9] It can be explained that with an increase in gate voltage, c-SBD induces more substrate current as a result of valance band electron tunneling. Further increase in gate bias leads to a low amplification gain by the floating-body to the shot noise, because the equivalent substrate resistance decreases with the substrate current increase, thus the noise magnitude decreases.[3.7]

3.5 Summary

The significance of soft breakdown position to the low frequency drain current noise in floating body PD SOI nMOSFETs has been evaluated. The excess floating body noise of nMOSFETs would be enhanced if a breakdown path occurs at the channel. The enhanced noise correlates with channel soft breakdown induced large substrate current of valance band electron tunneling. This noise sources origins from the amplification by small white noise of the substrate current. The c-SBD enhanced excess noise may occur even with supply voltage less than 1.0V and would be a serious reliability concern in ultra-thin oxide analog SOI devices.

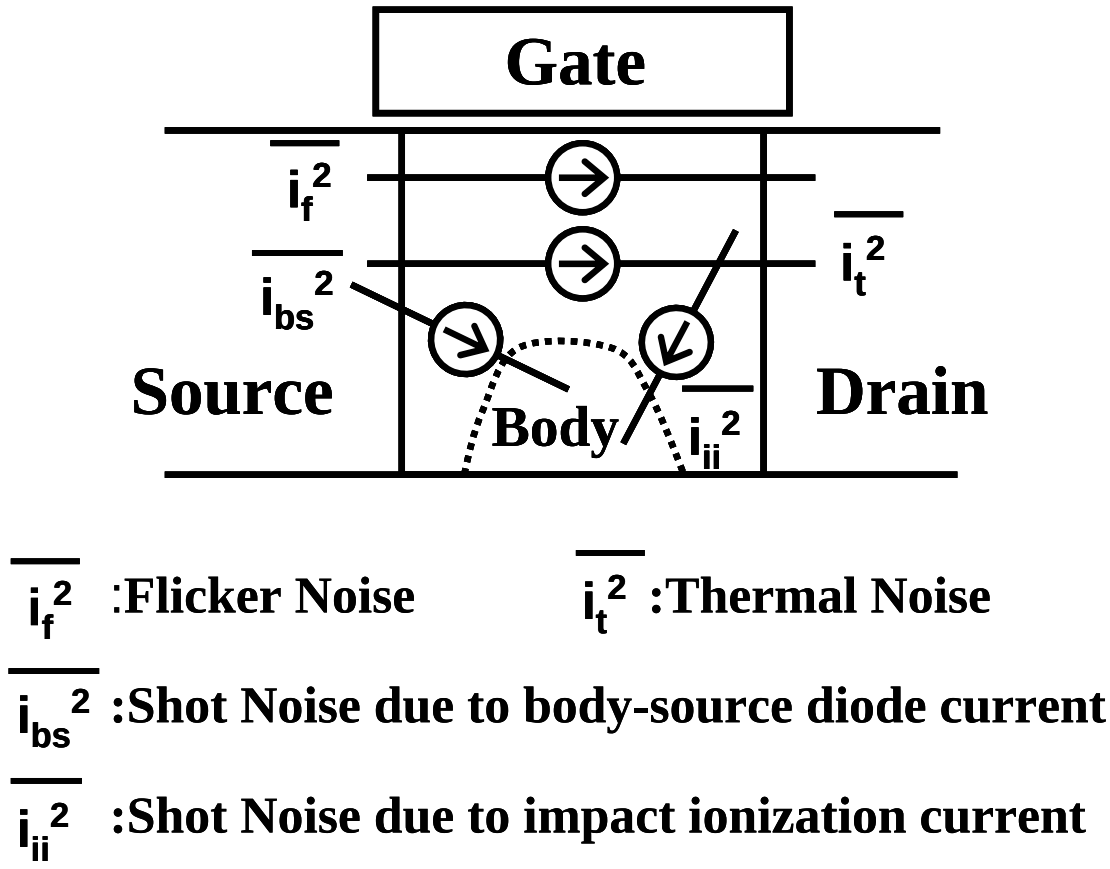

Fig.3.1 Noise sources in an SOI MOSFET.

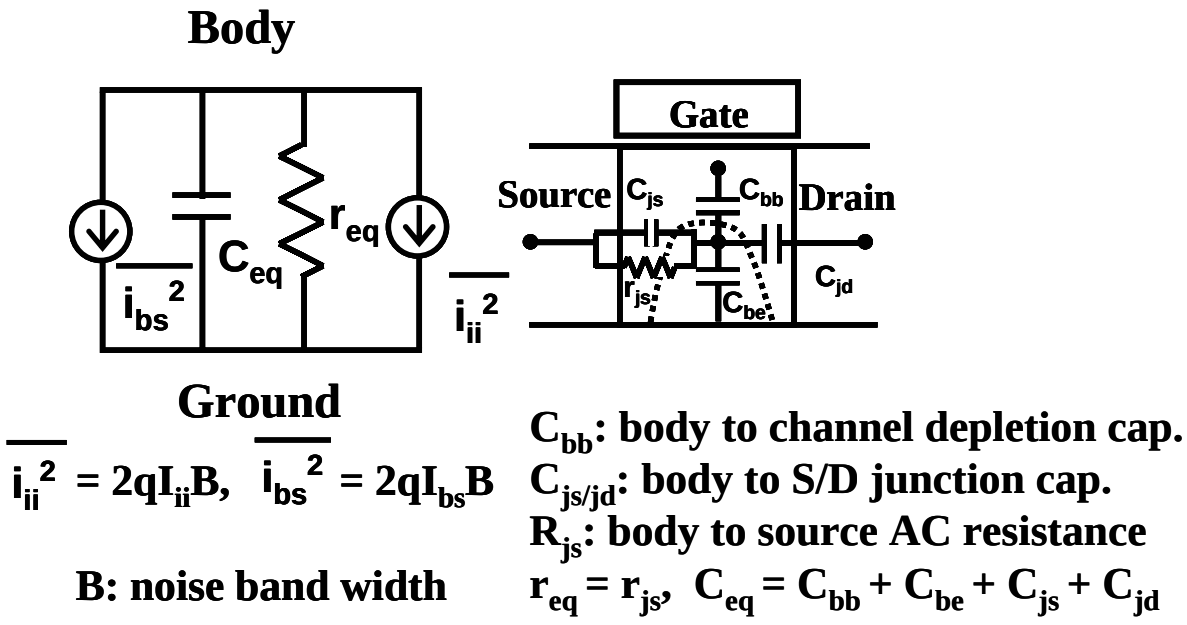

Fig.3.2 (a) Noise small-signal equivalent circuit for the floating-body and (b) schematic for the r_{eq} and C_{eq} network.

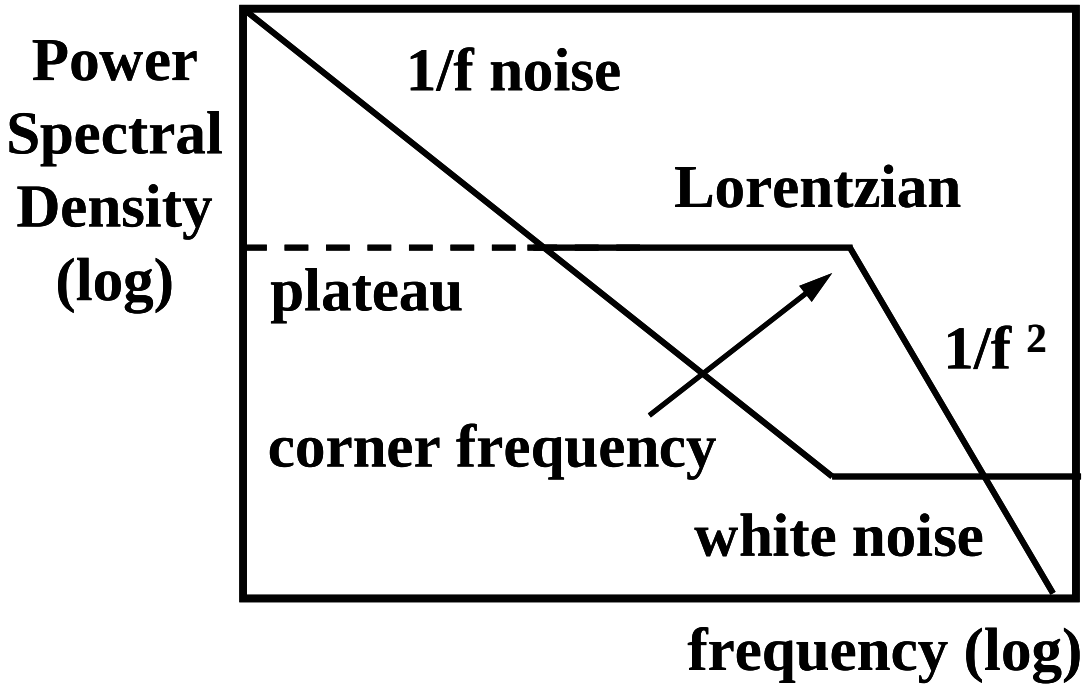

Fig.3.3 Typical input-referred low-frequency noise spectrum.

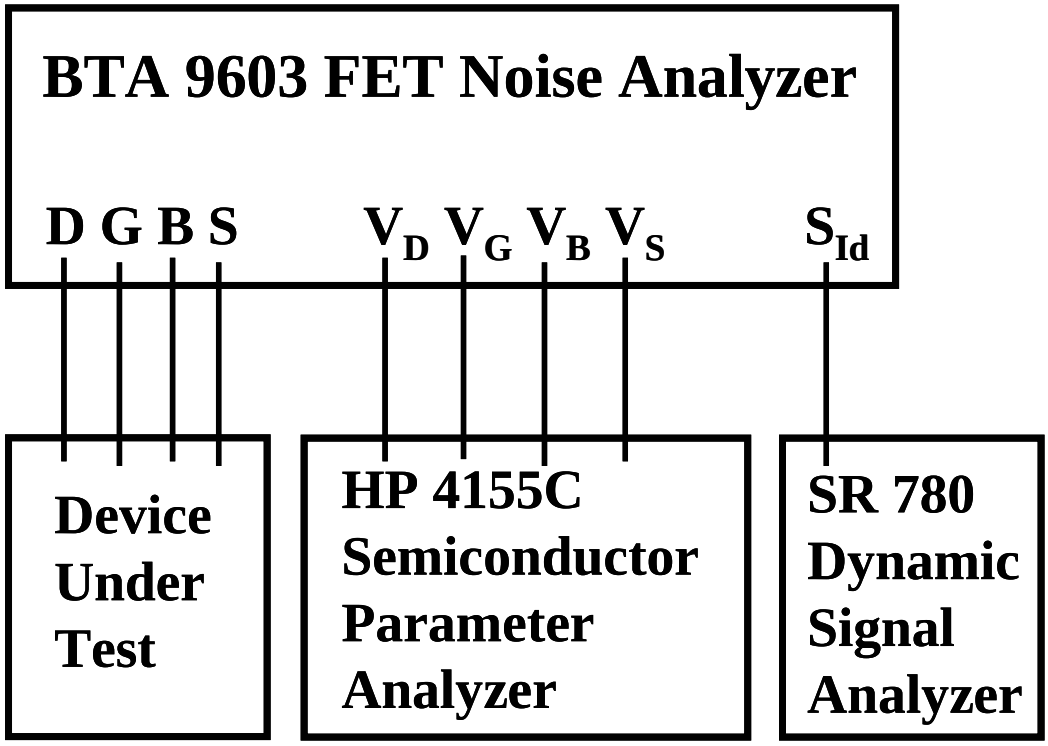

Fig.3.4 Low-frequency noise measurement setup.

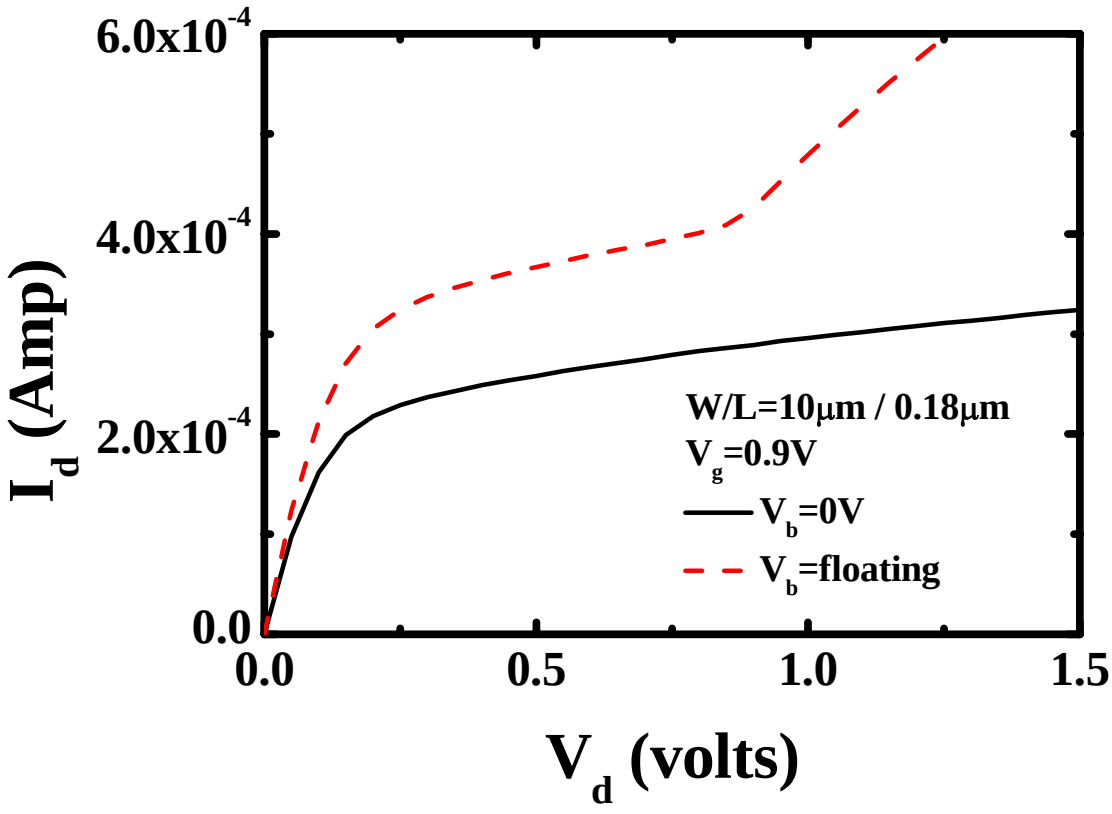

Fig.3.5 The I_d-V_d characteristics in nMOS SOI devices with floating body and grounding body when gate is biased at 0.9V.

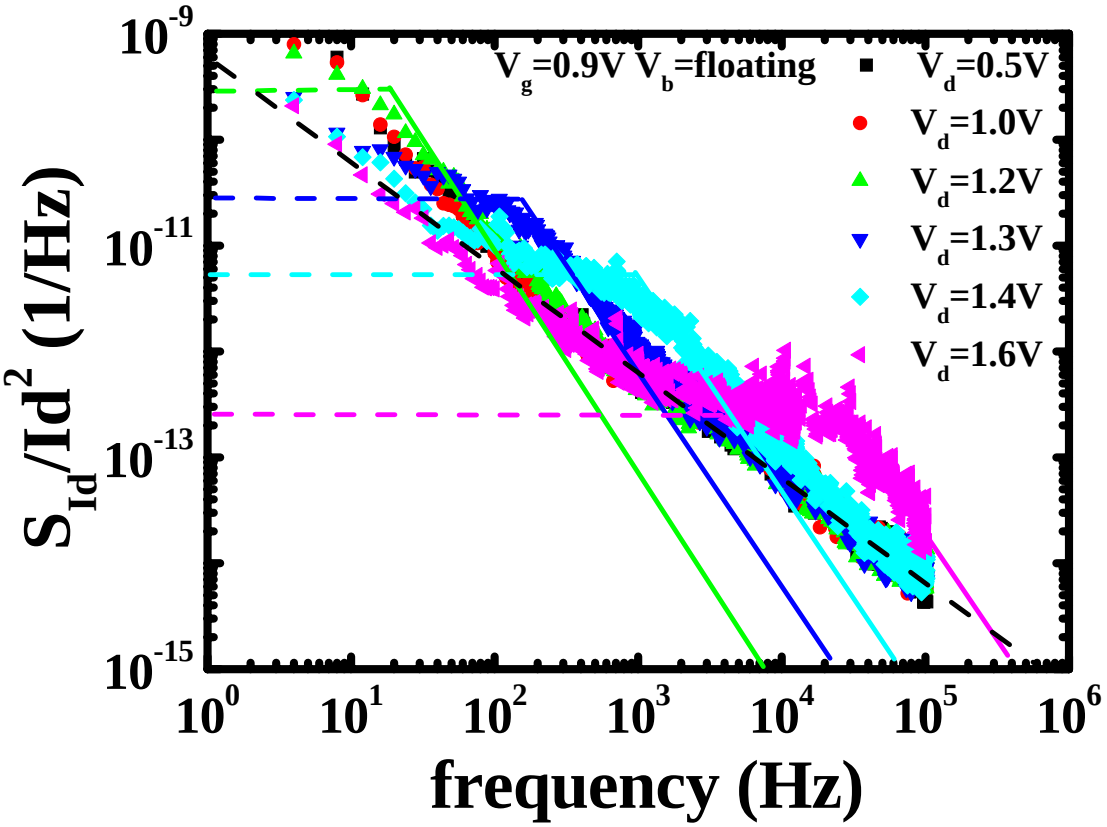

Fig.3.6 Normalization noise power spectral density in floating body nMOS SOI devices under different drain voltage when gate is biased at 0.9V.

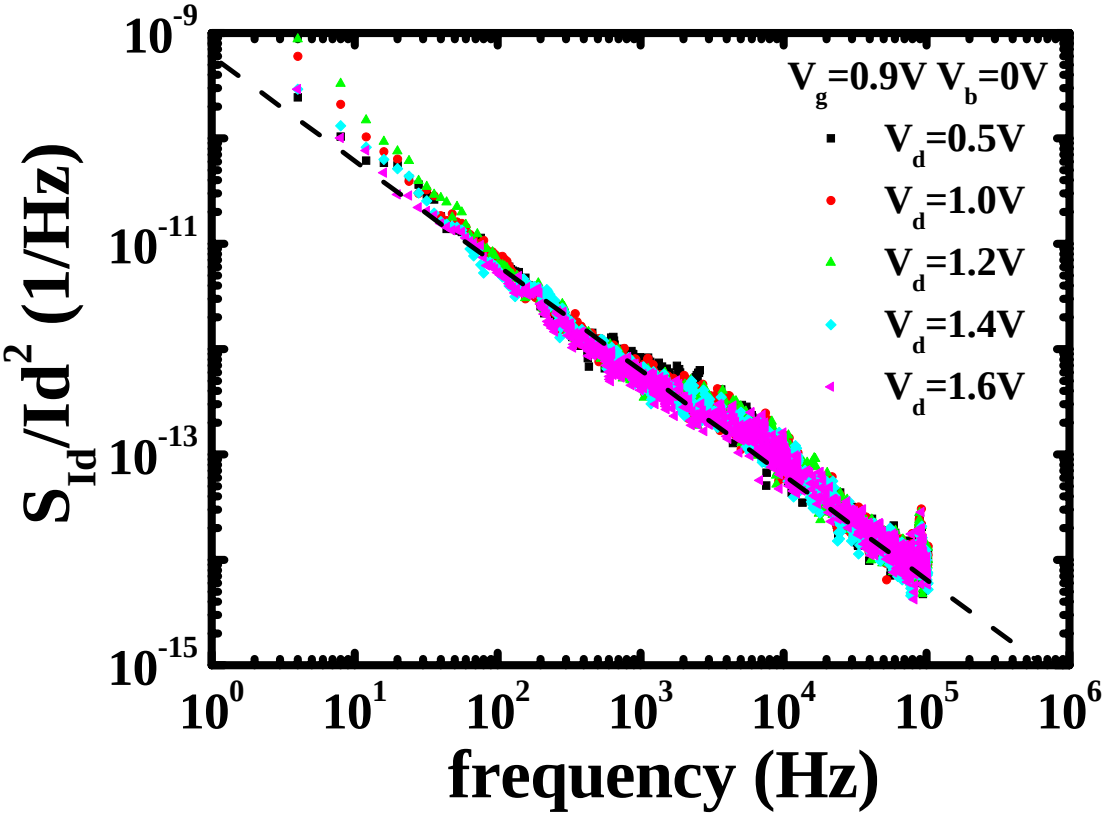

Fig.3.7 Normalization noise power spectral density in grounding body nMOS SOI devices under different drain voltage when gate is biased at 0.9V.

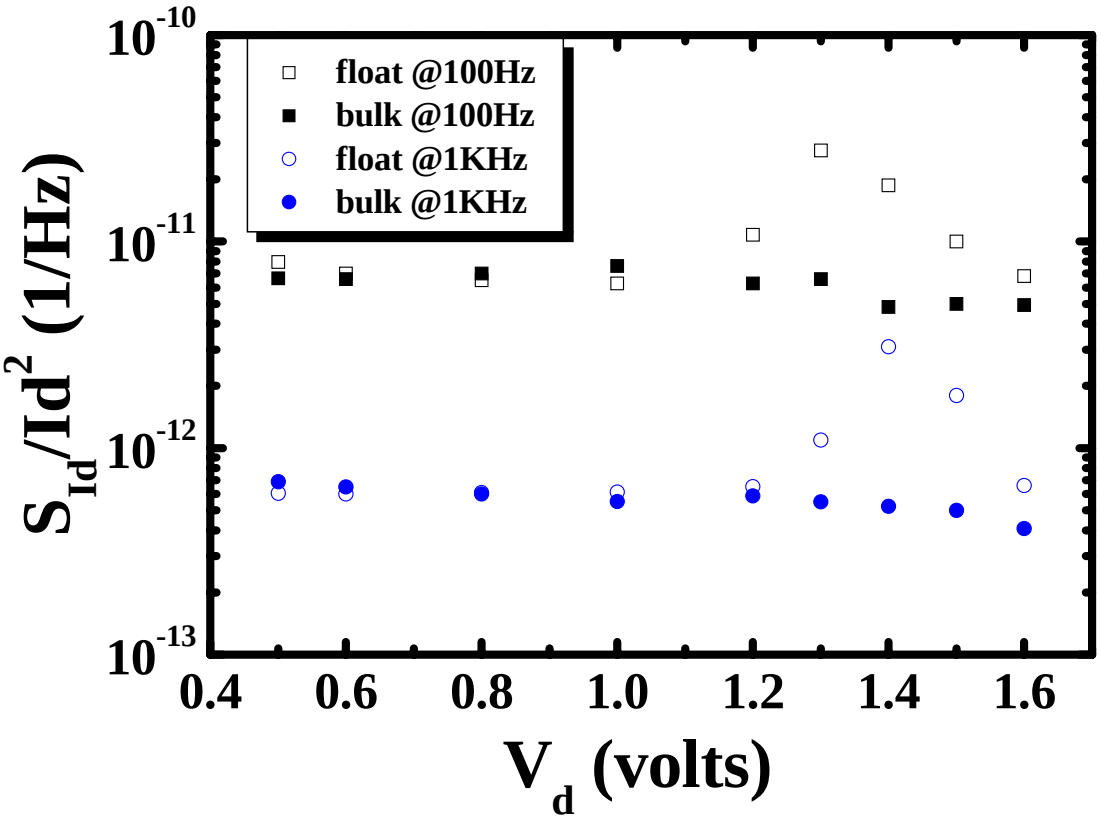

Fig.3.8 Comparison of normalization noise power spectral density under different drain bias in floating body SOI devices and grounding body SOI devices for given frequency.

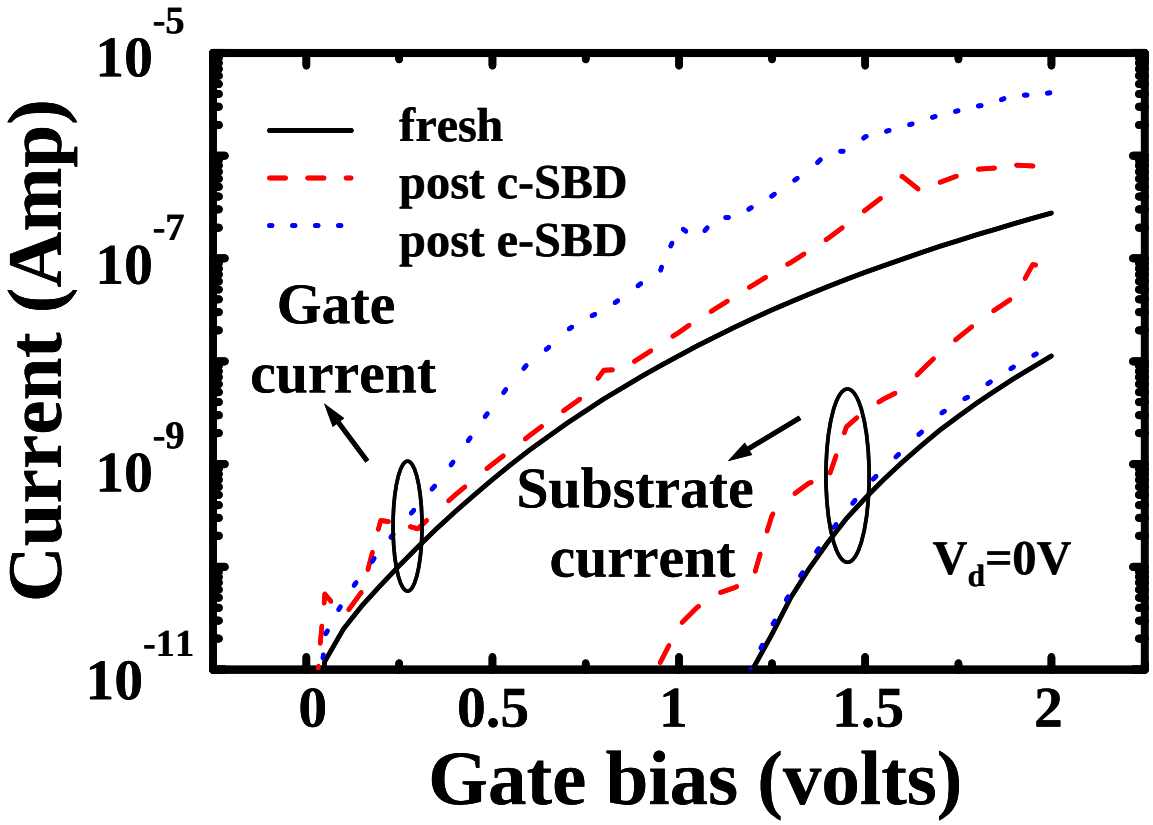

Fig.3.9 The gate current and substrate current as a function of V_g in fresh, channel SBD, and edge SBD n-MOSFETs were compared.

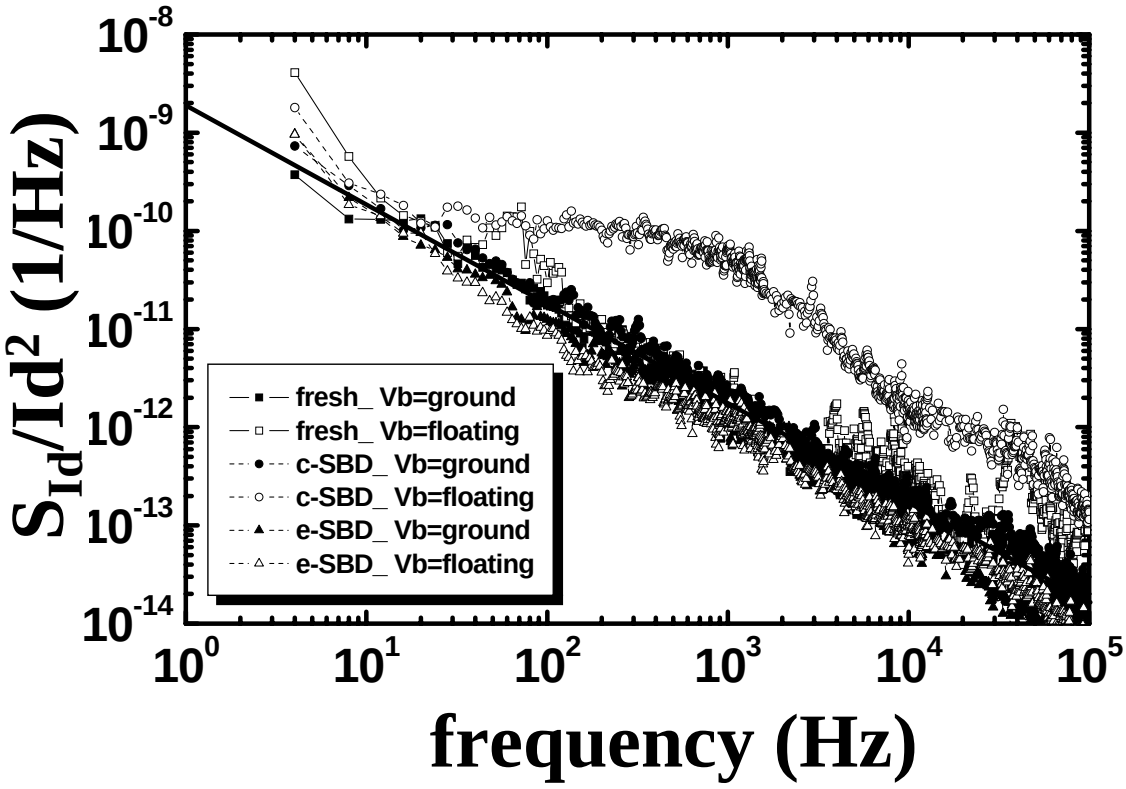

Fig.3.10 The low frequency drain noise spectrums of n-MOSFET before and after both SBD modes are shown. The measurement drain bias is 0.1V and the gate bias is 1.2V.

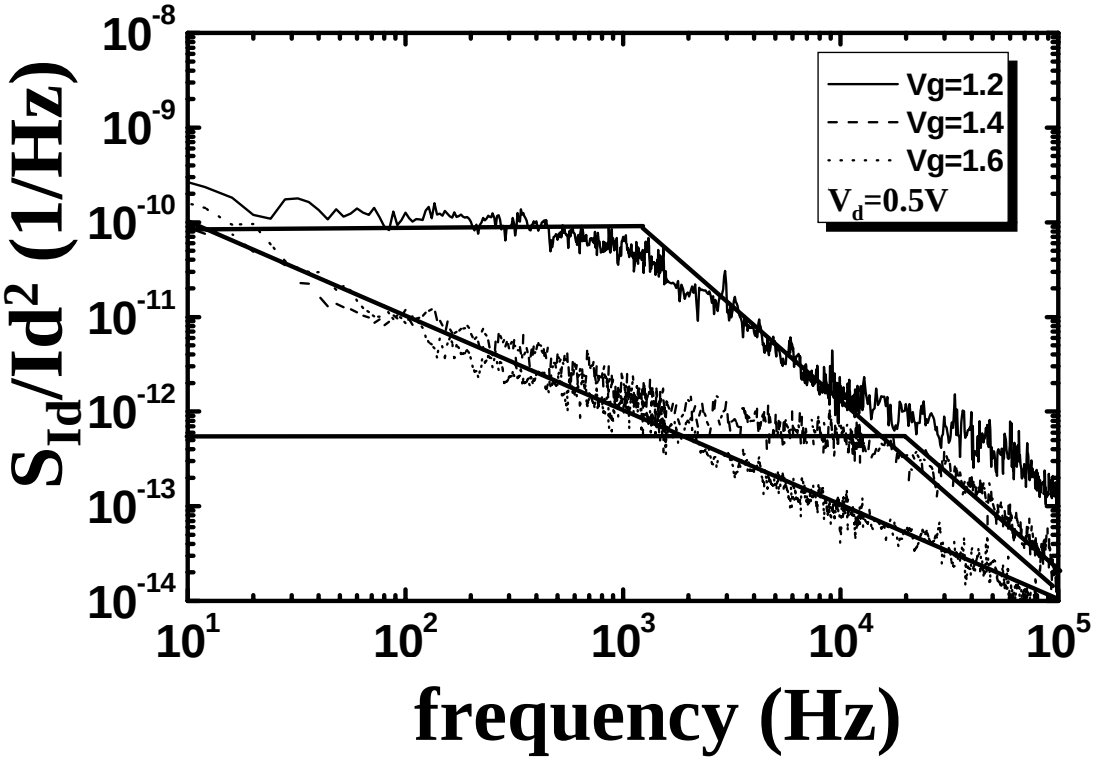

Fig.3.11 The normalized noise power spectrum of a c-SBD nMOS SOI device with floating body under different gate biases is shown.

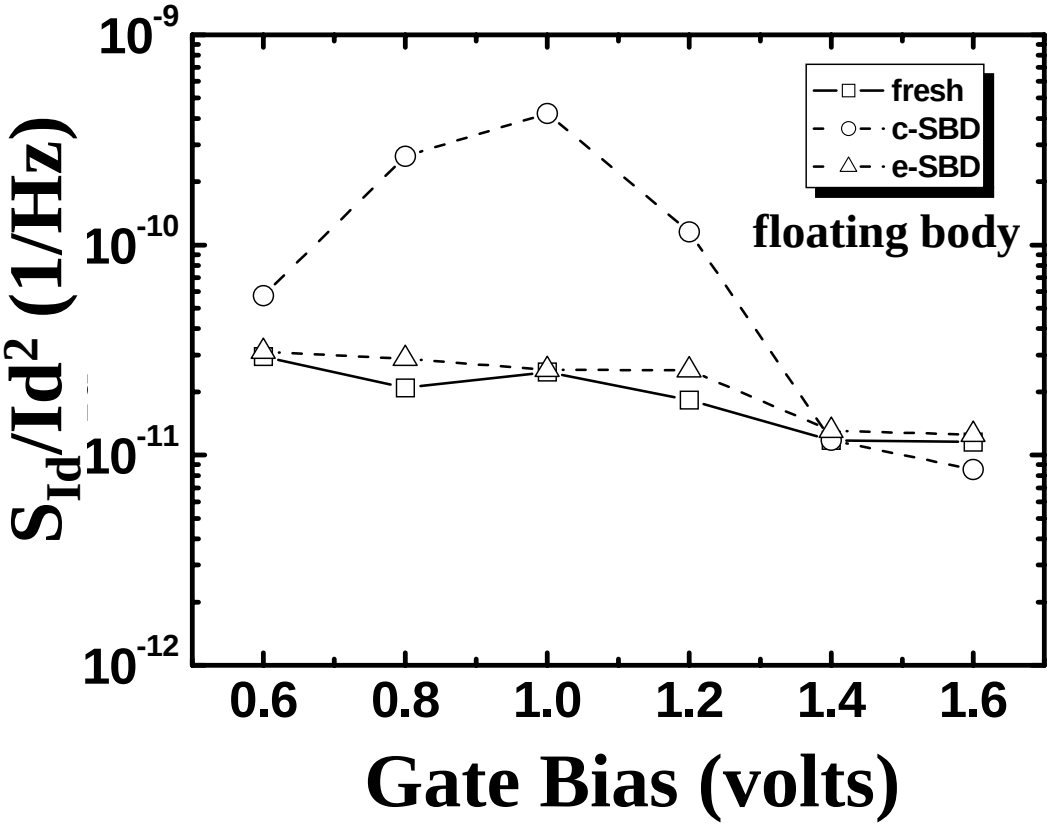

Fig.3.12 Comparison of normalization noise power spectral density with floating body under different gate bias in the fresh device, c-SBD device and e-SBD device at f=100Hz.

Chapter 4
Floating Body Accelerated Oxide Breakdown Progression in Ultra-Thin Oxide SOI p-MOSFETs

4.1 Introduction

The aggressive scaling of advanced complementary metal-oxide-semiconductor (CMOS) field effect transistors (MOSFETs) has pushed the gate oxide thickness towards its limit in terms of reliability.[4.1-4.4] In ultra-thin gate oxide MOSFETs, oxide breakdown (BD) has been shown to evolve in a continuous manner from initial stages to final shorting.[4.5-4.7] Previous study has shown that a small increase in gate leakage due to oxide BD does not disrupt circuit operation, and the failure criterion should be changed to a higher level of gate leakage.[4.8-4.9] Therefore, the oxide failure time is determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate. Presently, the silicon-on-insulator (SOI) technology has emerged to be a candidate for advanced CMOS technology for its higher performance. The BD progression in conventional bulk CMOS devices [4.10-4.12] has been widely investigated. In this chapter, we will investigate the influence of floating body effect on BD progression in partially depleted (PD) p-type SOI MOSFETs.

Several concerns of hard breakdown evolution in ultra-thin oxides have been proposed.[4.7-4.14] Monsieur et al [4.7] reported that for low gate stress bias, the defect generation rate being very low, the degradation of the BD conduction path becomes macroscopic and can last thousands of seconds even in the case of accelerated test. Linder et al [4.9] showed that the growth of BD current could be exponentially dependent on gate bias, oxide thickness, and any other parasitics, such as inversion layer resistances, altering the observed growth rate drastically. Alam et al [4.13] indicated that circuits do continue to operate after the first soft breakdown (SBD), and suggested that the standard reliability

specification is too restrictive, and should be redefined, particularly for pMOS devices. In ultra-thin oxide pMOSFETs, enhanced gate oxide BD growth rate was observed with a negative substrate bias.[4.14] Furthermore, the floating body configuration of partially depleted SOI CMOS may result in a non-zero body voltage due to various body charging mechanisms [4.15-4.18] and thus affects oxide BD evolution. The objective of this chapter is therefore to investigate floating body effect on BD progression rate. A model based on breakdown induced channel carrier heating will be proposed to explain the observed phenomenon.

4.2 Devices and Experiment

The devices in this work were made with an optimized 0.13μm CMOS process on p-type SOI wafer and have a gate length of 0.5μm, a gate width of 2μm and an oxide thickness of 1.6nm. The gate oxide was grown with rapid plasma nitridation (RPN) process. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this chapter, all devices were stressed at constant gate voltage with the source and drain grounded. Fig. 4.1 shows typical BD evolution in a 1.4nm oxide and a 2.5nm oxide bulk pMOSFETs. In the 1.4nm gate oxide pMOSFET, oxide BD is evolved in a progressive way, and the gate leakage current increases gradually with stress time. As a contrast, the 2.5nm oxide pMOSFET exhibits an abrupt jump in gate leakage current after BD. Since a slight gate leakage increase due to oxide BD is considered to be nondestructive for circuit operation [4.8], we define oxide breakdown time (t_{BD}) and device fail time (t_{fail}) as the time when the gate leakage current reaches 1.5 times and 15 times its pre-stress value, respectively.

4.3 Result and Discussion

4.3.1 A Shorter t_{fail} in SOI pMOSFETs

Fig. 4.2 shows the gate leakage current evolution with stress time at a stress gate voltage of V_g=-2.9V for various applied substrate biases (V_b) in pMOSFETs. The oxide t_{BD} is almost the same for different substrate biases. This can be understood because oxide defect generation rate is dependent on injected charge energy and fluence during stress [4.19-4.22], regardless of applied substrate bias. After the onset of BD, the BD growth rate exhibits an apparent dependence on substrate bias. A forward substrate bias can significantly enhance BD growth rate. It should be noted that the SOI device with floating body configuration has the worst BD progression rate in Fig. 4.2. The statistic Weibull distributions of oxide t_{BD} and t_{fail} for SOI (floating substrate) and bulk (grounding substrate) pMOSFETs are plotted in Fig. 4.3. Although the floating substrate configuration does not affect t_{BD}, it does cause a 2 times shorter t_{fail} than in bulk pMOSFETs.

4.3.2 Mechanism of Enhanced BD Progression in SOI

The floating body configuration of SOI devices may result in a small forward body voltage due to various body charging processes. In an ultra-thin oxide pMOSFET, the gate stress current may have comparable electron and hole components at a negative gate bias. To analyze the polarity of dominant stress current in a pMOSFET, a charge separation technique is utilized to measure electron stress current and hole stress current. The inset of Fig. 4.4 illustrates the carrier flow at a negative gate bias, I_b denotes electron current and comes from valance-band electron tunneling from the gate electrode. I_{sd} stands for hole tunneling current from the inverted channel. The substrate bias dependence of electron current and hole current before and after t_{BD} is shown in Fig. 4.4. Note that the electron and hole currents in a fresh device are independent of substrate bias. Interestingly, the post-t_{BD} hole current, unlike the pre-BD I_b and I_{sd}, exhibits a significant V_b dependence. Furthermore, Fig. 4.5 reveals that the

V_b dependence of the post-t_{BD} hole current increases with BD evolution. Since the hole stress current dominates gate stress during BD evolution and increases with a forward body bias, the enhanced BD progression in a floating body configuration can be understood.

4.3.3 BD Caused Carrier Heating

Since the post-t_{BD} electron current does not exhibit V_b dependence (Fig. 4.4), the possibility that the V_b dependence of the post-t_{BD} hole current is caused by the variation of effective gate-to-channel voltage resulting from V_b modulated channel resistance can be excluded. Otherwise, the post-t_{BD} I_b should have the same V_b effect as the post-t_{BD} I_{sd}. Moreover, substrate impact ionization and negative bias-temperature instability effects are also excluded because the trend of the V_b dependence is opposite.

To further investigate the origin of the V_b dependence of the post-t_{BD} hole current, we measured the spectral distribution of hot carrier light emission before and after t_{BD} (Fig. 4.6). The light intensity is greatly increased after oxide BD. The high-energy tail of the post-t_{BD} spectral distribution indicates the rise of the carrier temperature. Similar finding was also reported by other groups.[4.23] The extracted carrier temperature from the high-energy tail of the spectrum is around 1300^{o} K (Fig. 4.6(b)). There are two possible theories to explain the rise of channel carrier temperature at a BD spot. First, based on the model proposed by Rasras et al [4.23], the gate voltage may penetrate into the substrate after BD and causes lateral field heating of channel carriers. However, this process is unlikely here since the post-t_{BD} electron current and hole current have distinctly different V_b dependence. The second possible reason is that high-dissipated energy, released by valence electrons tunneling from the gate through the BD path, will locally produce a rise of hole temperature. A temperature range of 1000^{o} K to 2000^{o} K was estimated in Ref. [4.24]. Electron-hole scattering or Auger recombination is suspected to be the responsible energy transfer process.

To show that the rise of hole temperature may account for the observed V_b dependence,

we calculate the hole tunneling current with hole temperature at 300^{o}K and 1300^{o}K. In our calculation, we solve the coupled Poisson and Schrodinger equations to obtain the sub-band structure for the inversion holes (Fig. 4.7). A simple one-band effective mass approximation is used for simplicity. The hole tunneling current density is calculated according to the Tsu-Esaki formula [4.25]

$$J_{sd} = qm^{*}_{//}(\frac{1}{2\pi^{2}\hbar^{3}})k_{B}T\sum_{n} D_{n}\{\ln(1+\exp((E_{n}-E_{f})/k_{B}T))) - \ln(1+\exp((E_{n}-E_{f'})/k_{B}T)))\} \quad (4\text{-}1)$$

where E_f ($E_{f'}$) denotes the Fermi energy in the channel (poly gate) and D_n is the hole tunneling probability of the n-th sub-band. m^{*} is the hole effective mass in Si. Other variables have their usual definitions. It should be emphasized that it is not our intention to consider detailed trap-assisted charge transport in the BD path. It is also not our intension to calculate the precise current value before and after oxide BD, since the BD area and BD caused effective oxide thinning cannot be easily determined. Instead, our purpose is to investigate the effect of hole temperature on the inversion hole distribution in different sub-bands and the corresponding substrate bias effect on hole tunneling current. Therefore, a simple WKB formula for direct tunneling is employed for D_n.

Our result in Fig. 4.8 clearly shows that the hole tunneling current exhibits a larger V_b dependence at 1300 ^{o} K. The simulation can well interpret the measured V_b dependence of the post-t_{BD} I_{sd} by simply using an elevated hole temperature. The trend in Fig. 4.8 is similar to the measured V_b dependence in Fig. 4.5. To explain the temperature effect on the V_b dependence in more detail, the distribution of inversion holes in the lowest three sub-bands is given in Table. 4.1. At T=300 ^{o} K, channel holes mostly reside in the first sub-band no matter of V_b. At T=1300 ^{o} K, a large part of holes are thermally excited to higher sub-bands at a

forward body voltage (-0.5V), where the oxide tunneling probability is larger. Thus, a much larger hole tunneling current is obtained at negative body voltages.

4.4 The Impact of Gate Stress Bias

From previous discussion, the V_b dependence of hole stress current was identified to be the origin of the floating-body enhanced BD progression. Now, the impact of gate stress bias scaling on the enhanced BD progression is explored. Fig. 4.9 shows the V_b dependence of BD current at various measurement gate biases. The V_b dependence is more distinguished at a smaller gate bias. Fig. 4.10 shows the range of the gate stress bias where hole current is dominant. The hole current dominates gate stress at small gate biases (less than ~3.0V) and the hole component of the stress current increases during BD evolution. This result is consistent with the findings in Fig. 4.9 that a large V_b dependence of the post-BD stress current is obtained at smaller gate voltages. Fig. 4.11 compares the 63% time-to-failure in SOI and bulk pMOSFETs at various gate stress biases. Accelerated BD progression is noticed in SOI samples and the trend becomes more apparent at lower gate stress biases. Fig. 4.12 shows the range of oxide thickness and stress gate voltage where the hole current component is dominant in a fresh device and after breakdown. For example, for an oxide thickness of 1.6nm, hole current is dominant in stress for V_g<2.5V in a fresh device and for V_g <3.0V after BD. High-energy electron impact ionization does not need to be considered until V_g is above 3.5V. Fig. 4.12 also reveals that the hole current dominant region increases not only with BD progression but with decreasing oxide thickness. It implies that the floating body enhanced BD progression will become more significant as oxide thickness scales down.

4.5 Summary

In ultra-thin oxide SOI pMOSFETs, breakdown progression is aggravated by a forward body bias. An enhanced post-t_{BD} gate current is observed in SOI devices due to the charging of the floating body. Numerical analysis shows that the V_b enhanced hole stress current can be explained by the increase of hole temperature at the breakdown spot. The V_b accelerated BD progression is more significant at a lower stress gate bias and for a thinner oxide.

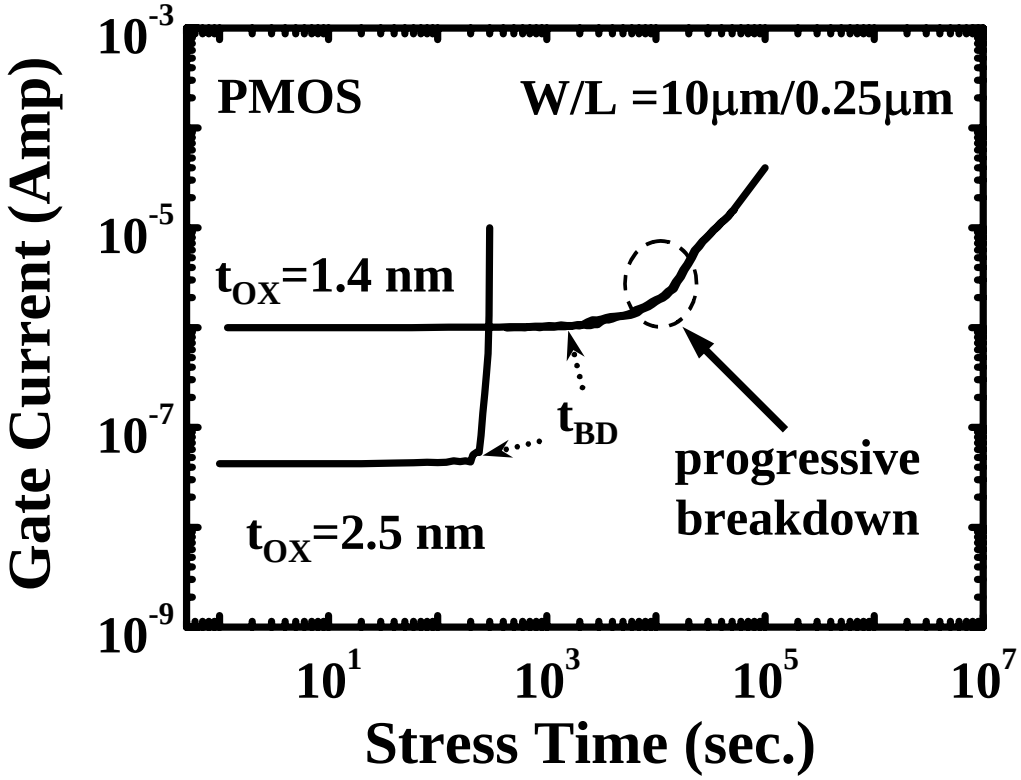

Fig.4.1 Comparsion of breakdown behavior in a 1.4nm oxide pMOSFETand in a 2.5nm oxide pMOSFET. The stress gate voltage is –3V for the 1.4nm oxide and –4.5V for the 2.5nm oxide. t_{BD} denotes the onset time of oxide breakdown.

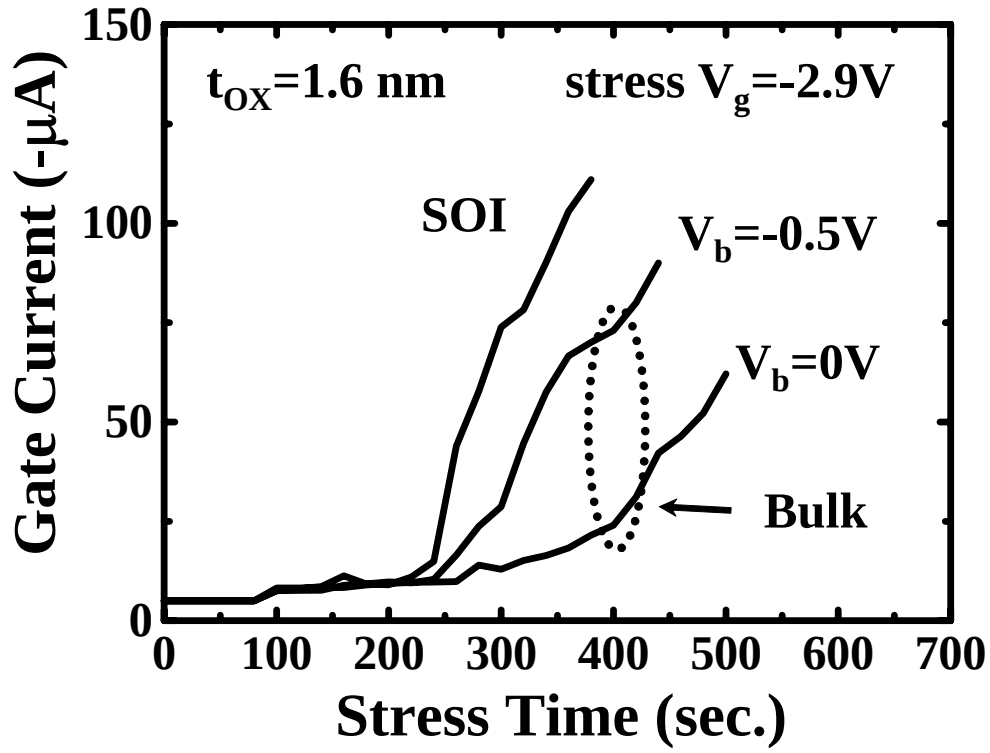

Fig.4.2 Oxide breakdown progression in bulk and SOI pMOSFETs. The stress gate bias is –2.9V and temperature is 125^{o} C.

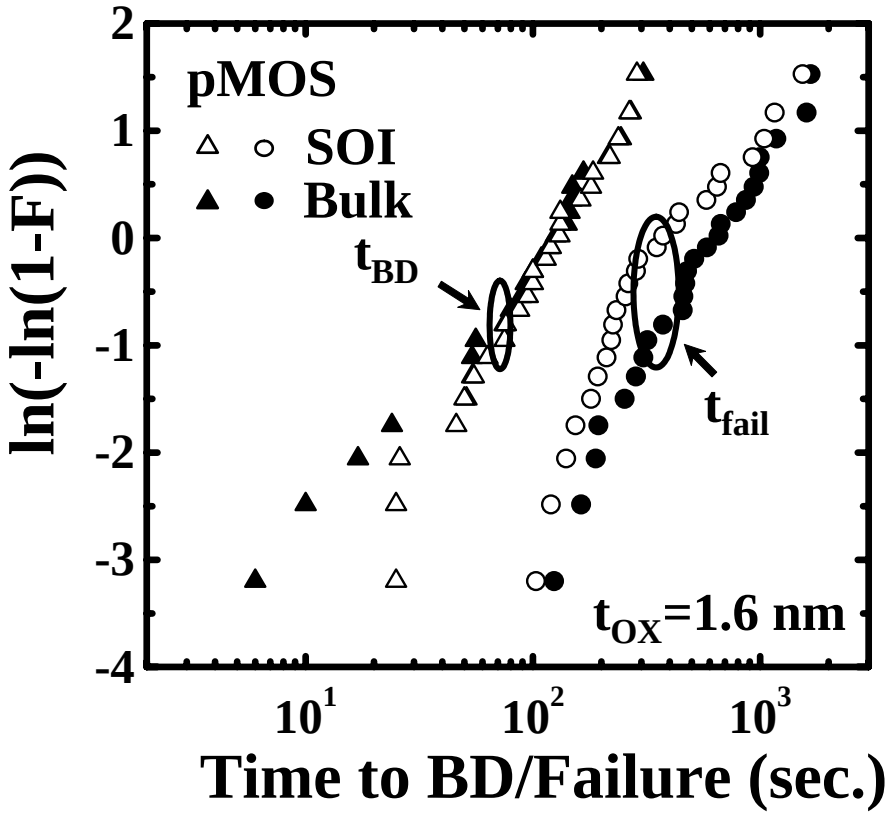

Fig.4.3 The Weibull plots of t_{BD} and t_{fail} distribution for 1.6nm oxide SOI and bulk pMOSFETs. The stress gate bias is –2.9V and the temperature is 125^{o}C. t_{BD} and t_{fail} are defined as the time for gate current to reach 1.5 times and 15 times its pre-stress value, respectively.

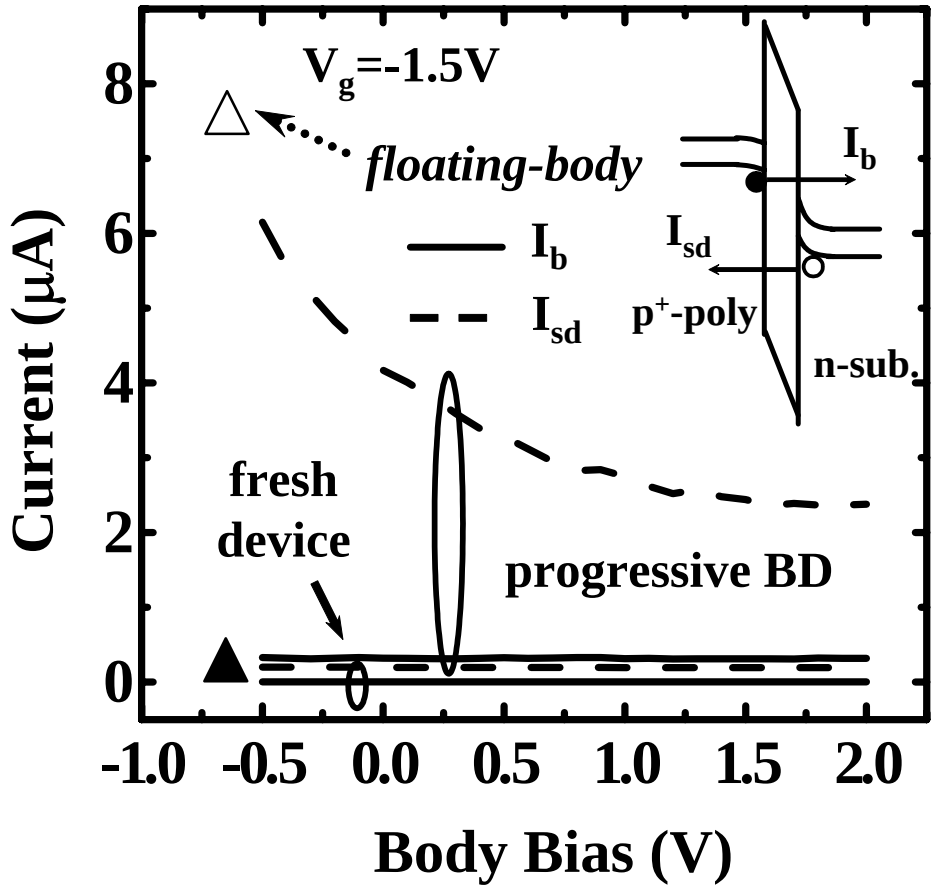

Fig.4.4 The V_b dependence of pre-BD and post-BD electron currents (I_b) and hole currents (I_{sd}) at V_g=-1.5V. Distinct V_b dependence of the post-t_{BD} I_{sd} is noted. The floating body configuration corresponds to a body voltage of approximately -0.65V. The inset illustrates carrier flow in a pMOSFET at a negative gate bias.

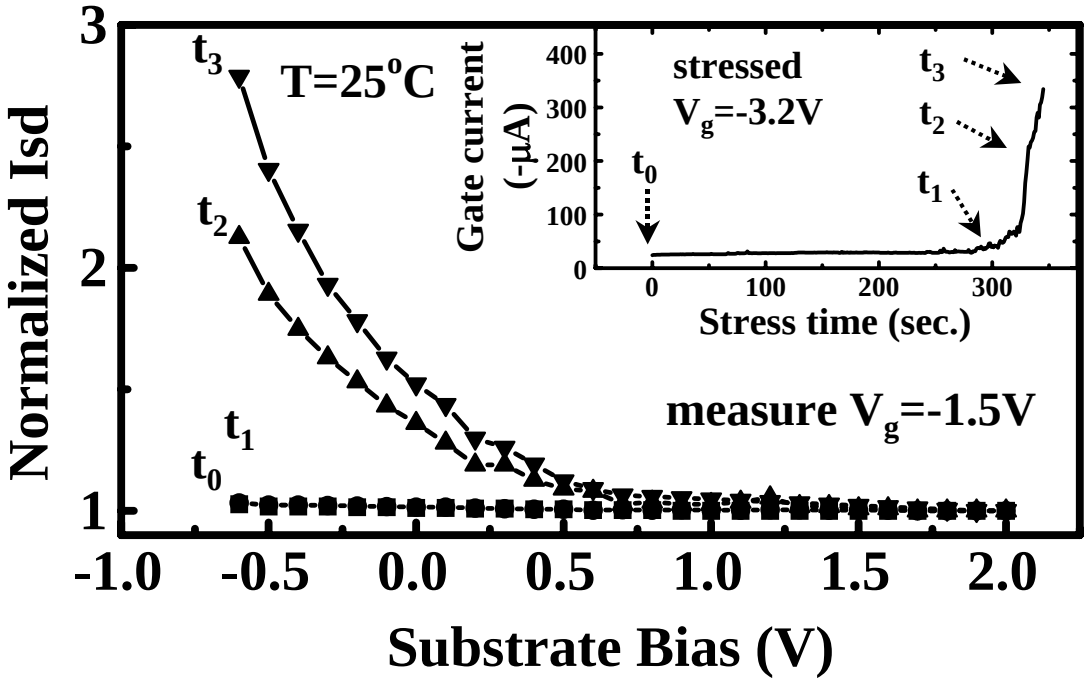

Fig.4.5 The V_b dependence of the hole current I_{sd} at different stress times, t_0, t_1, t_2 and t_3. I_{sd} is normalized to its value at V_b=2V. Gate current vs. stress time in a stress condition of V_g=-3.2V and T=25° C is shown in the inset.

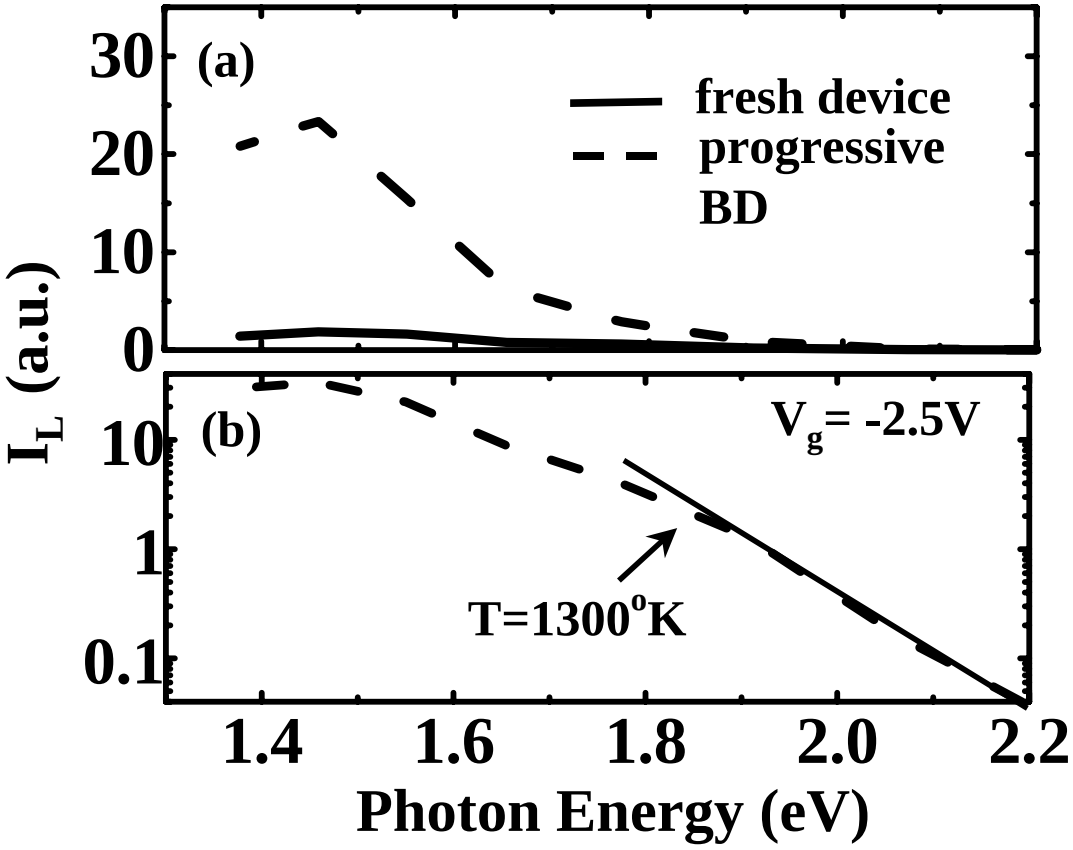

Fig.4.6 Spectral distribution of light emission in a 1.4nm oxide pMOSFET at V_g=-2.5V. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 ^{o} K.

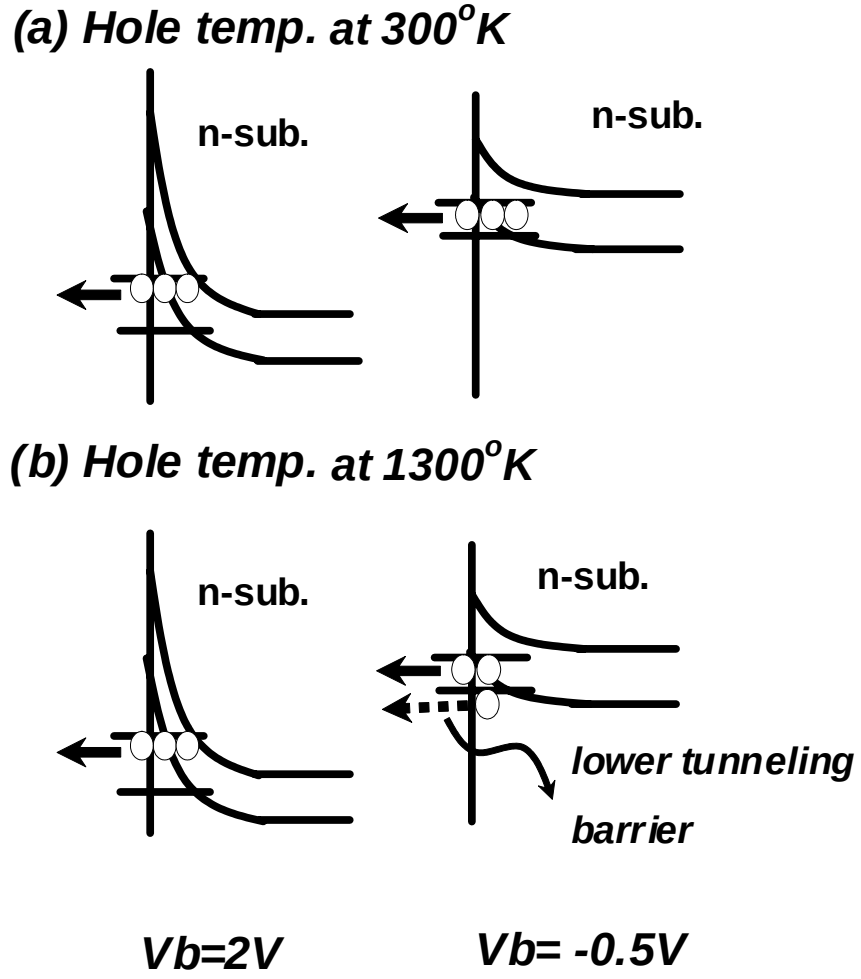

Fig.4.7 Illustration of hole distribution in sub-bands at a hole temperature of 300 ^{o} K and 1300 ^{o} K. Higher carrier temperature results in a larger V_b effect.

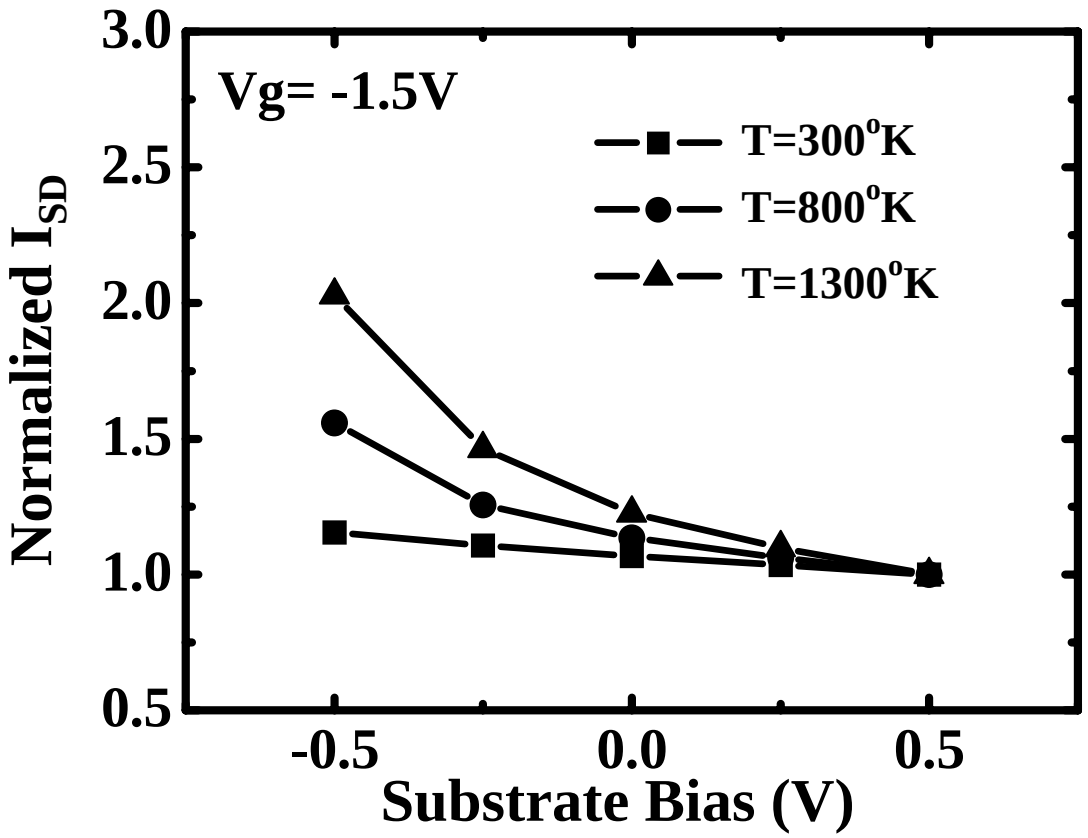

Fig.4.8 Simulated substrate bias effect on hole tunneling current in a 1.6nm oxide pMOSFET. I_{sd} is normalized to its value at V_b=2V. Simulated V_g=-1.5V.

cond. / sub-band	channel hole dist. (%)			
	300°K		**1300°K**	
	V_b=-0.5	V_b=2	V_b=-0.5	V_b=2
1st	96.6%	99.5%	39.8%	99.4%
2nd	3%	0.5%	18%	0.6%
3rd	0.3%	0%	11.6%	0%

Table 4.1 Calculated distributions of channel holes in the lowest three sub-bands. The gate bias in simulation is –1.5V. The parameters used in simulation is m*(Si) = $0.67m_0$, m*(SiO_2) = $0.55m_0$, ϕ_h (hole barrier height at SiO_2 interface) = 4.25eV, t_{ox} = 1.6nm, and N_B (substrate doping) = $1x10^{18}cm^{-3}$.

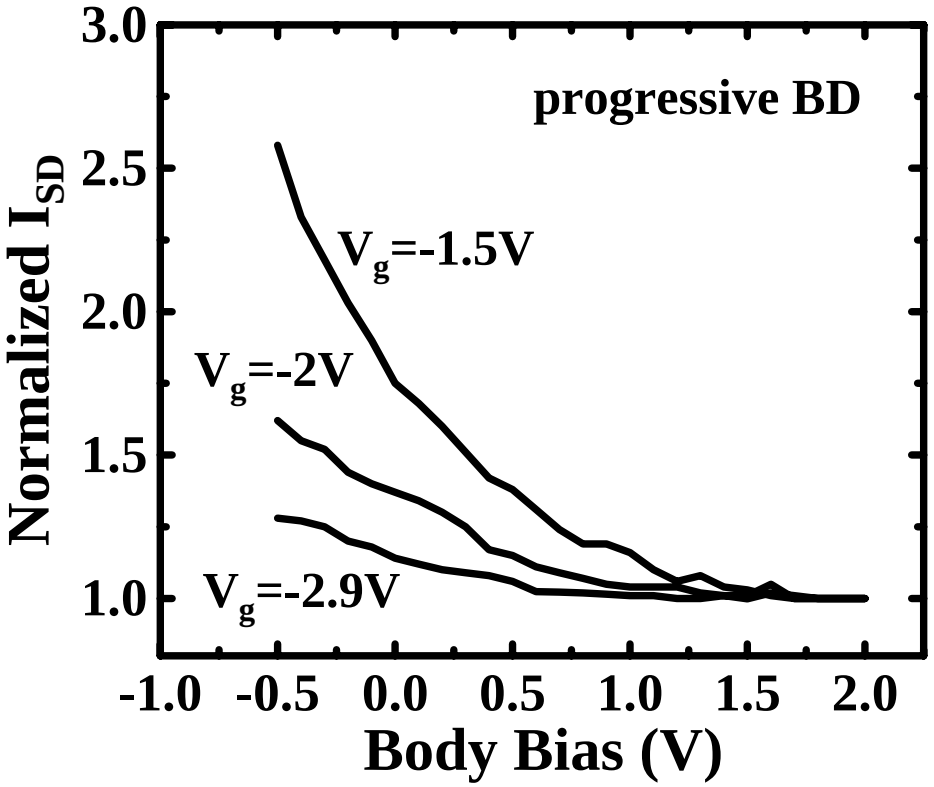

Fig.4.9 Substrate bias dependence of the post-BD hole current at various gate biases. I_{sd} is normalized to its value at V_b=2V.

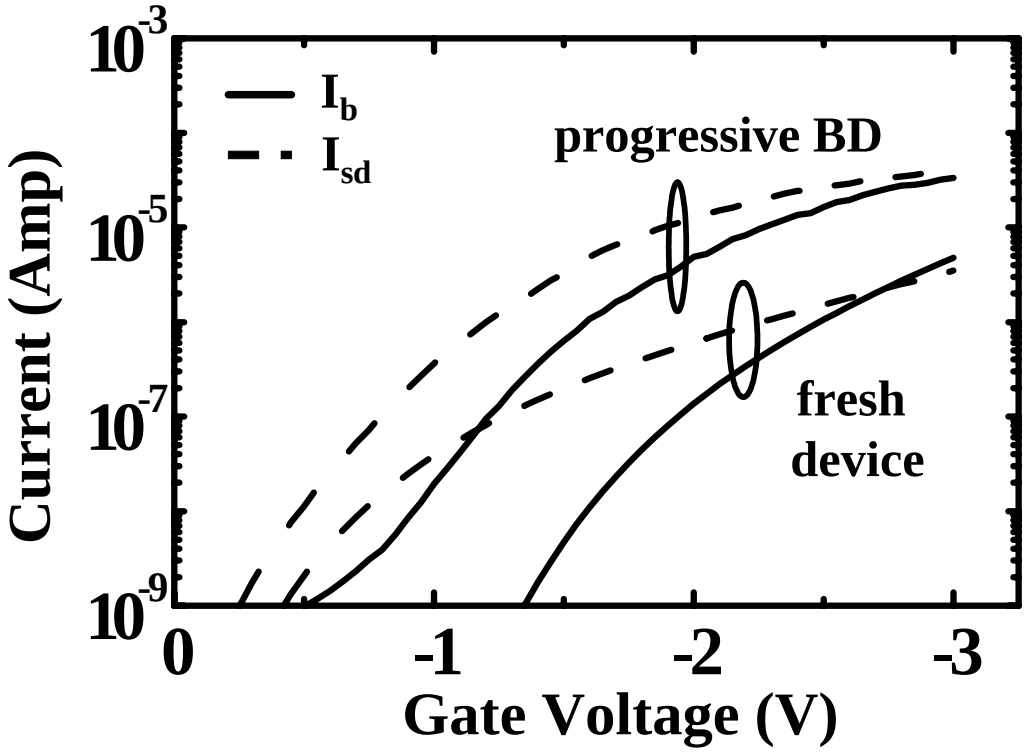

Fig.4.10 Gate bias dependence of electron current and hole current in a fresh pMOSFET and during progressive BD.

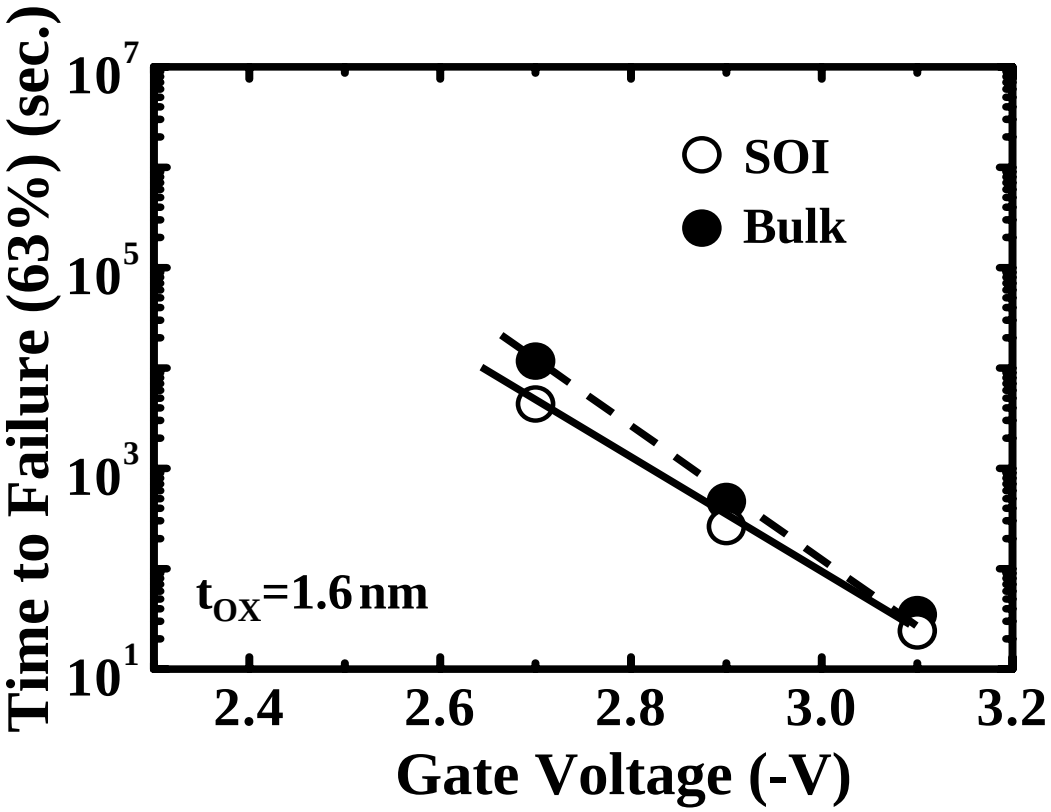

Fig.4.11 t_{fail} (63%) vs. gate stress bias for SOI and bulk pMOS devices.

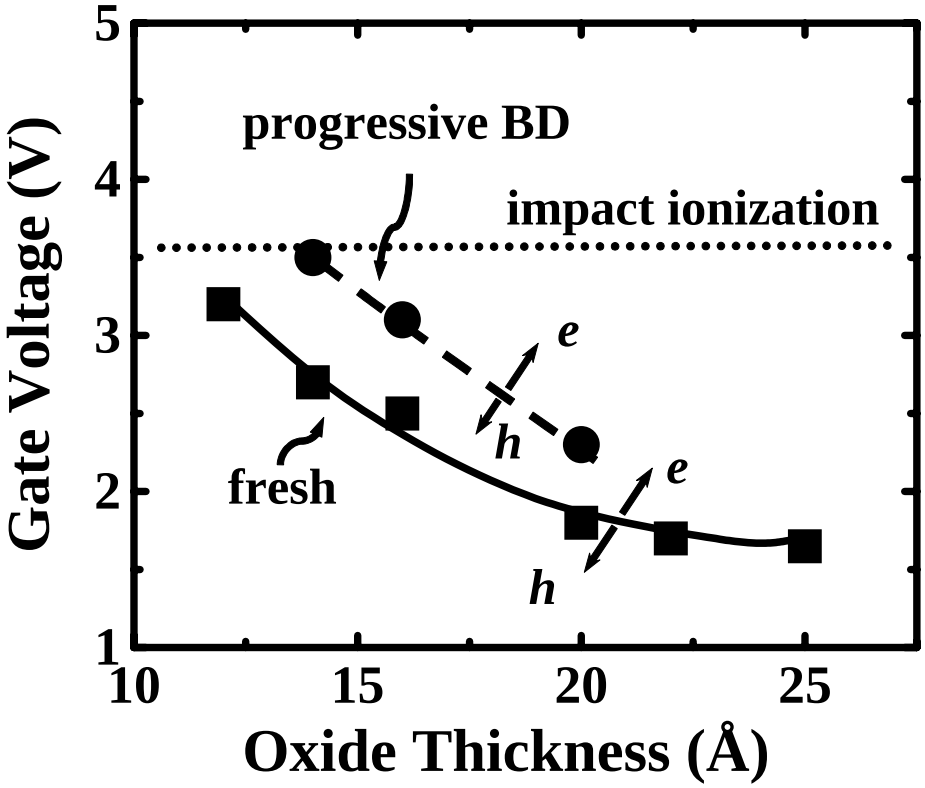

Fig.4.12 The range of oxide thickness and stress gate voltage where the hole current component is dominant in a fresh device and after breakdown. *h* or *e* represents hole current or electron current dominant regime, respectively.

Chapter 5
Conclusions

In short, this dissertation has discussed major SBD induced reliability issues in SOI CMOS with gate oxide in direct tunneling domain, among them the V_t hysteresis effects, excess low frequency noise, and breakdown hardness. Major contributions of each subject in this work are summarized as follows.

First, we have calculated the gate tunneling leakage current in ultra-thin oxide MOSFETs. Two charge transport modes attributed to gate tunneling current is proposed. The gate tunneling current includes both source/drain tunneling current and substrate tunneling current. A quantum charge transport mechanism is developed to study the I_{sd} of the inversed carrier tunneling processes, and a classical charge transport mechanism is built to explore the I_b of the valance band electron tunneling processes. In addition, the combined Poisson and Schrodinger equations are solved self-consistently to simulate the accurate oxide electric field. The C-V curve of ultra-thin gate oxide capacitance also can be calculated from the simulated results. The measured C-V and I-V of ultra-thin oxide can be fitted well by our proposed models.

Next, we reported the impact of breakdown position on hysteresis effects for ultra-thin oxide PD SOI MOSFETs. The excess substrate tunneling current of SBD PD SOI devices will modulate the substrate bias in specific operation conditions. As input signal is switching, the hysteresis effect of c-SBD PD SOI devices is enhanced. The dominant floating-body charging mechanism is valance band tunneling due to applied gate voltage. While output signal is changing, the hysteresis effect of e-SBD PD SOI devices is aggravated. The dominant floating-body charging mechanism is band-to-band tunneling when drain bias is large. Two SBD enhanced hysteresis modes in off-state CMOS have been evaluated and would be a serious reliability concern in ultra-thin oxide PD SOI circuits.

Then, the significance of soft breakdown position to the low frequency drain current noise in PD SOI nMOS devices has been identified. In high gate bias, the excess floating body noise would be enhanced if a breakdown path occurs at the channel. Large substrate leakage current of valance band electron tunneling in c-SBD not only affects the V_t hysteresis effect but also generates excess low frequency drain current noise source. This noise source correlates with the amplification by small white noise of substrate tunneling currents. The c-SBD enhanced excess noise would become an important reliability subject in ultra-thin oxide analog SOI devices.

Finally, in ultra-thin oxide pMOS, hole current instead of electron current is found to dominate breakdown progression. Enhanced breakdown hardness is observed with floating body. The enhanced breakdown evolution can be explained by the heating of channel holes and thus increased hole stress current during breakdown progression. The temperature rise of channel holes after oxide breakdown is caused by the valance electron tunneling through the BD path and the following electron-hole energy transfer process. Higher carrier temperature can produce a larger substrate bias effect on hole tunneling current by thermal excitation of holes into higher sub-bands. Numerical analysis of substrate bias effect on hole tunneling current is performed to support the proposed theory. The floating-body enhanced BD progression has large impact on the failure time of ultra-thin oxide SOI pMOS devices. All of these findings make SBD not just increase the tunneling leakage current but become a challenge of reliability issues in ultra-thin oxide PD SOI MOSFETs.

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Publication List

本計畫研究成果發表論文共八篇：國際會議三篇，期刊論文三篇，以及兩本博士論文。其中兩度於半導體可靠性物理領域權威會議的國際可靠性物理年會（International Reliability Physics Symposium，IRPS）發表論文，另一會議為日受國際重視、每年於日本舉行之國際固態電子元件與材料會議（International Conference on Solid State Devices and Materials，SSDM）；參加會議之心得附於下一章節。期刊論文則分別為 IEEE EDL（Electron Device Letter）一篇以及 JAP（Journal of Applied Physics）兩篇。此外，本研究計畫成果亦匯集成兩本博士論文（其中一本僅少部分）。所有相關成果分別詳列如下：

[A] Conference Papers

[1] M. C. Chen, C. W. Tsai, S. H. Gu, T. Wang, S. Huang Lu, S. W. Lin, G. S. Yang, J. K. Chen, S. C. Chien, Y. T. Loh, and F. T. Liu, “Soft Breakdown Enhanced Hysteresis Effects in Ultra-Thin Oxide SOI nMOSFETs,” ***IRPS Proceedings***, pp. 404-408, 2002

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[B] Journal Papers

[1] C. W. Tsai, M. C. Chen, S. H. Gu, and T. Wang, “Substrate Bias Dependence of Breakdown Progression in Ultrathin Oxide pMOSFETs”, IEEE Electron Device Letter**,** VOL. 24, NO. 4, pp. 269-271, 2003.

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[3] M. C. Chen, S. H. Gu, C. T. Chan, and T. Wang, “Comparison of Oxide Breakdown Progression in Ultra-thin Oxide Silicon-On-Insulator and Bulk Metal-Oxide-Semiconductor Field Effect Transistors,” Journal of Applied Physics, VOL. 96, NO. 6, pp.3473-3477, 2004

[C] Ph. D. Dissertations

[1] C. W. Tsai, “Investigation of Direct Tunneling Induced Reliability Issues in Ultra-Thin Oxide CMOS Devices,” Ph. D. Dissertation, National Chiao Tung University, Taiwan, 2003

[2] M. C. Chen, “Investigation of Soft Breakdown Induced Reliability Issues in Ultra-Thin Oxide SOI Devices,” Ph. D. Dissertation, National Chiao Tung University, Taiwan, 2004

[A] Conference Papers

[1]

Soft Breakdown Enhanced Hysteresis Effects in Ultra-Thin Oxide SOI nMOSFETs

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Abstract

The impact of soft breakdown location on V_t hysteresis in partially depleted SOI nMOSFETs with ultra-thin oxide (1.6nm) is investigated. Two breakdown enhanced hysteresis modes are identified. In a channel breakdown MOSFET, excess holes attributed to valence electron tunneling flow to the floating body and thus cause V_t hysteresis in gate bias switching. As a contrast, in a drain-edge breakdown device, enhanced V_t hysteresis is observed during drain bias switching because of increased band-to-band tunneling current.

Introduction

Silicon-on-insulator (SOI) technology has emerged as a promising technology for low power and/or high performance digital application. The floating body configuration is desirable in scaled SOI CMOS technology from the viewpoint of area efficacy. Unfortunately, the floating body configuration of partially depleted SOI MOSFETs will result in V_t hysteresis due to the long time constants associated with various body charging/discharging mechanisms, including positive feedback of impact ionization [1], gate tunneling [2] and GIDL current [3]. Timing large-scale circuits with hysteretic V_t variation, which leads to hysteretic delay and noise margin variations, becomes one of the most challenging tasks in bringing SOI devices into mainstream applications [4].

In bulk CMOS, the only noticeable signature of gate oxide soft breakdown (SBD) is an increase in leakage current without degrading any on-state device performance in operation [5]. However, this excess substrate leakage current will vary the floating body potential in SOI devices and give rise to different hysteresis modes depending on the location of the SBD spot. For example, if breakdown occurs in the transistor channel, excess holes attributed to valence band electron tunneling at a positive gate bias flow to the floating body and thus cause V_t fluctuation. On the other side, if the breakdown spot is in the drain extension region, the V_t hysteresis will be enhanced at a large drain bias due to increased band-to-band tunneling current. In this study, our purpose is to explore the dependence of the V_t hysteresis on SBD position in PD SOI nMOSFET's.

Device Structure and Characterization

The schematic top-view of a partially depleted SOI nMOSFET used in this study is shown in Fig. 1. The test device has a H-gate structure with an additional contact to facilitate the measurement of body current and voltage. The devices were made with an optimized 0.15μm CMOS process on p-type silicon and have a gate length of 0.15μm, a gate width of 10μm and an oxide thickness of 1.6nm. In this paper, all devices were stressed at constant voltage (3.3V) with source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection is chosen to be 100μA. After breakdown, the device on-state characteristics were checked and no difference was observed.

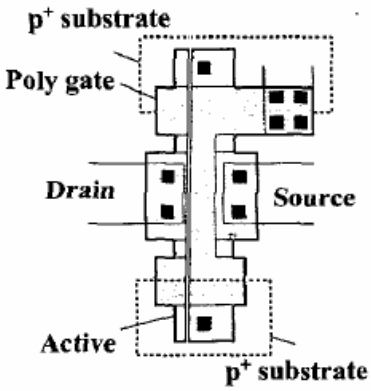

Fig. 1 Schematic representation (top-view) of a H-gate partially depleted SOI nMOSFET.

The breakdown position is examined by using the method given in [6]. Table 1 shows the ratio of $I_d/(I_s+I_d)$ before and after SBD in two SOI devices, device A and device B. The measurement gate bias is V_g=-1.5V and V_d=V_s=0V. An enormous increase of $I_d/(I_s+I_d)$ in device B indicates that breakdown is located at the drain edge, while in device A the moderate change in I_d/I_s+I_d implies that SBD position is in the channel. Aside from I_d/I_s+I_d, we further measured I_b/I_s+I_d (also shown in Table 1). In the c-SBD device, hole tunneling from the substrate to the gate is

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enhanced, thus resulting in a larger ratio of I_b to I_s+I_d. In the case of e-SBD, since the breakdown is above the drain edge, the hole tunneling current in the channel region should remain almost the same as before SBD. Nevertheless, the increased edge leakage current makes I_s+I_d larger and leads to a smaller I_b/I_s+I_d.

Table 1 The ratio of $I_d/(I_s+I_d)$ and $I_b/(I_s+I_d)$ before and after soft breakdown in two SOI nMOSFETs. The measurement bias is V_g = -1.5V and V_d=V_s=0V

	device A (c-SBD)	device B (e-SBD)
I_d/I_s+I_d before SBD	0.496	0.486
I_d/I_s+I_d after SBD	**0.155**	**0.989**
I_b/I_s+I_d before SBD	0.052	0.0488
I_b/I_s+I_d after SBD	**0.169**	**0.0092**

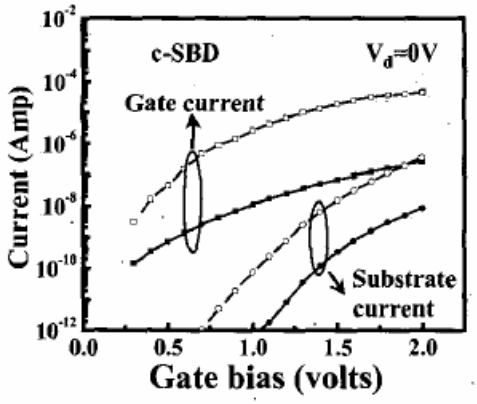

Fig. 2 Gate current and substrate current versus gate bias. Filled symbols refer to an unstressed device and open symbols refer to the device after channel SBD.

Post-SBD gate current and substrate current versus gate bias are shown in Fig. 2 (c-SBD) and in Fig. 3 (e-SBD). The substrate current at a positive gate bias is attributed to valence-band electron tunneling from Si substrate to the conduction band of the gate. It should be remarked that valence electron tunneling occurs mainly in the channel. It is unlikely to occur in the n+ drain region since the valence-band edge in the n+ drain is aligned with the bandgap in the n+ poly-gate. As a result, the post c-SBD I_b is increased drastically at a positive gate bias due to a localized effective thinning of the oxide [7] (Fig. 2) while I_b is nearly unchanged after e-SBD (Fig. 3).

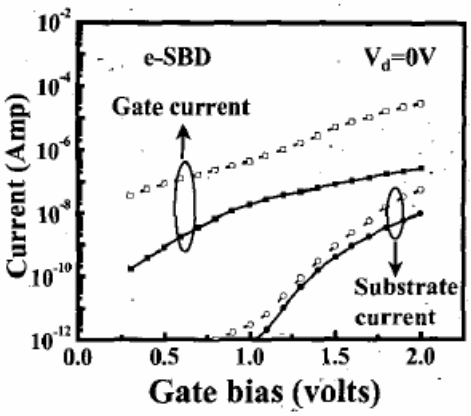

Fig. 3 Gate current and substrate current versus gate bias. Filled symbols refer to an unstressed device and open symbols refer to the device after drain-edge SBD

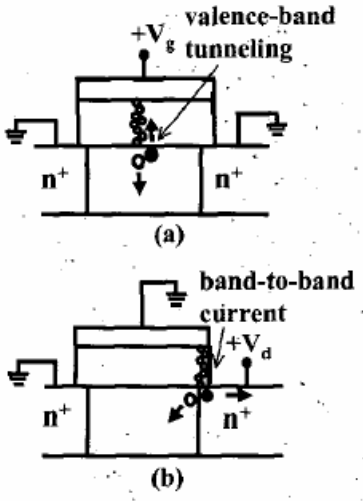

Fig. 4 Illustration of two soft-breakdown enhanced floating-body charging processes in SOI nMOSFETs. (a) Soft breakdown in the channel region and hole creation due to valence band tunneling (b) soft breakdown in the drain region and enhanced band-to-band current

Modes of SBD Enhanced Hysteresis

Fig. 4 illustrtaes channel breakdown and drain-edge breakdown [8] and respective floating-body charging processes. In a c-SBD device with a positive gate bias (Fig. 4(a)), valence band electron tunneling from the substrate to

the gate is increased after SBD. The excess holes left behind in the valence band flow to the body and raise the body potential. Fig. 4(b) illustrates the drain-induced floating-body charging in an e-SBD MOSFET. If the breakdown path is in the drain edge, band-to-band tunneling current is increased due to a larger band bending in the n^+ drain (Fig. 5(a)), thus raising the body potential at a high drain bias. On the contrary, the band-to-band current does not change in a c-SBD device (Fig. 5(b)). From the above result, it can be concluded that the body charging current I_b in a SBD device can be enhanced either in gate switching or in drain switching depending on the location of the SBD spot.

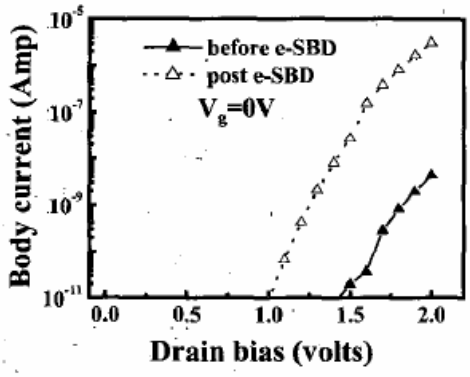

Fig. 5(a) The body current versus drain bias before e-SBD and after e-SBD

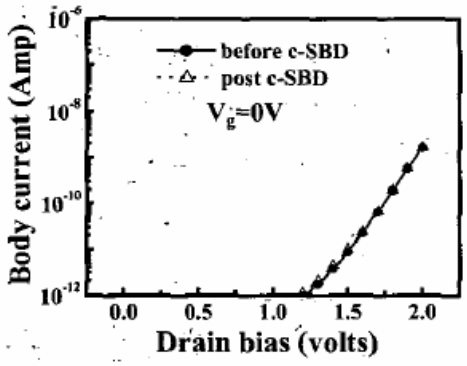

Fig. 5(b) The body current versus drain bias before c-SBD and after c-SBD

Results and Discussion

Fig. 6 shows the hysteresis in I_{ds}-V_{gs} of an SOI nMOSFET before and after c-SBD. The measurement drain bias is 0.1V. The gate bias has a forward sweep from 0V to 1.0V and then a reverse sweep. Note that (i) the subthreshold hysteresis before SBD is minimal and (ii) the post-SBD hysteresis is induced by a gate bias sweep in this device. Fig. 7 shows the hysteresis in transconductance (g_m) after c-SBD. The corresponding body potential fluctuation in gate bias sweep is shown in Fig. 8. The arrow in the figure indicates the direction of sweep. After c-SBD, the body potential begins to rise when the V_g sweep amplitude is above 0.8V. The gate switching induced body potential variation can be as large as 0.5V in this case. The pre-SBD body potential hysteresis at the same switching amplitude is less than a few tens of milli-volts.

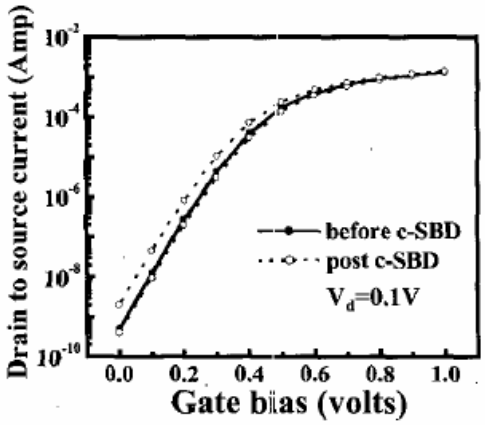

Fig. 6 Hysteresis in I_{ds} versus V_g in a c-SBD SOI device Measurement is performed with forward and then reverse gate bias sweeps

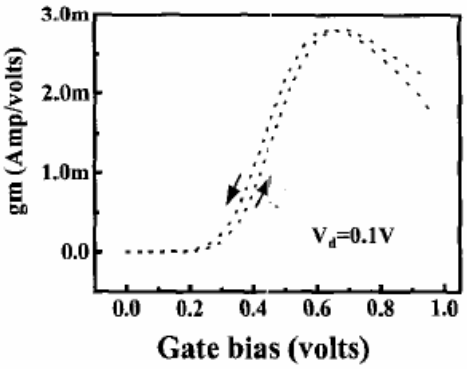

Fig. 7 Hysteresis in gm versus V_g in a c-SBD SOI device. Measurement is performed with forward and then reverse gate bias sweeps

In the e-SBD device, although gate enhanced hysteresis is not observed, drain sweep induced hysteresis in subthreshold region appears to be remarkable (Fig. 9). In the measurement, V_{gs} is 0V and the drain bias is from 0V to

1.2V and then has a reverse sweep. The corresponding body potential variation in the drain switching is shown in Fig. 10. The e-SBD enhanced hysteresis effect in drain bias switching is clearly shown in this figure. It should be noted that this drain induced hysteresis is caused by off-state band-to-band current rather than on-state hot carrier impact ionization reported previously [1].

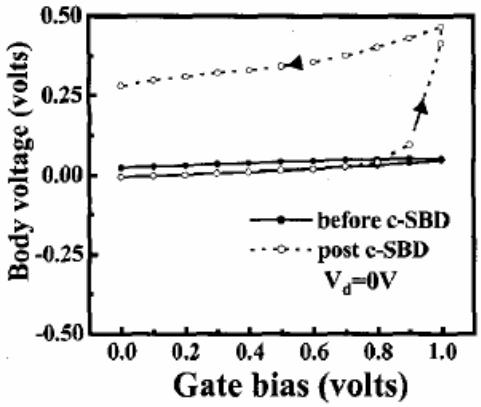

Fig. 8 Measured floating-body potential hysteresis before and after c-SBD.

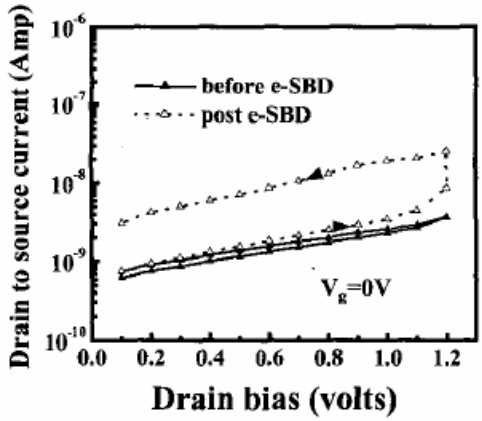

Fig. 9 Hysteresis in off-state subthreshold current in an e-SBD nMOSFET. Measurement is performed with forward and then reverse drain sweeps from 0V to 1.2V

The degree of hysteresis in terms of the body potential variation versus the amplitude of the sweep voltage is shown in Fig. 11 for gate bias sweep and in Fig. 12 for drain bias sweep. In gate bias sweep, the c-SBD device shows the largest hysteresis effect while in drain bias sweep the hysteresis effect in the e-SBD device is most significant. The SBD induced hysteresis may become appreciable even when the supply voltage is below 0.8V.

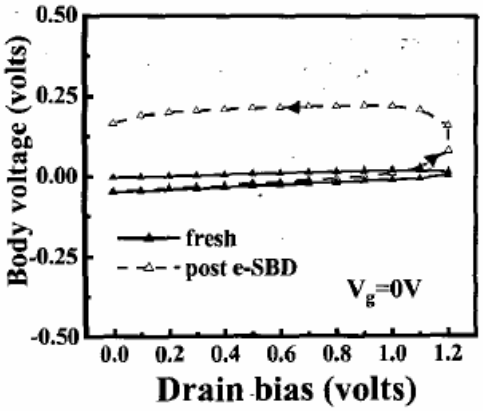

Fig. 10 Measured floating-body potential before and after e-SBD. Measurement is performed with forward and then reverse drain bias sweeps.

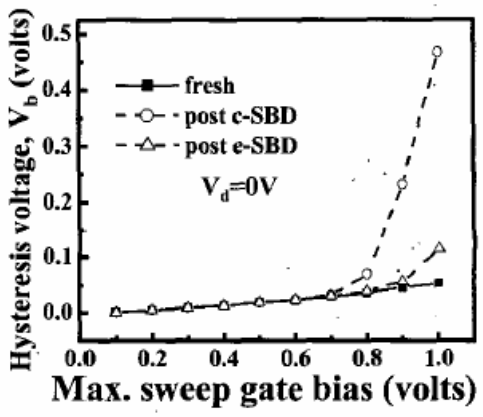

Fig. 11 The variation of body voltage V_b as a function of the amplitude of drain bias sweep.

Fig. 13 illustrates the dominant V_t hysteresis mode during the switching of a SOI CMOS inverter. Hot carrier induced hysteresis may occur in on-state [1]. c-SBD enhanced V_t hysteresis takes place when input signal is at high level and e-SBD enhanced V_t hysteresis dominates when input signal is at low level. Our study reveals that SBD in PD SOI MOSFETs not only increases leakage current but also affects circuit stability.

Conclusion

The significance of soft breakdown position to the V_t hysteresis in PD SOI CMOS devices has been evaluated. Two SBD enhanced hysteresis modes in off-state CMOS are

identified. The SBD enhanced hysteresis may occur with supply voltage less than 1.0V and will be a serious reliability concern in ultra-thin oxide SOI CMOS.

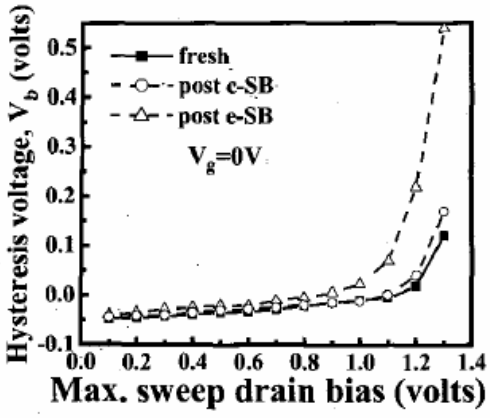

Fig. 12 The variation of body voltage V_b as a function of the amplitude of gate bias sweep.

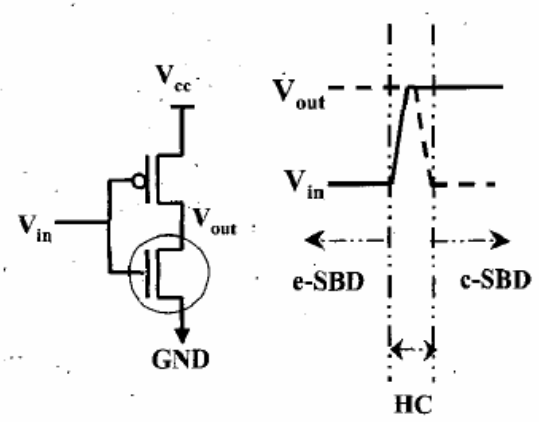

Fig. 13 Illustration of the dominant Vt hysteresis modes in the switching of an SOI CMOS inverter.

Acknowledgement

The authors would like to acknowledge United Microelectronics Co., Taiwan for providing financial support and fabricating SOI devices.

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[2]

Negative Substrate Bias Enhanced Breakdown Hardness in Ultra-Thin Oxide pMOSFETs

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Abstract

Negative substrate bias enhanced breakdown hardness in ultra-thin oxide (1.4nm) pMOS is observed. This result is believed due to the increase of hole stress current during breakdown progression via breakdown induced carrier heating. Numerical analysis of substrate bias effect on hole tunneling current is performed to support the proposed theory. This phenomenon is particularly significant to gate oxide reliability in floating substrate (PD-SOI) or forward-biased substrate devices.

Introduction

Gate oxide breakdown (BD) has been considered as one of the most critical reliability issues for aggressive scaling of oxide thickness. In ultra-thin oxide devices, oxide BD behavior is quite different from that in thicker oxides [1-3]. Fig. 1 compares BD evolution in a 1.4nm oxide and a 2.5nm oxide pMOS. Oxide BD in the 1.4nm oxide device is evolved in a progressive way, and the oxide leakage current increases gradually with stress time. Previous study has shown that a small increase in gate leakage due to oxide BD is considered to be nondestructive for circuit operation [4]. The criterion for oxide failure is thus determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate. It has been reported that the BD hardness of oxide is influenced by the BD location in a device or the stress bias condition [5-7]. The type of MOSFETs [8] and the current compliance [7] also affect the hardness of BD.

A forward substrate bias (V_b) is sometimes employed in certain analog and digital circuits to achieve improved device characteristics, such as better transistor matching [9] and lower flicker noise [10] in analog circuits and higher I_{on}/I_{off} ratio in DTMOS circuits [11]. In addition, the floating body configuration of partially depleted SOI CMOS will result in a non-zero body voltage due to various body charging mechanisms [12]. Although the dependence of oxide breakdown on reverse substrate bias has been widely explored [13], a forward substrate bias effect on the evolution of oxide BD in ultra-thin oxide pMOS is rarely studied.

In this work, we observe for the first time that the BD progression rate in a 1.4nm oxide pMOS exhibits distinct substrate bias (V_b) dependence. Typical BD growth rate with various stress substrate biases is shown in Fig. 2. The device area is 2μmx2μm. The Weibull distribution of oxide failure time is shown in Fig. 3. In measurement, all the devices were stressed at a high gate voltage (V_g=-3.5V, V_b=V_s=V_d=0V,) until the onset of BD (t_{BD}), defined as 50% increase in gate current. Then, the devices were subjected to a lower gate voltage stress (V_g=-3.0V, V_s=V_d=0V) with different V_b to investigate the BD evolution rate. The oxide failure time (t_{fail}) in Fig. 3 is defined as 15X increase in gate leakage current, compared to an unstressed device. The mechanism for the increased breakdown progression rate with a forward substrate bias will be discussed.

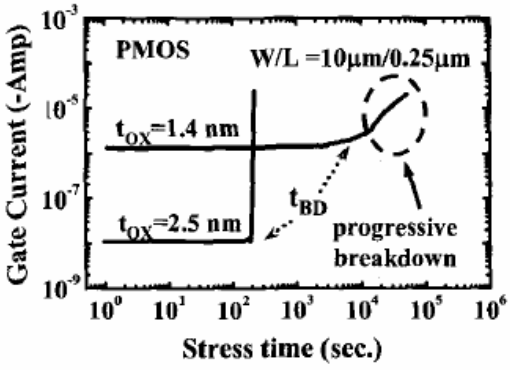

Fig. 1 Comparison of breakdown behavior in a 1.4nm oxide pMOS and in a 2.5nm oxide pMOS. The stress gate voltage is –3V for the 1.4nm oxide and –4.5V for the 2.5nm oxide. t_{BD} denotes the onset of oxide breakdown. The current compliance for t_{BD} is 50% increase in gate current.

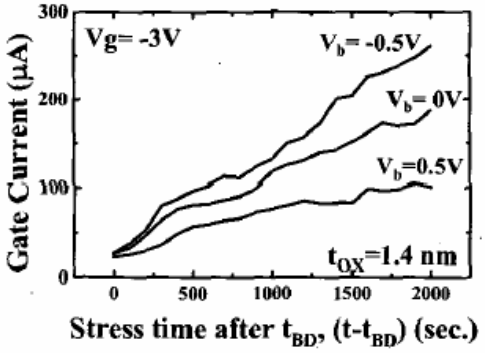

Fig. 2 Substrate bias dependence of oxide breakdown evolution in a 1.4nm oxide pMOS. The stress gate voltage is –3.5V before t_{BD} and is –3V after t_{BD}. The device area is 2μmx2μm.

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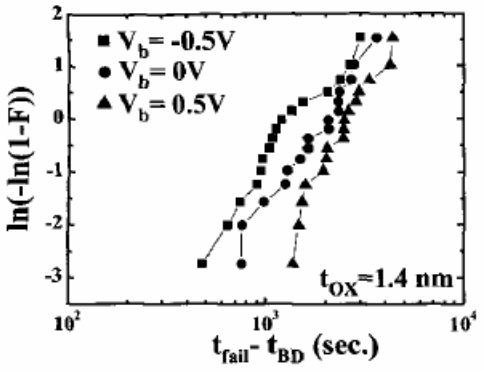


Fig. 3 The Weibull plot of t_{fail} distribution for V_b =-0.5V, 0V, and 0.5V.

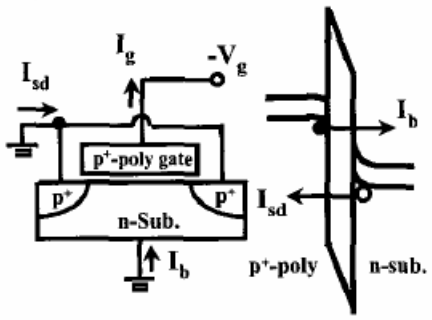


Fig. 4 Illustration of charge separation measurement and current flow in a pMOS at a negative-gate bias. I_b denotes electron stress current and I_{sd} represents hole stress current.

V_b Dependence of Stress Current

In ultra-thin oxide pMOS, the gate stress current may have comparable electron and hole components at a negative gate bias. To analyze the polarity of dominant stress current in a pMOS, a charge separation technique is used to separate electron stress current and hole stress current. Fig. 4 illustrates the measurement method and the carrier flow at a negative gate bias. I_b denotes electron current and is constituted by valence-band electron tunneling from the gate. I_{sd} stands for hole tunneling current from the inverted channel. The result for I_b and I_{sd} in a 1.4nm oxide and in a 2.2nm oxide pMOS is shown in Fig. 5. Note that the dominant stress current in the 1.4nm oxide pMOS changes from electron current in a fresh device to hole current after t_{BD}. Moreover, the V_b dependence of electron current and hole current before and after t_{BD} is shown in Fig. 6. It should be noted that, unlike pre-t_{BD} I_b and I_{sd}, the post-t_{BD} hole current increases significantly with a forward V_b. Furthermore, Fig 7 shows the V_b dependence of post-t_{BD} hole current increases with BD evolution. Since the hole current dominates during BD evolution and increases with negative V_b, the V_b dependence of BD progression can be understood.

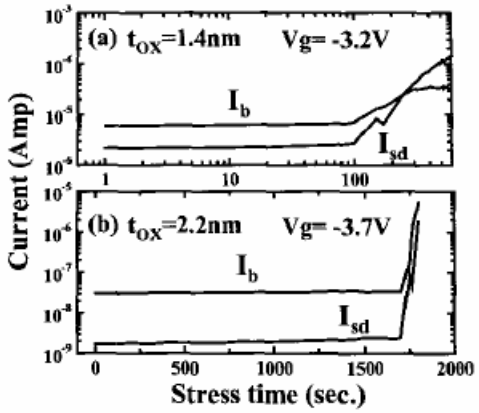


Fig. 5 Electron and hole current components versus stress time in a 1.4nm oxide pMOS (a) and in a 2.2nm oxide pMOS (b).

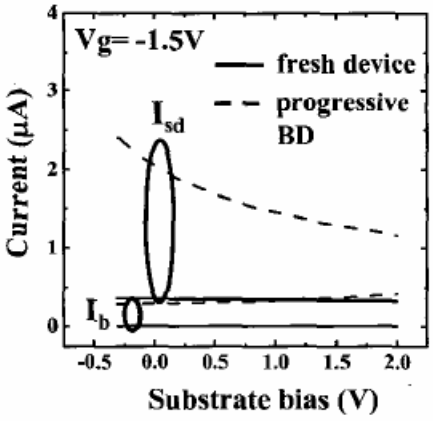
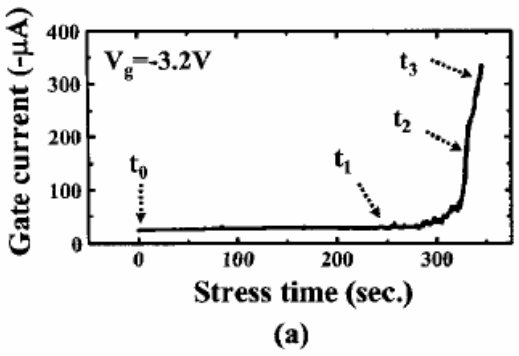


Fig. 6 The dependence of electron current and hole current on substrate bias in a 1.4nm oxide pMOS.

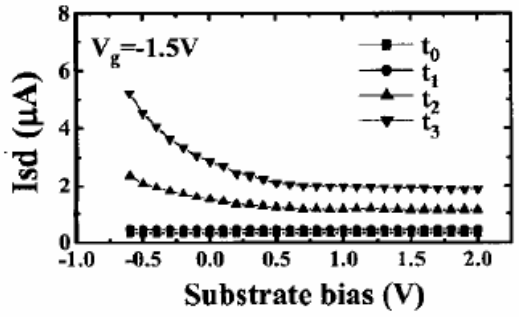
BD Caused Carrier Heating and V_b Dependence

Because the post-t_{BD} hole current increases with negative V_b while the electron current (I_b) remains almost unchanged (Fig. 6), the possibility that the V_b dependence of the post-t_{BD} hole current is caused by the variation of

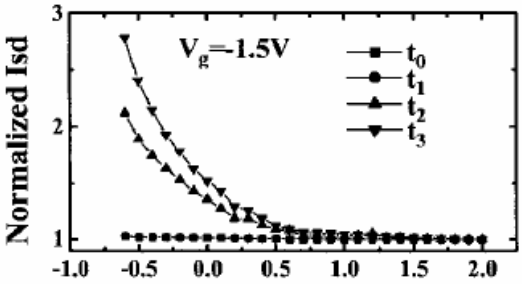
effective gate-to-channel voltage [2] resulting from V_b modulated channel resistance should be excluded. Otherwise, the electron tunneling current should possess similar V_b dependence as the hole current. Moreover, substrate impact ionization [13] and NBTI effects are also excluded because the trend of the V_b dependence is opposite.



(a)



(b)



(c)

Fig. 7 (a)Gate current vs. stress time in a 1.4nm oxide pMOS. V_g=-3.2V. (b)The corresponding V_b dependence of hole current at t_0, t_1, t_2 and t_3. V_g =-1.5V. (c)Normalized V_b dependence of I_{sd}. I_{sd} is normalized to its value at V_b=2V. V_g =-1.5V.

To further investigate the origin of the V_b dependence of the post-t_{BD} hole current, we measured the spectral distribution of hot carrier light emission before and after t_{BD}. The light intensity is greatly increased after BD (Fig. 8). Similar result was also obtained by other groups [14]. The high-energy tail of the post-t_{BD} spectral distribution indicates the rise of the carrier temperature. There are two possible theories to explain the rise of channel carrier temperature in the BD spot. First, based on the model proposed by [14], the gate voltage will penetrate into the substrate after BD and cause lateral field heating of channel carriers. However, this process is unlikely here since the post-t_{BD} electron current and hole current have distinctly different V_b dependence. The second reason is that high-dissipated energy, released by valence electrons tunneling from the gate through the BD path, will locally produce a rise of hole temperature. A temperature range of 1000K to 2000K was estimated in [15]. Electron-hole scattering or Auger recombination is suspected to be the responsible energy transfer process.

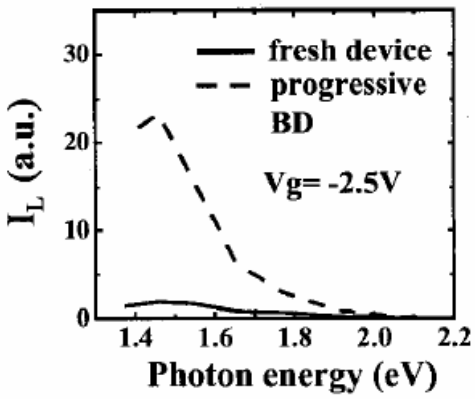


Fig. 8 Spectral distribution of light emission in a 1.4nm oxide pMOS at V_g =-2.5V.

To show that the rise of hole temperature may account for the observed V_b dependence, we calculate the hole tunneling current with hole temperature at 300K and 1300K. In our calculation, we solved the coupled Poisson and Schrodinger equation to obtain the sub-band structure for the inversion holes (Fig. 9). An one-band effective mass approximation is adopted. The hole tunneling current is calculated according to the Tsu-Esaki formula [16]

$$I_{sd} = qm^*\left(\frac{1}{2\pi^2\eta^3}\right)k_BT\sum_n D_n\{\ln(1+\exp((E_n-E_f)/k_BT))) - \ln(1+\exp((E_n-E_{f'})/(k_BT)))\} \quad (1)$$

where E_f ($E_{f'}$) denotes the Fermi energy in the channel (poly gate) and D_n is the hole tunneling probability of the n-th sub-band. m^* is the hole effective mass in Si. Other variables have their usual definitions. It should be emphasized that it is not our intention here to consider detailed trap-assisted charge transport in the BD path. It is also not our intension to calculate the precise current value before and after oxide BD since the BD area and BD caused effective oxide thinning cannot be easily determined. Instead, our purpose is to investigate the effect of hole temperature on the distribution of inversion holes in different sub-bands and the corresponding substrate bias effect on hole tunneling current. Therefore, the simple WKB formula for direct tunneling is employed for D_n.

Our result in Fig. 10 clearly shows that the hole tunneling current exhibits larger V_b dependence at 1300K. The simulation can well interpret the measured V_b dependence of post-t_{BD} I_{sd} by simply using an elevated hole temperature. We also simulate the V_b dependence for another oxide thickness (0.6nm). Similar trend of the V_b dependence is obtained (Fig. 11). The effective post-t_{BD} oxide thickness is possibly between the two thicknesses. The simulated change of post-t_{BD} I_{sd} from V_b=0.5V to V_b =-0.3V is about 31% for t_{ox}=0.6nm and is about 43% for t_{ox}=1.4nm. The measured result is about 43% (Fig. 6). The measured and calculated results are consistent in orders of magnitude.

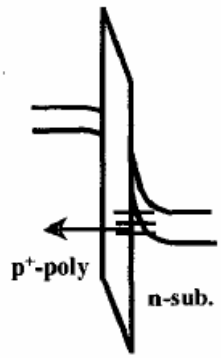


Fig. 9 Hole direct tunneling from each sub-band (m^*=0.68m_0, m_{SiO2}=0.55m_0, Φ_h=4.25eV).

Conclusion

In ultra-thin oxide pMOS, hole current is found to dominate BD progression. Enhanced breakdown hardness is observed with a negative stress substrate bias. Numerical analysis shows that the enhanced hardness can be explained by the increase of hole temperature in the breakdown spot. The V_b accelerated BD progression has large impact in SOI or DTMOS-like devices.

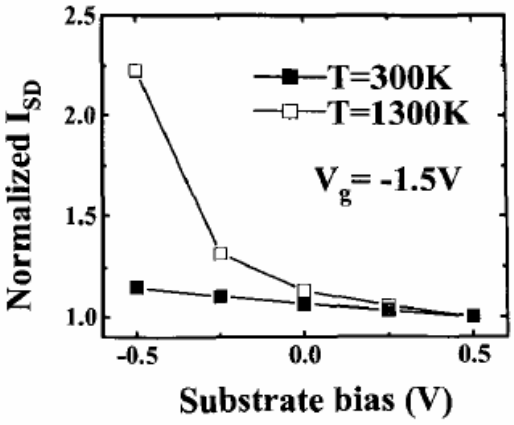


Fig. 10 Simulated substrate bias effect on hole current density in a 1.4nm oxide pMOS. I_{sd} is normalized to its value at V_b=0.5V. V_g =-1.5V.

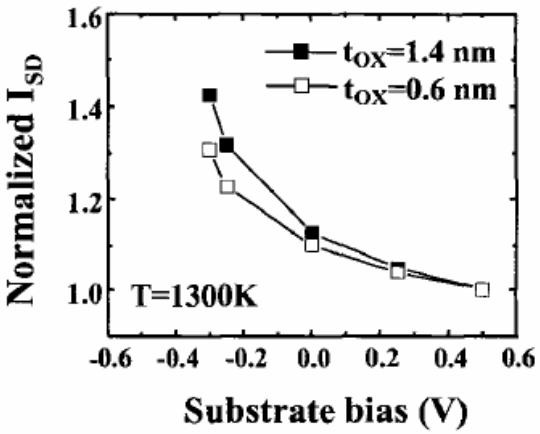


Fig. 11 Simulated substrate bias effect with t_{ox}=1.4nm and 0.6nm. V_g =-1.5V.

Acknowledgements

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C-6-3

Floating Body Accelerated Oxide Breakdown Progression in Ultra-Thin Oxide SOI pMOSFETs

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1. Abstract

Enhanced oxide breakdown progression in ultra-thin oxide (1.4nm) SOI pMOS is observed, as compared to bulk devices. The enhanced progression is attributed to the increase of hole stress current resulting from breakdown induced channel carrier heating in a floating-body configuration. Numerical analysis of hole tunneling current and hot carrier luminescence measurement are performed to support the proposed theory.

Keywords: breakdown progression, SOI pMOS, carrier temperature, body potential.

2. Introduction

It has been reported that oxide breakdown (BD) behavior in ultra-thin oxides is quite different from that in thicker oxides [1-3]. Fig. 1 shows that oxide BD in a 1.4nm oxide pMOS is evolved in a progressive way and the oxide leakage current increases slowly with stress time. Previous study has shown that a small increase in gate leakage due to oxide BD is considered to be nondestructive for circuit operation [4]. The criterion for oxide failure is thus determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate.

In this work, we observe an enhanced BD progression rate in 1.4nm oxide PD SOI pMOS, as compared to bulk devices (Fig. 2). The Weibull distribution of oxide t_{BD} and t_{fail} for SOI and bulk pMOS is plotted in Fig. 3. The gate stress voltage is −2.9V. t_{BD} and t_{fail} are defined as 50% and 15X increase in gate current, respectively. Although SOI and bulk devices exhibit the same time-to-breakdown (t_{BD}), the SOI pMOS apparently has a shorter time-to-failure (t_{fail}).

3. Mechanism for Floating-body Enhanced BD Progression

The floating body configuration of SOI devices will result in a small forward body voltage due to various body charging processes. The SOI samples were fabricated with an additional body contact to facilitate the measurement of body potential and current. To analyze the polarity of gate stress current, a charge separation measurement is performed (Fig. 4(a)). Fig. 4(b) shows that the dominant stress current changes from electron current (I_b) to hole current (I_{sd}) after t_{BD}. *More interestingly, unlike I_b and I_{sd} in a fresh device, the post-t_{BD} hole current exhibits significant body bias (V_b) dependence (Fig. 5).* This V_b dependence is more distinguished at a smaller gate bias (Fig. 6). Fig. 7 shows the range of stress gate bias where hole current is dominant. Because hole stress current dominates during BD evolution and it increases with a forward body bias, the enhanced BD progression due to the floating body configuration in SOI can be understood. Fig. 8 compares the time-to-failure in SOI and bulk pMOS. Accelerated BD progression is noticed in SOI samples. This trend is more apparent at lower stress gate biases. The measured result is consistent with the V_b dependence in Fig. 6.

4. BD Caused Carrier Heating and V_b Dependence

Since the post-t_{BD} electron current does not exhibit V_b dependence (Fig. 5), *the possibility that the V_b dependence of the post-t_{BD} I_{sd} is caused by the variation of effective gate-to-channel voltage [2] resulting from V_b modulated channel resistance is excluded.* Otherwise, the post-t_{BD} I_b should have similar V_b effect. Moreover, substrate impact ionization and NBTI effects are also excluded because the trend of the V_b dependence is opposite.

Fig. 9 shows the measured spectral distribution of hot carrier light emission in a post-t_{BD} pMOS. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300K (Fig. 9(b)). The possible explanation for the rise of carrier temperature is that high-dissipated energy, released by valence electrons from the gate through the BD path, will locally produce a temperature rise of carriers in the channel [5]. In order to show that an elevated hole temperature may account for the observed V_b dependence, we calculate the hole tunneling current with hole temperature at 300K and 1300K through the Tsu-Esaki formula [6],

$$I_{sd} = qm^*\left(\frac{1}{2\pi^2\hbar^3}\right)k_BT\sum_n D_n\{\ln(1+\exp((E_n-E_f)/k_BT))) - \ln(1+\exp((E_n-E_{f'})/(k_BT)))\} \quad (1)$$

where E_f ($E_{f'}$) denotes the Fermi energy in the channel (poly gate) and D_n is the hole tunneling probability of the n-th sub-band. Other variables have their usual definitions. The detail of the calculation can be found in our earlier publication [3]. *It should be emphasized that it is not our intention here* to model trap-assisted charge transport in the BD path. Instead, our purpose is to investigate the effect of hole temperature on hole distribution in sub-bands and corresponding V_b effect on hole tunneling current. Our simulation (Fig. 10) clearly reveals that the V_b dependence of the hole tunneling current indeed increases with hole temperature. The trend is similar to the measured V_b dependence in Fig. 6. To explain the temperature effect on the V_b dependence in more detail, the distribution of inversion holes in the lowest three sub-bands is given in Table. 1. At T=300K, channel holes mostly reside in the first sub-band no matter of V_b. At T=1300K, a large part of holes are thermally excited to higher sub-bands at a forward body voltage (-0.3V), where the oxide tunneling probability is larger. Thus, a much larger hole tunneling current is obtained at V_b= -0.3V.

5. Conclusion

In ultra-thin oxide SOI pMOS, breakdown progression is aggravated by a forward body bias. A larger post-t_{BD} gate current is observed in SOI devices (Figs. 2&5). The V_b accelerated BD progression has large impact on the failure time of SOI and DTMOS devices.

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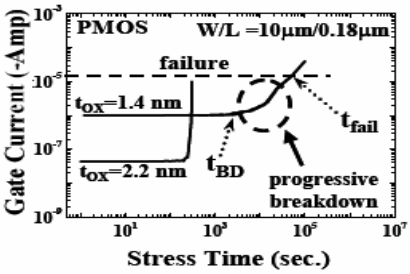


Fig. 1 Comparison of breakdown behavior in a 1.4nm oxide pMOS and in a 2.2nm oxide pMOS. The stress gate voltage is –2.6V for the 1.4nm oxide and –3.9V for the 2.2nm oxide. t_{BD} denotes the onset of oxide breakdown.

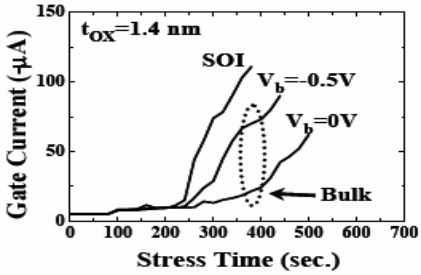


Fig. 2 Oxide breakdown progression in bulk and SOI pMOS. Stress V_g=-2.9V at T=125C.

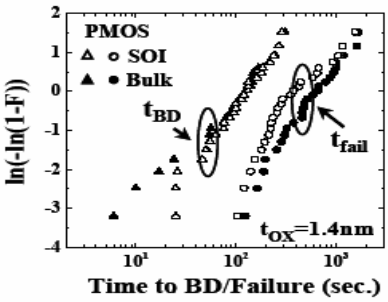
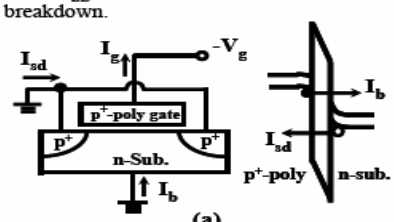


Fig. 3 Weibull plots of t_{BD} and t_{fail} distribution for 1.4nm oxide devices.



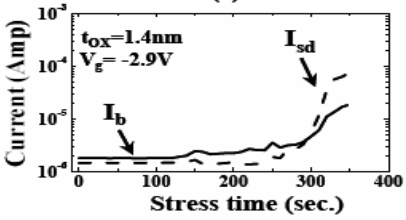


Fig. 4(a)Illustration of current flow in a pMOS at a negative gate bias. I_b (I_{sd}) denotes electron (hole) stress current. (b)Electron and hole current components versus stress time.

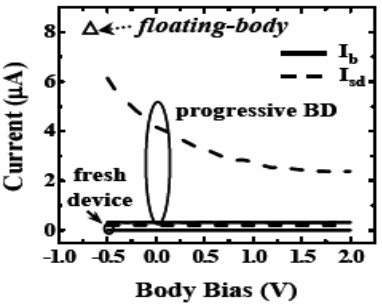


Fig. 5 The dependence of electron current and hole current on body bias at Vg=-1.5V. Hole current during progressive BD in a floating-body configuration is indicated.

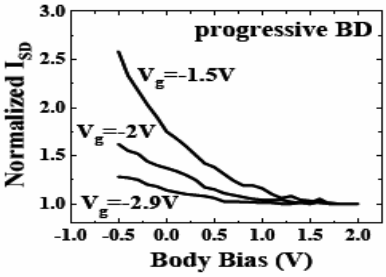


Fig. 6 Body bias dependence of hole current at various gate biases. I_{sd} is normalized to its value at V_b=2V.

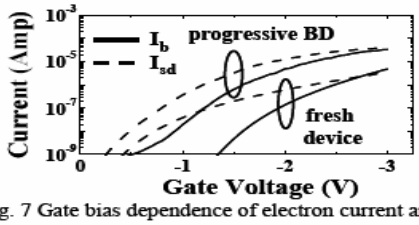


Fig. 7 Gate bias dependence of electron current and hole current in a fresh pMOS and during progressive BD.

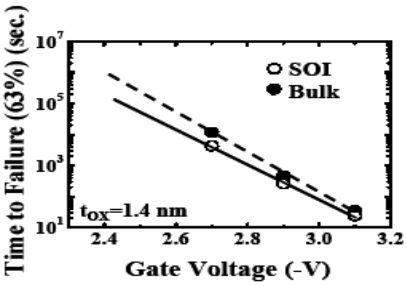


Fig. 8 t_{fail} (63%) vs. stress gate bias for SOI and bulk pMOS devices.

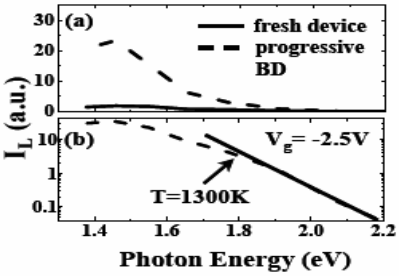


Fig. 9 (a)Spectral distribution of light emission in a 1.4nm oxide pMOS at V_g=-2.5V. (b)The extracted carrier temperature is around 1300K.

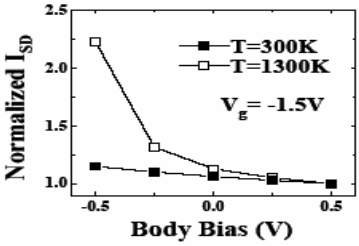


Fig. 10 Simulated body bias effect on hole tunneling current in a 1.4nm oxide pMOS. I_{sd} is normalized to its value at V_b=0.5V.

Table 1 Calculated distribution of channel holes in the lowest three sub-bands.

cond. / sub-band	channel hole dist. (%)			
	300K		1300K	
	V_b=-0.3	V_b=2	V_b=-0.3	V_b=2
1st	98	99.9	62.7	81.3
2nd	1.9	0.1	13.8	13.1
3rd	0.1	0	6	3.5

[B] Journal Papers

[1]

Substrate Bias Dependence of Breakdown Progression in Ultrathin Oxide pMOSFETs

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***Abstract*—Negative substrate bias-enhanced oxide breakdown (BD) progression in ultrathin oxide (1.4 nm) pMOS is observed. The enhanced progression is attributed to the increase of hole-stress current resulting from BD-induced, channel-carrier heating. The carrier temperature extracted from the spectral distribution of hot-carrier luminescence is around 1300 K. The substrate bias dependence of post-BD hole-tunneling current is confirmed from measurement and calculation. The observed phenomenon is particularly significant to ultrathin gate oxide reliability in floating substrate (SOI) and forward-biased substrate devices.**

***Index Terms*—Breakdown (BD) progression, carrier temperature, substrate bias, ultrathin oxide pMOS.**

I. Introduction

GATE-oxide breakdown (BD) has been considered as one of the most critical reliability issues for aggressive scaling of oxide thickness. In ultrathin oxide devices, oxide BD is evolved in a progressive way and the oxide leakage current increases slowly with stress time [1]–[3]. Previous study has shown that a small increase in gate leakage due to oxide BD is considered to be nondestructive for circuit operation [4]. The oxide failure time is thus determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate.

A forward-substrate bias (V_b) is sometimes employed in certain analog and digital MOS circuits to achieve improved device characteristics [5]. In addition, the floating body configuration of partially depleted floating substrate (SOI) CMOS will result in a nonzero body voltage due to various body-charging mechanisms [6], [7]. Although the dependence of oxide BD on V_b has been widely explored [8], [9], a forward V_b effect on the evolution of oxide BD is rarely investigated.

In this work, we observe for the first time that oxide BD progression in a 1.4-nm oxide pMOS exhibits distinct V_b dependence. The devices were stressed at a high gate voltage ($V_g = -3.5$ V) until the onset of BD ($t_{\rm BD}$), and then the devices were subjected to a lower gate voltage stress ($V_g = -3.0$ V) with different substrate bias to study the evolution of oxide BD. The Weibull distribution of oxide failure time ($t_{\rm fail}$) for different stress V_b is shown in Fig. 1 by assuming that oxide failure is defined as ten times increase in gate current. Apparently, a forward V_b aggravates BD evolution, and the responsible mechanism will be discussed.

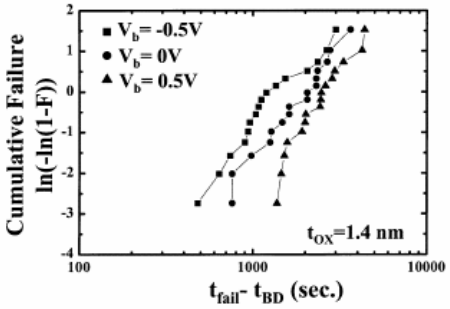

Fig. 1. Weibull plot of oxide failure time ($t_{\rm fail}$) for a 1.4-nm oxide pMOS. Stress V_g is -3 V and V_b is -0.5, 0, and 0.5 V. The $t_{\rm fail}$ is defined as an increase of gate current by ten times. The device area is 2×2 μm.

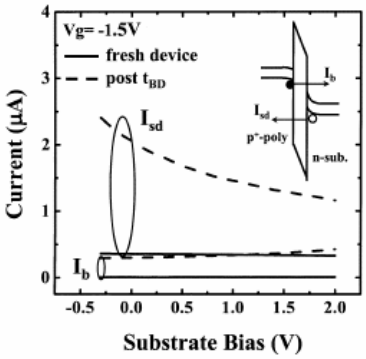

Fig. 2. Charge separation measurement result of electron current (I_b) and hole current ($I_{\rm sd}$) versus substrate bias. The inset shows the electron and hole current flows at a negative gate bias. In measurement, source, drain, and substrate are grounded, and the gate voltage is -1.5 V. The hole-tunneling current is measured at the source, and the drain and the electron current is measured at the substrate.

II. Mechanism for Enhanced BD Progression

To investigate the role of V_b in BD evolution, we analyze the polarity of stress-gate current first by using charge-separation measurement. The gate current in an ultrathin oxide (1.4 nm) pMOS is found to have comparable electron (I_b) and hole ($I_{\rm sd}$) components at a negative gate bias. Fig. 2 shows that the dominant component after $t_{\rm BD}$ is the hole current. Unlike I_b and $I_{\rm sd}$ in a fresh device, the post-$t_{\rm BD}$ hole current increases significantly with a negative V_b. By comparing the V_b dependence of

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Digital Object Identifier 10.1109/LED.2003.810890

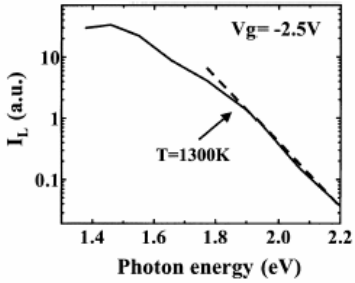


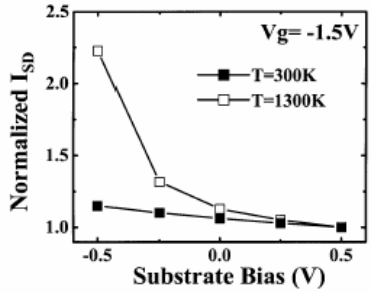
Fig. 3. Measured spectral distribution of light emission (I_L) after oxide breakdown. The dashed line represents the Boltzmann tail with a carrier temperature of 1300 K. $V_g = -2.5$ V.

post-$t_{\rm BD}$ I_b and $I_{\rm sd}$, we exclude the possibility that the V_b dependence of the post-$t_{\rm BD}$ hole current is caused by the change of effective gate-to-channel bias in the BD spot [2] resulting from V_b modulated channel resistance. Otherwise, the post-$t_{\rm BD}$ electron tunneling current (I_b) should exhibit the same V_b dependence. Furthermore, substrate impact ionization [9] and negative bias temperature instability (NBTI) effects are also excluded, since the trend of the V_b dependence is opposite.

Fig. 3 shows the measured spectral distribution of hot carrier light emission after $t_{\rm BD}$. The measurement is performed with a Hamamatsu C3230 single photon counting system. The photon number at different wavelengths is counted individually. The measurement result is then corrected for the wavelength dependence of the filter transmittance. The pre-$t_{\rm BD}$ light emission is negligible and is not shown here. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 K. There are two theories to explain the rise of carrier temperature after BD [10], [11]. First, based on the model proposed in [10], the gate voltage will penetrate into the substrate after BD and cause lateral field heating of channel carriers. This mechanism is unlikely here because the post-$t_{\rm BD}$ I_b does not exhibit V_b dependence, as pointed out earlier. The second explanation is that high-dissipated energy, released by valence electrons (I_b) from the gate through the BD path, will locally produce a temperature rise of holes in the channel [11].

III. Simulation of Hole-Tunneling Current

To show that the rise of hole temperature may account for the V_b dependence of post-$t_{\rm BD}$ $I_{\rm sd}$, we calculate the hole-tunneling current from $T = 300$ to 1300 K. In our calculation, we solved the coupled Poisson and Schrodinger equation to obtain the valence band diagram. A single band effective mass approximation is used. The hole direct-tunneling current can be calculated through the Tsu Esaki equation [12]. See (1), shown at the bottom of the page, where m^* is the hole effective mass in Si, E_f ($E_{f'}$) denotes the Fermi energy in the channel (p^+-poly), E_n stands for the nth subband energy, and D_n is the hole tunneling probability. Other variables have their usual definitions.



(a)

cond. / sub-band	channel hole dist. (%)			
	300K		1300K	
	V_b=-0.3	V_b=2	V_b=-0.3	V_b=2
1st	98	99.9	62.7	81.3
2nd	1.9	0.1	13.8	13.1
3rd	0.1	0	6	3.5

(b)

Fig. 4. (a) Simulated substrate bias effect on hole-tunneling current for different hole temperatures. The hole current is normalized to its value at $V_b = 0.5$ V. (b) Distribution of channel holes in the lowest three subbands. The gate bias in simulation is -1.5 V. The parameters used in simulation is $m^*(\text{Si}) = 0.67m_o$, $m^*(\text{SiO}_2) = 0.55m_o$, ϕ_h(hole barrier height at SiO_2 interface) = 4.25 eV, $t_{\rm ox} = 1.4$ nm, and N_B(substrate doping) $= 1 \times 10^{18}$ cm^{-3}. The density of states mass m^*(Si) is treated as a fitting parameter.

It should be emphasized that it is not our intention here to calculate detailed charge transport in the BD path since the effective oxide thickness after $t_{\rm BD}$ is not known. Instead, our purpose is to investigate the influence of hole temperature on hole distribution in subbands and corresponding V_b effect on hole-tunneling current. Therefore, the simple Wentzel–Kramers–Brillouin (WKB) formula for direct tunneling is employed. Our result in Fig. 4(a) clearly shows that the hole-tunneling current exhibits larger V_b dependence at a higher temperature. The simulation can well interpret the measured V_b dependence of post-$t_{\rm BD}$ $I_{\rm sd}$ by simply using an elevated hole temperature. To further explain the temperature effect on the V_b dependence, the distribution of channel holes in the lowest three subbands is given in Fig. 4(b). Before $t_{\rm BD}$, hole temperature is 300 K. Most of inversion holes reside in the first subband, regardless of V_b, for example, 99.9% at $V_b = 2$ V versus 98% at $V_b = -0.3$ V. In other words, the V_b effect on hole-tunneling current is small at 300 K. After $t_{\rm BD}$, the hole temperature is increased. For $V_b = 2$ V, since the substrate confinement field is large, a large part of holes (81%) still stay in the first subband, although the hole temperature is rather high (1300 K), but for $V_b = -0.3$ V, the confinement substrate field is small, and a large portion of holes are thermally excited to higher sub-bands, where the oxide tunneling probability is large.

$$I_{\rm sd} = qm^* \left(\frac{1}{2\pi^2\hbar^3}\right) k_B T \sum_n D_n \left\{\ln\left(1+\exp\left(\frac{(E_n - E_f)}{(k_B T)}\right)\right) - \ln\left(1+\exp\left(\frac{(E_n - E_{f'})}{(k_B T)}\right)\right)\right\} \quad (1)$$

A larger hole-tunneling current is obtained. Thus, the substrate bias effect on hole-tunneling current becomes more significant at a higher hole temperature.

IV. Conclusion

BD evolution in ultrathin oxide pMOS is aggravated by a forward-substrate bias. Numerical analysis shows that the enhanced BD evolution can be explained by a rise of substrate hole temperature and thus increased hole stress current. The accelerated BD evolution has large impact on circuit lifetime in forward-biased substrate or SOI devices.

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Soft breakdown enhanced hysteresis effects in ultrathin oxide silicon-on-insulator metal-oxide-semiconductor field effect transistors

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The impact of oxide soft breakdown location on threshold voltage hysteresis in partially depleted silicon-on-insulator metal-oxide-semiconductor field effect transistors with an ultrathin oxide (1.6 nm) is investigated. Two breakdown enhanced hysteresis modes are identified. In a drain-edge breakdown device, excess holes result from band-to-band tunneling flow to the floating body, thus causing threshold voltage variation in drain bias switching. In contrast, in a channel breakdown device, enhanced threshold hysteresis is observed during gate bias switching because of increased valence band electron tunneling. Our findings reveal that soft breakdown enhanced hysteresis effect can be a serious reliability issue in silicon-on-insulator devices with floating body configuration.
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I. INTRODUCTION

Silicon-on-insulator (SOI) technology has emerged as a promising technology for system-on-a-chip applications, which require high-performance complementary metal-oxide-semiconductor field effect transistors (MOSFET), low power, embedded memory, and bipolar devices. The primary feature of a MOSFET with SOI configuration is that the local substrate of the device is floating electrically, and thus the substrate-source bias (V_{BS}) is not fixed. As V_{BS} changes, the device threshold voltage (V_t) will change due to the body effect. This "instability" in V_t resulting from floating body configuration becomes one of the most challenging tasks in bringing SOI devices into mainstream applications.[1–4] One manifestation of the V_t variation is the hysteresis effect. The V_t hysteresis as a result of various floating body charging/discharging mechanisms has been widely investigated.[2–4] In this work, the influence of gate oxide breakdown position on hysteresis effects in ultrathin oxide partially-depleted (PD) SOI MOSFETs will be explored.

Several causes of V_t hysteresis in PD SOI MOSFETs have been proposed.[5–8] Boudou *et al.*[5] reported that V_t hysteresis could be caused by positive feedback of impact ionization due to long time constants associated with body potential charging. Chen *et al.*[6] showed that at high drain biases the floating body effect can lead to hysteresis in the subthreshold $I_{ds}-V_{gs}$ characteristics even when the gate is biased well below its threshold voltage. Fung *et al.*[7] found that in ultrathin gate oxide devices the gate-to-body tunneling current modulates the body voltage and induces a hysteresis effect. All the above works investigate the hysteresis phenomenon in PD SOI MOSFETs without considering gate oxide soft breakdown (SBD). Recent studies[9–13] showed that in bulk CMOS the impact of gate oxide SBD is only manifested in a noticeable increase in gate leakage current without degrading other device characteristics in operation. Crupi *et al.*[14] showed that at high gate voltages the substrate current steeply increases after SBD due to localized effective thinning of gate oxide. Chan *et al.*[15] presented that in thinner oxides the post-SBD gate induced drain leakage (GIDL) current increases significantly because of the enhancement of band-to-band tunneling. Although the dependence of these excess substrate currents on the location of a SBD spot was widely explored, the influence of SBD location on V_t hysteresis in SOI devices has been rarely investigated.

II. DEVICE STRUCTURE AND CHARACTERIZATION

The devices in this work were made with a 0.13 μm standard CMOS process on p-type PD SOI substrate. The gate oxide was grown with rapid plasma nitridation (RPN) process. The gate length is 0.13 μm, the gate width is 10 μm and the oxide thickness is 1.6 nm. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this paper, all devices were stressed at high constant gate voltage with the source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection was chosen to be 10 μA. After breakdown, the device on-state characteristics were checked and no difference was observed.

TABLE I. The ratio of $I_d/(I_s+I_d)$ and $I_b/(I_s+I_d)$ before and after soft breakdown in four SOI MOSFETs. The measurement is in the accumulation region and $V_g=|1.5\ \text{V}|$, $V_d=V_s=0$ V.

	*n*MOSFET		*p*MOSFET	
Acc. region	Device A (*c*-SBD)	Device B (*e*-SBD)	Device C (*c*-SBD)	Device D (*e*-SBD)
I_d/I_s+I_d before SBD	0.5078	0.5297	0.5174	0.5251
I_d/I_s+I_d after SBD	0.4482	0.9957	0.1368	0.9387
I_b/I_s+I_d before SBD	0.0287	0.0178	0.3202	0.1163
I_b/I_s+I_d after SBD	0.1426	0.0001	10.8680	0.0102

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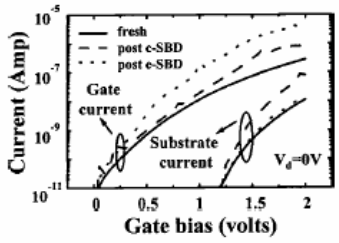

FIG. 1. Gate current and substrate current versus gate bias in *n*MOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

The breakdown position was examined by using the method proposed by Degraeve *et al.*[16] Table I shows the ratio of I_d to (I_s+I_d) before and after SBD in four SOI devices. The measurement is in accumulation region and $|V_g|$=1.5 V and $V_d=V_s=0$ V. A significant increase of $I_d/(I_s+I_d)$ in device B and device D indicates that breakdown is located at the drain edge, while in device A and device C the moderate change in $I_d/(I_s+I_d)$ implies that the SBD position is in the channel. Aside from $I_d/(I_s+I_d)$, $I_b/(I_s+I_d)$ was measured (also shown in Table I). In the channel SBD (*c*-SBD) devices, the valence band tunneling leakage in the channel region (I_b) was enhanced, resulting in a larger $I_b/(I_s+I_d)$. In the case of edge SBD (*e*-SBD), the breakdown was above the drain edge. As a result, the tunneling leakage current in the channel region remains almost the same as in pre-SBD, and the increased edge leakage current makes I_s+I_d larger and thus a smaller $I_b/(I_s+I_d)$. In short, the results in Table I shows that we can use the change of $I_d/(I_s+I_d)$ or $I_b/(I_s+I_d)$ to determine the breakdown location in the channel or in the drain edge region.

By utilizing the above technique, the device electrical behavior in *c*-SBD and *e*-SBD devices were characterized. In Fig. 1, the gate current and the substrate current as a function of V_g in a fresh, *c*-SBD, and an *e*-SBD *n*MOSFET were compared. The result shows that the substrate current increases drastically after *c*-SBD, but has little change after *e*-SBD. The substrate current at a positive gate bias is attributed to valence electron tunneling from the channel to the gate. The generated holes left behind in the channel then flow to the substrate. This tunneling process is unlikely to occur in the n^+ drain region since the valence-band edge of the n^+ drain is aligned with the band gap of the n^+ poly-gate.

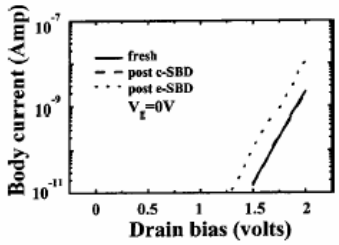

FIG. 2. Body current versus drain bias in *n*MOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

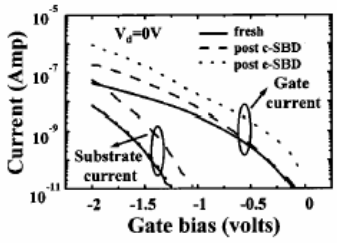

FIG. 3. Gate current and substrate current versus gate bias in *p*MOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

Thus, I_b is enhanced significantly at a positive gate bias in a *c*-SBD device due to localized effective oxide thinning[14,17,18] while I_b in an *e*-SBD device is nearly unchanged. Figure 2 shows the drain bias dependence of the GIDL current before and after SBD. The substrate current has an apparent increase after edge SBD. This is because at a high drain bias the I_b comes from electron band-to-band tunneling in the drain depletion region and the generated holes flow to the substrate. Since the electrical field in the drain region becomes stronger after *e*-SBD due to effectively oxide thinning, the GIDL (I_b) in an *e*-SBD device is enhanced. The same phenomena in *p*-MOSFETs are also observed and the result is shown in Fig. 3.

III. MODES OF SBD ENHANCED HYSTERESIS

Two modes of SBD enhanced body potential alteration are proposed. Figure 4 illustrates two floating-body charging processes in *c*-SBD and in *e*-SBD SOI *n*MOSFETs.[19,20] In a *c*-SBD device with a positive gate bias [Fig. 4(a)], valence band electron tunneling from the channel to the gate is increased after SBD. The generated holes flow to the body and raise the body potential. Figure 4(b) shows the drain-induced floating-body charging in an *e*-SBD *n*MOSFET. Since the

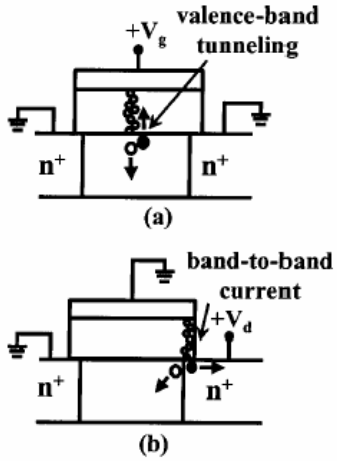

FIG. 4. Illustration of two soft-breakdown enhanced floating-body charging processes in SOI *n*MOSFETs. (a) Soft breakdown in the channel region and hole creation due to valence band electron tunneling; (b) soft breakdown in the drain region and enhanced GIDL current.

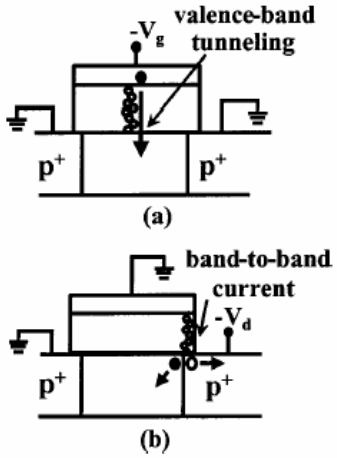

FIG. 5. Illustration of two soft-breakdown enhanced floating-body charging processes in SOI *p*MOSFETs. (a) Soft breakdown in the channel region and valence band electron tunneling from poly-gate to the floating body; (b) soft breakdown in the drain region and enhanced GIDL current.

breakdown path is in the drain edge, the GIDL current increases due to a stronger band bending in the n^+ drain region, thus raising the body potential at a high drain bias. On the contrary, the GIDL current does not change in a *c*-SBD device. Likewise, Fig. 5 shows two possible floating-body charging processes in *p*MOSFETs. Due to the above two charging processes, we conclude that the body potential of both *n*MOSFET and *p*MOSFET can be modified either during gate switching or during drain switching depending on the location of a SBD spot.

IV. RESULTS AND DISCUSSION

Figure 6 shows the $I_{ds}-V_{gs}$ hysteresis in a PD SOI *n*MOSFET before and after *c*-SBD. The measurement drain bias is 0.1 V. The gate bias is swept from 0 V to 1.3 V and then is reversely swept from 1.3 to 0 V. Note that (i) the subthreshold hysteresis before SBD is insignificant and (ii) the post-SBD hysteresis is induced by gate bias sweep in this device. The corresponding body potential fluctuation in gate bias sweep is shown in Fig. 6. The arrow in the figure indicates the direction of bias sweep. After *c*-SBD, the body potential begins to rise when the V_g amplitude is above 0.8 V. The gate switching induced body potential variation

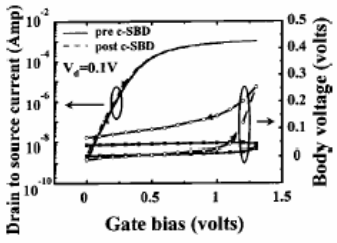

FIG. 6. Hysteresis in I_{ds} and corresponding floating-body potential versus V_g in a *c*-SBD SOI *n*MOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0 V to 1.3 V.

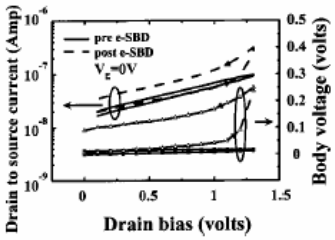

FIG. 7. Hysteresis in subthreshold current and corresponding floating-body potential in an *e*-SBD SOI *n*MOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0 V to 1.3 V.

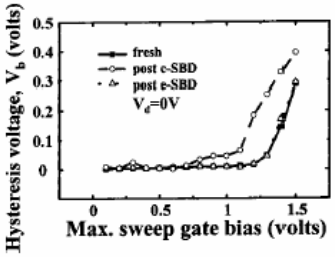

FIG. 8. The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI *n*MOSFETs. V_d=0 V.

can be as large as 0.3 V in this case. The pre-SBD body potential hysteresis at the same switching amplitude is less than a few tens of millivolts. The *c*-SBD induced V_t hysteresis is also observed in a *p*MOSFET. The measurement data are not shown here.

In an *e*-SBD device, although gate enhanced hysteresis is not observed, drain sweep induced hysteresis in subthreshold leakage current is remarkable (Fig. 7). In this figure, the measurement V_{gs} is 0 V and the drain bias is swept from 0 V to 1.3 V and then reversely swept back. The body potential variation is shown in Fig. 7, too. The *e*-SBD enhanced hysteresis effect is clearly shown in this figure. It should be noted these breakdown-induced hysteresis effects occurs in off-state rather than in on-state where hot carrier impact ionization has been reported as a responsible charging mechanism.[5]

The relationship between the magnitude of sweep voltage and the body potential hysteresis in the two SBD modes is investigated. In *n*MOSFETS, the degree of hysteresis in terms of the body potential variation versus the amplitude of the sweep voltage is shown in Fig. 8 for gate bias sweep and

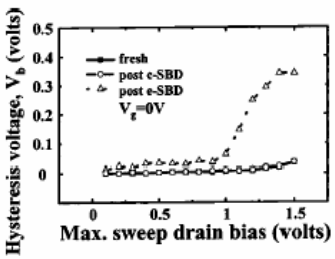

FIG. 9. The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI *n*MOSFETs. V_g=0 V.

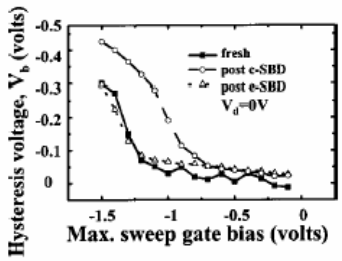

FIG. 10. The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI *p*MOSFETs. V_d=0 V.

in Fig. 9 for drain bias sweep. The hysteresis voltage is defined as the maximum substrate charging voltage during the sweep. In gate bias sweep (Fig. 8), the *c*-SBD device shows an increased hysteresis voltage while the hysteresis voltage of the *e*-SBD device is almost unchanged. In contrast, the *e*-SBD device shows a larger hysteresis voltage in drain bias sweep (Fig. 9). Similar results in *p*MOSFETs are presented in Fig. 10 for gate bias sweep and in Fig. 11 for drain bias sweep. From our characterization, we found SBD induced hysteresis effect may become appreciable even when the supply voltage is below 0.8 V.

The impact of SBD enhanced body charging effect in CMOS operation is described as follows. Figure 12 illustrates the dominant V_t hysteresis modes in a SOI CMOS inverter. Hot carrier (HC) induced floating body charging occurs in on-state[1,5] and it is dominant only when the inverter is during switching. On the other hand, floating body charging takes place in *c*-SBD (*e*-SBD) *n*MOSFETs and *e*-SBD (*c*-SBD) *p*MOSFETs when the input signal is at high (low) state. Since the soft breakdown induced body charging is in the off-state, the time for charging can be much longer than the on-state HC caused body charging. Our study reveals that SBD in PD SOI MOSFETs not only increases leakage current but also affects circuit stability.

V. CONCLUSIONS

The significance of soft breakdown position to V_t hysteresis in PD SOI CMOS devices has been evaluated. Two SBD enhanced hysteresis modes in off-state CMOS are identified. The dominant floating body charging mechanism is valence band tunneling in *c*-SBD devices and band-to-band tunneling

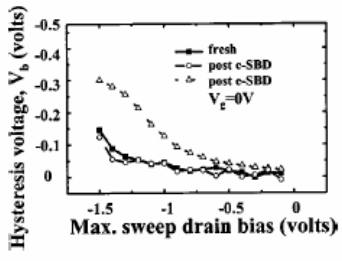

FIG. 11. The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI *p*MOSFETs. V_g=0 V.

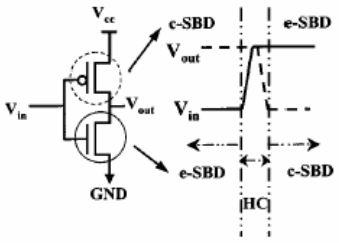

FIG. 12. Illustration of dominant V_t hysteresis modes in the switching of an SOI CMOS inverter.

in *e*-SBD devices. The SBD enhanced hysteresis effect may occur even with supply voltage less than 1.0 V and would be a serious reliability concern in ultrathin oxide PD SOI circuits.

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Comparison of oxide breakdown progression in ultra-thin oxide silicon-on-insulator and bulk metal-oxide-semiconductor field effect transistors

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Enhanced oxide breakdown progression in ultra-thin oxide silicon-on-insulator *p*-type metal-oxide-semiconductor field-effect transistors is observed, as compared to bulk devices. The enhanced progression is attributed to the increase of hole stress current resulting from breakdown induced channel carrier heating in a floating-body configuration. Numerical analysis of hole tunneling current and hot carrier luminescence measurement are performed to support our proposed theory. This phenomenon is particularly significant to the reliability of devices with ultra-thin oxides and low operation gate voltage. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1776640]

I. INTRODUCTION

The aggressive scaling of advanced complementary metal-oxide-semiconductor (CMOS) field effect transistors (MOSFETs) has pushed the gate oxide thickness towards its limit in terms of reliability.[1–4] In ultra-thin gate oxide MOSFETs, oxide breakdown (BD) has been shown to evolve in a continuous manner from initial stages to final shorting.[5–7] Previous study has shown that a small increase in gate leakage due to oxide BD does not disrupt circuit operation, and the failure criterion should be changed to a higher level of gate leakage.[8,9] Therefore, the oxide failure time is determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate. Presently, the silicon-on-insulator (SOI) technology has emerged to be a candidate for advanced CMOS technology for its higher performance. The BD progression in conventional bulk CMOS devices[10–12] has been widely investigated. In this paper, we will investigate the influence of floating body effect on BD progression in partially depleted (PD) *p*-type SOI MOSFETs.

Several concerns of hard breakdown evolution in ultra-thin oxides have been proposed.[7–14] Monsieur *et al.*[7] reported that for low gate stress bias, the defect generation rate being very low, the degradation of the BD conduction path becomes macroscopic and can last thousands of seconds even in the case of accelerated test. Linder *et al.*[9] showed that the growth of BD current could be exponentially dependent on gate bias, oxide thickness, and any other parasitics, such as inversion layer resistances, altering the observed growth rate drastically. Alam *et al.*[13] indicated that circuits do continue to operate after the first soft breakdown (SBD), and suggested that the standard reliability specification is too restrictive, and should be redefined, particularly for pMOS devices. In ultra-thin oxide pMOSFETs, enhanced gate oxide BD growth rate was observed with a negative substrate bias.[14] Furthermore, the floating body configuration of partially depleted SOI CMOS may result in a nonzero body voltage due to various body charging mechanisms[15–18] and thus affects oxide BD evolution. The objective of this paper is therefore to investigate floating body effect on BD progression rate. A model based on breakdown induced channel carrier heating will be proposed to explain the observed phenomenon.

II. DEVICES AND EXPERIMENT

The devices in this work were made with an optimized 0.13 μm CMOS process on *p*-type SOI wafer and have a gate length of 0.5 μm, a gate width of 2 μm, and an oxide thickness of 1.6 nm. The gate oxide was grown with rapid plasma nitridation process. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this paper, all devices were stressed at constant gate voltage with the source and drain grounded. Figure 1 shows typical BD evolution in a 1.4 nm oxide and a 2.5 nm oxide bulk pMOSFETs. In the 1.4 nm gate oxide pMOSFET, oxide BD is evolved in a progressive way, and the gate leakage current increases gradually with stress time. As a contrast, the 2.5 nm oxide pMOSFET exhibits an abrupt jump in gate leakage current after BD. Since a slight gate leakage increases due to oxide BD is considered to be nondestructive for circuit operation,[8] we define oxide breakdown time t_{BD} and device fail time t_{fail}

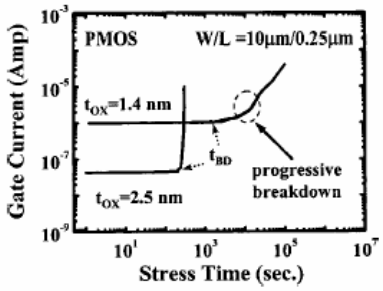

FIG. 1. Comparison of breakdown behavior in a 1.4 nm oxide pMOSFET and in a 2.5 nm oxide pMOSFET. The stress gate voltage is −3 V for the 1.4 nm oxide and −4.5 V for the 2.5 nm oxide. t_{BD} denotes the onset time of oxide breakdown.

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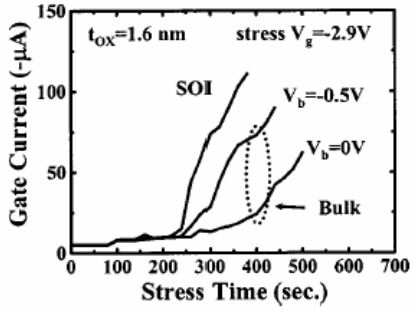

FIG. 2. Oxide breakdown progression in bulk and SOI pMOSFETs. The stress gate bias is −2.9 V and temperature is 125 °C.

as the time when the gate leakage current reaches 1.5 times and 15 times its prestress value, respectively.

III. RESULT AND DISCUSSION

A. A shorter t_{fail} in SOI pMOSFETs

Figure 2 shows the gate leakage current evolution with stress time at a stress gate voltage of V_g=−2.9 V for various applied substrate biases (V_b) in pMOSFETs. The oxide t_{BD} is almost the same for different substrate biases. This can be understood because oxide defect generation rate is dependent on injected charge energy and fluence during stress,[19–22] regardless of applied substrate bias. After the onset of BD, the BD growth rate exhibits an apparent dependence on substrate bias. A forward substrate bias can significantly enhance BD growth rate. It should be noted that the SOI device with floating-body configuration has the worst BD progression rate in Fig. 2. The statistic Weibull distributions of oxide t_{BD} and t_{fail} for SOI (floating substrate) and bulk (grounded substrate) pMOSFETs are plotted in Fig. 3. Although the floating substrate configuration does not affect t_{BD}, it does cause a two times shorter t_{fail} than in bulk pMOSFETs.

B. Mechanism of enhanced BD progression in SOI

The floating body configuration of SOI devices may result in a small forward body voltage due to various body

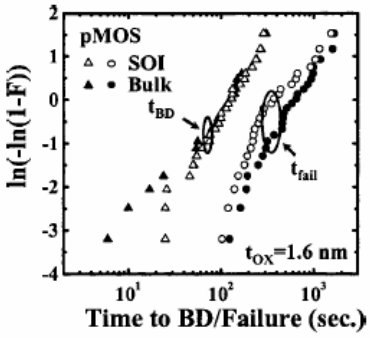

FIG. 3. The Weibull plots of t_{BD} and t_{fail} distribution for 1.6 nm oxide SOI and bulk pMOSFETs. The stress gate bias is −2.9 V and the temperature is 125 °C. t_{BD} and t_{fail} are defined as the time for gate current to reach 1.5 times and 15 times its prestress value, respectively.

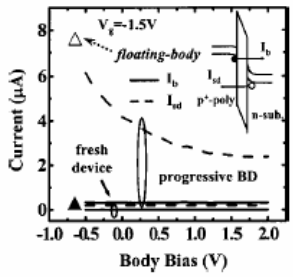

FIG. 4. The V_b dependence of pre-BD and post-BD electron currents I_b and hole currents I_{sd} at V_g=−1.5 V. Distinct V_b dependence of the post-t_{BD} I_{sd} is noted. The floating body configuration corresponds to a body voltage of approximately −0.65 V. The inset illustrates carrier flow in a pMOSFET at a negative gate bias.

charging processes. In an ultra-thin oxide pMOSFET, the gate stress current may have comparable electron and hole components at a negative gate bias. To analyze the polarity of dominant stress current in a pMOSFET, a charge separation technique is utilized to measure electron stress current and hole stress current. The inset of Fig. 4 illustrates the carrier flow at a negative gate bias, I_b denotes electron current and comes from valance-band electron tunneling from the gate electrode. I_{sd} stands for hole tunneling current from the inverted channel. The substrate bias dependence of electron current and hole current before and after t_{BD} is shown in Fig. 4. Note that the electron and hole currents in a fresh device are independent of substrate bias. Interestingly, the post-t_{BD} hole current, unlike the pre-BD, I_b, and I_{sd}, exhibits a significant V_b dependence. Furthermore, Fig. 5 reveals that the V_b dependence of the post-t_{BD} hole current increases with BD evolution. Since the hole stress current dominates gate stress during (BD) evolution and increases with a forward body bias, the enhanced (BD) progression in a floating body configuration can be understood.

C. BD caused carrier heating

Since the post-t_{BD} electron current does not exhibit V_b dependence (Fig. 4), the possibility that the V_b dependence of the post-t_{BD} hole current is caused by the variation of effective gate-to-channel voltage resulting from V_b modulated channel resistance can be excluded. Otherwise, the post-t_{BD} I_b should have the same V_b effect as the post-

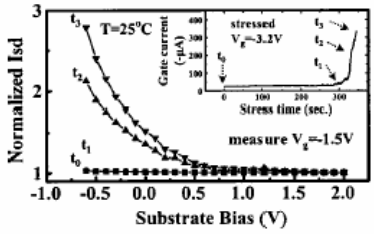

FIG. 5. The V_b dependence of the hole current I_{sd} at different stress times, t_0,t_1,t_2, and t_3. I_{sd} is normalized to its value at V_b=2 V. Gate current vs stress time in a stress condition of V_g=−3.2 V and T=25 °C is shown in the inset.

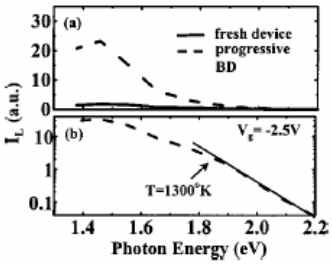

FIG. 6. Spectral distribution of light emission in a 1.4 nm oxide pMOSFET at V_g=−2.5 V. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 K.

t_{BD} I_{SD}. Moreover, substrate impact ionization and negative bias-temperature instability effects are also excluded because the trend of the V_b dependence is opposite.

To further investigate the origin of the V_b dependence of the post-t_{BD} hole current, we measured the spectral distribution of hot carrier light emission before and after t_{BD} (Fig. 6). The light intensity is greatly increased after oxide BD. The high-energy tail of the post-t_{BD} spectral distribution indicates the rise of the carrier temperature. Similar finding was also reported by other groups.[23] The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 K [Fig. 6(b)]. There are two possible theories to explain the rise of channel carrier temperature at a BD spot. First, based on the model proposed by Rasras *et al.*,[23] the gate voltage may penetrate into the substrate after BD and causes lateral field heating of channel carriers. However, this process is unlikely here since the post-t_{BD} electron current and hole current have distinctly different V_b dependence. The second possible reason is that high-dissipated energy, released by valence electrons tunneling from the gate through the BD path, will locally produce a rise of hole temperature. A temperature range of 1000 to 2000 K was estimated in Ref. 24. Electron-hole scattering or Auger recombination is suspected to be the responsible energy transfer process.

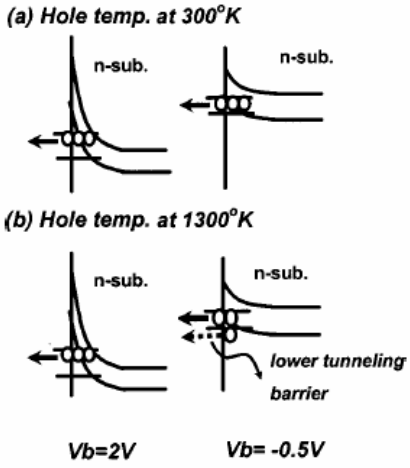

FIG. 7. Illustration of hole distribution in subands at a hole temperature of 300 K and 1300 K. Higher carrier temperature results in a larger V_b effect.

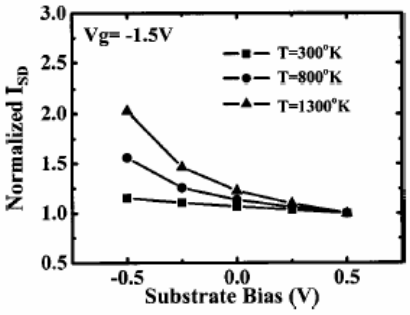

FIG. 8. Simulated substrate bias effect on hole tunneling current in a 1.6 nm oxide pMOSFET. I_{sd} is normalized to its value at V_b=2 V. Simulated V_g =−1.5 V.

To show that the rise of hole temperature may account for the observed V_b dependence, we calculate the hole tunneling current with hole temperature at 300 K and 1300 K. In our calculation, we solve the coupled Poisson and Schrödinger equations to obtain the subband structure for the inversion holes (Fig. 7). A simple one-band effective mass approximation is used for simplicity. The hole tunneling current is calculated according to the Tsu-Esaki formula[25]

$$I_{sd} = qm_{\parallel}^{*}\left(\frac{1}{2\pi^2\hbar^3}\right)k_BT\sum_n D_n(\ln\{1+\exp[(E_n-E_f)/k_BT]\} - \ln\{1+\exp[(E_n-E_{f'})/k_BT]\}), \quad (1)$$

where E_f ($E_{f'}$) denotes the Fermi energy in the channel (poly gate) and D_n is the hole tunneling probability of the nth subband. m^* is the hole effective mass in Si. Other variables have their usual definitions. It should be emphasized that it is not our intention to consider detailed trap-assisted charge transport in the BD path. It is also not our intension to calculate the precise current value before and after oxide BD, since the BD area and BD caused effective oxide thinning cannot be easily determined. Instead, our purpose is to investigate the effect of hole temperature on the inversion hole distribution in different subbands and the corresponding substrate bias effect on hole tunneling current. Therefore, a simple WKB formula for direct tunneling is employed for D_n.

Our result in Fig. 8 clearly shows that the hole tunneling current exhibits a larger V_b dependence at 1300 K. The simulation can well interpret the measured V_b dependence of the

TABLE I. Calculated distribution of channel holes in the lowest three subbands. The gate bias in simulation is −1.5 V. The parameters used in simulation is $m^*(Si)=0.67\ m_0$, $m^*(SiO_2)=0.55\ m_0$, ϕ_h (hole barrier height at SiO_2 interface)=4.25 eV, t_{ox}=1.6 nm, and N_B (substrate doping)=1 $\times 10^{18}$ cm^{-3}.

	Channel hole dist. (%)			
	300 K		1300 K	
Subband	V_b=−0.5	V_b=2	V_b=−0.5	V_b=2
1st	96.6	99.5	39.8	99.4
2nd	3	0.5	18	0.6
3rd	0.3	0	11.6	0

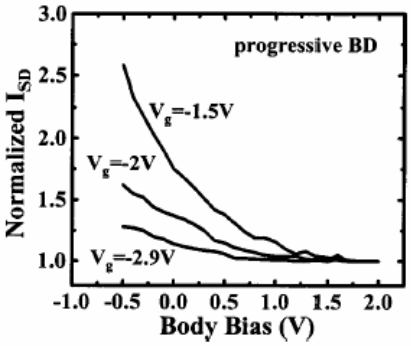

FIG. 9. Substrate bias dependence of the post-BD hole current at various gate biases. I_{sd} is normalized to its value at V_b=2 V.

post-t_{BD} I_{sd} by simply using an elevated hole temperature. The trend in Fig. 8 is similar to the measured V_b dependence in Fig. 5. To explain the temperature effect on the V_b dependence in more detail, the distribution of inversion holes in the lowest three subbands is given in Table I. At T=300 K, channel holes mostly reside in the first subband no matter of V_b. At T=1300 K, a large part of holes are thermally excited to higher subbands at a forward body voltage (−0.5 V), where the oxide tunneling probability is larger. Thus, a much larger hole tunneling current is obtained at negative body voltages.

IV. THE IMPACT OF GATE STRESS BIAS

From previous discussion, the V_b dependence of hole stress current was identified to be the origin of the floating-body enhanced BD progression. Now, the impact of gate stress bias scaling on the enhanced BD progression is explored. Figure 9 shows the V_b dependence of BD current at various measurement gate biases. The V_b dependence is more distinguished at a smaller gate bias. Figure 10 shows the range of the gate stress bias where hole current is dominant. The hole current dominates gate stress at small gate biases (less than ~3.0 V) and the hole component of the stress current increases during BD evolution. This result is consistent with the findings in Fig. 9 that a large V_b dependence of the post-BD stress current is obtained at smaller gate voltages. Figure 11 compares the 63% time-to-failure in

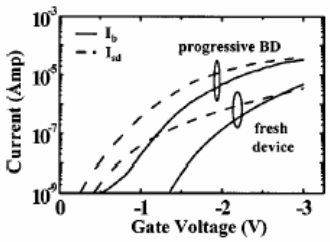

FIG. 10. Gate bias dependence of electron current and hole current in a fresh pMOSFET and during progressive BD.

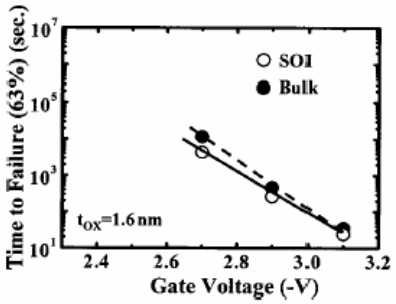

FIG. 11. t_{fail} (63%) vs gate stress bias for SOI and bulk pMOS devices.

SOI and bulk pMOSFETs at various gate stress biases. Accelerated BD progression is noticed in SOI samples and the trend becomes more apparent at lower gate stress biases. Figure 12 shows the range of oxide thickness and stress gate voltage, where the hole current component is dominant in a fresh device and after breakdown. For example, for an oxide thickness of 1.6 nm, hole current is dominant in stress for V_g<2.5 V in a fresh device and for V_g<3.0 V after BD. High-energy electron impact ionization does not need to be considered until V_g is above 3.5 V. Figure 12 also reveals that the hole current dominant region increases not only with BD progression but with decreasing oxide thickness. It implies that the floating body enhanced BD progression will become more significant as oxide thickness scales down.

V. CONCLUSION

In ultra-thin oxide SOI pMOSFETs, breakdown progression is aggravated by a forward body bias. An enhanced post-t_{BD} gate current is observed in SOI devices due to the charging of the floating body. Numerical analysis shows that the V_b enhanced hole stress current can be explained by the increase of hole temperature at the breakdown spot. The V_b accelerated BD progression is more significant at a lower stress gate bias and for a thinner oxide.

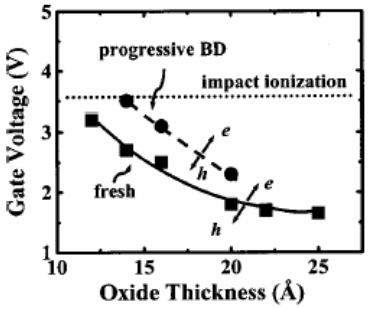

FIG. 12. The range of oxide thickness and stress gate voltage, where the hole current component is dominant in a fresh device and after breakdown *h* or *e* represents hole current or electron current dominant regime, respectively.

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出席國際會議心得報告

本計畫研究成果發表論文共八篇，包含國際會議論文有三篇。其中兩度於半導體可靠性物理領域權威會議的國際可靠性物理年會（IRPS）發表論文，另一會議為日受國際重視、每年於日本舉行之國際固態電子元件與材料會議（SSDM）。

[A] IRPS： 參與學生：陳旻政

2003 年國際可靠性物理會議(2003 IEEE International Reliability Physics Symposium Proceedings)簡稱 2003 IRPS，為半導體可靠性物理方面之最知名的國際性會議，其主要乃是專精於半導體元件、電路及製程研究方面。與會人士達數百人，國內學術界與工業界皆有代表參與該會議。

其議程如下: (1)BEOL Dielectrics (2)Circuits (3)Compound Semiconductors (4)Device and Process (5)Device Dielectrics (6)ESD (8)Failure Analysis (9)Gate Dielectric (10)High K Dielectrics (11)Interconnects (12)Latch-up (13)Late News Papers (14)Memory (15)MEMS (16) Packaging (17)Product Reliability (18)SER (19)SiGe (20)Transistors, 本計畫所發表的論文與IBM, Agere, IMEC, STM等公司同一於Session（Gate Dielectrics）。

攜回資料包括 2003 年 IRPS 會議論文集一本以及光碟一片。

學生此次出國參加會議，深深覺得國內半導體方面的研究，無論研究規模和論文質與量每年均有進步，然而比起美國與日本等國仍然還有一段的差距。目前國內學術界應該獎勵基礎理論的研究發展，而工業界應該鼓勵參與國際工程研發的創作，而使國家整體半導體界趨於世界一流水準。然而，現今國內發表論文於期刊的風氣日盛，而參與國際性會議型論文發表卻遠遠落後美日先進半導體國家。如何能急起直追，而超越先進國家。這可能需要透過獎勵出國發表論文，才能更進一步的提昇國內半導體於國際的知名度。

[B] SSDM： 參與學生：詹前泰

本次會議議程一共四天，九月十四日至九月十七日，九月十四日為大會安排之課程，因全程使用日文，故吾人並未參加，九月十五日至十七日則為各領域之會議報告。此外，九月十六日下午於展示廳舉辦 poster exhibition，讓無法排入口頭報告議程之論文能藉此機會發表成果。大會安排吾人於十六日下午五點四十分，Session C-6: SOI- Device Characterization 中報告。報告時間為十五分鐘，五分鐘的時間開放提問。由於吾人準備充分，報告十分順利。此外，吾人亦參加與目前研究領域相關之會議，如 high-k gate dielectrics, oxide reliability…等等，接觸目前最新之研究成果。此為吾人首次出國參加會議，與國內會議最大之不同即為語言。由於吾人英文能力極佳，會議上皆能順暢地與國外學者交換意見。值得一提的是任教於東京大學電子工程系（The University of Tokyo，Dep. Of Electronic Engineering）的國際知名學者高木信一（Shinichi Takagi）教授會中曾向吾人提問，吾人並於會後與高木教授進行長達將近十五分鐘之更深入討論與交談，並與之交換名片；高木教授為理論方面知名專家，能有此機會與之交流，為此次會議一大收穫。

本篇論文獲 Marubun Research Promotion Foundation 評選為年輕研究人員獎勵名單之一，大會數百篇論文僅十四篇獲獎，本篇論文為台灣地區兩篇論文之一。

攜回資料包括 2004 年 SSDM 會議論文集一本、光碟一片以及 Marubun Travel Grant Award 紀念牌一面。