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高介電常數閘極介電層材料製備與可靠性分析

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高介電常數閘極介電層材料製備與可靠性分析
Preparation and characterization of high-K gate dielectric materials

Abstract

HFO_2 is a promising alternative for replacing SiO_2 in ULSI manufacturing. In this work, we employ different gas plasma, i.g. N_2O, NH_3, and N_2, to nitrify the HfO_2 films in order to obtain less bulk traps responsible to threshold voltage instability. In this work, we found that HfO_2 film with N_2O plasma nitridation exhibits excellent properties, such as lower swing, higher conductance and driving current. This is due to the N_2O plasma nitridation can reduce interface states and bulk traps in the HfO_2 film, confirmed by using charge pumping technique1) with different measurement method, i.e. fixed base, fixed peak and fixed amplitude method.

Keywords： bulk trap, charge pumping, nitridation, HfO_2

Introduction

Charge trapping is an important concern in the CMOS devices with HfO_2 gate dielectrics, due to the large amount of bulk traps presented in the HfO_2 films. Their presence can result in the reliability degradation,[2)] mobility degradation[3-7)] and threshold voltage instability[8-12)]. In order to improve the film quality, a variety of nitridation techniques were used to incorporate nitrogen into the high-k films.[4,9-11)] In this work, we utilized the N_2O plasma treatment following the HfO_2 deposition, which possesses the advantage of low thermal budget for preventing the HfO_2 films from crystallization during processing. It was found that the post-deposition N_2O plasma treatment can not only effectively improve the electrical characteristics of the pMOSFETs with the HfO_2 gate stack, such as lower bulk traps, interface states, mobility and the resultant higher driving current, but also reduce the gate leakage current substantially.

Experimental

The pMOSFETs were fabricated on n-type (100) 150 mm wafers. After conventional LOCOS isolation, standard RCA cleaning with a final HF-dip was performed, followed by the growth of an intentional 0.6nm thin interfacial oxyntride layer (SiON) using rapid thermal processing in a NO_2 ambient at 700°C. Subsequently, an approximately 3nm HfO_2 layer was deposited by atomic vapor deposition (AVD) using an AIXTRON Tricent® system at a substrate temperature of 500°C. The physical thicknesses of the SiON layer and HfO_2 film were measured by the optical n&k analyzer. After deposition of the HfO_2 films, some samples were subjected to an additional N_2O-gas, NH_3-gas or N_2-gas plasma treatment at the substrate temperature of 300°C. Then, all samples were annealed in a N_2 ambient at 600°C for 30s in order to improve the film quality. A 250nm polycrystalline silicon (poly-Si) layer was directly deposited by low pressure chemical vapor deposition (LPCVD) on top of the HfO_2 films, and then the gate electrode patterning was implemented through lithography and etching processing. Subsequently, the extension and deep source/drains were formed by implantation, which dopants were activated at 950°C with rapid thermal annealing (RTA) for 20s in a N_2 atmosphere. After passivation, contact holes formation, Al metallization and patterning, the forming gas annealing at 400°C was finally performed for 30minutes.

Fig. 2 and 3 shows the gate leakage current of PMOSFET with HfO2 gate stack subjected to various post-deposited plasma treatment under inversion and accumulation region, respectively. The gate leakage current could be reduced by N_2O plasma treatment both at inversion and accumulation region, especially at inversion region, reduction can be achieved two order magnitude.

Fig. 4 shows the typical C-V characteristics of HfO_2 gate stack with various plasmas treatment. It can be clearly found that the capacitance of C-V curves at strong inversion is lower than that at strong accumulation region, which is due to the poly depletion effect. In addition, the hump occurs at the depletion region for all samples. This may be due to the interface states and it seems the N_2O-treated sample exhibits no significant hump. Fig. 5 shows the EOT extracted from strong inversion for HfO_2 gate stack with various plasma treatment. The EOT for N_2O-treated sample increases, but for NH_3-treated and N_2-treated samples decrease. The slightly EOT for N_2O-treated sample may be one of the reason for reduced leakage current.

The values of subthreshold swing of pMOSFETs with HfO_2 gate stack objected various plasma treatment. It can be found that N_2O plasma-treated sample shows smaller swing resulted from lower interface states. However, the degradation of swing are observed for NH_3-treated and N_2-treated samples. This may be due to the ion bombardment from the plasma.

The influences of various plasma treatments on the driving current of the pMOSFETs with HfO_2 gate stack. The driving current can be enhanced by post-deposited N_2O plasma treatment for HfO_2 gate stack with higher EOT. Those results may be ascribed to lower interface states and higher normalized transconductance, as shown in Fig.7. However, the higher driving current for NH_3-treated and N_2-treated samples is attributed to smaller EOT values.

In order to gain into investigations of the improvements for N_2O-treated samples, the charge pumping measurements are used to analyze the interface states and bulk traps in the dielectrics. Recently, the CP measurement had been frequently employed to qualify the level of bulk traps 12,13) in the HfO_2 dielectrics using the fixed base sweep and/or the fixed peak sweep, as indicated in Fig. 8(b) and Fig. 8(c), respectively. The measured results of charge pumping measurements are shown in the Figure 9. We can find that the interface states and bulk traps 12,13) in the HfO_2 dielectrics can be reduced by the post-deposition N_2O plasma treatment, resulted in the higher driving current and lower interface states even that it has higher EOT.

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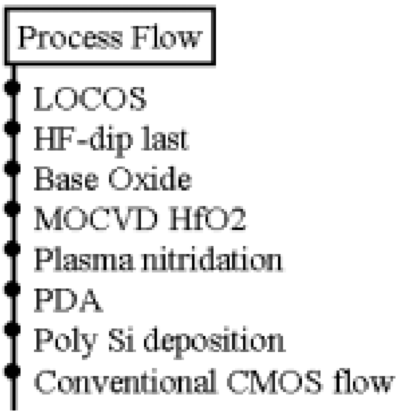
Process Flow

- LOCOS
- HF-dip last
- Base Oxide
- MOCVD HfO2
- Plasma nitridation
- PDA
- Poly Si deposition
- Conventional CMOS flow

Fig.1 Process flow of HfO_2 pMOSFET。

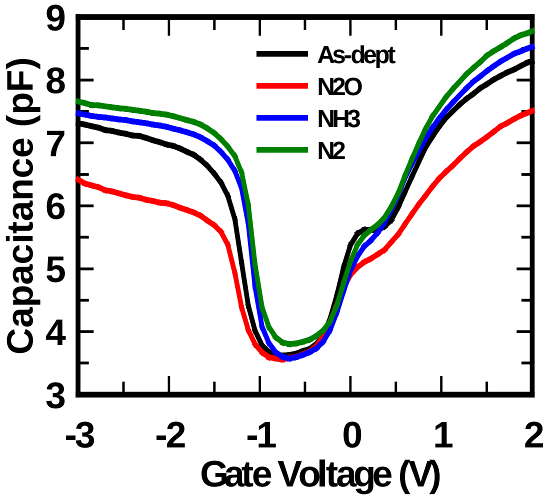

Fig. 4 CV characteristics of HfO_2 pMOSFET for various plasma treatments.

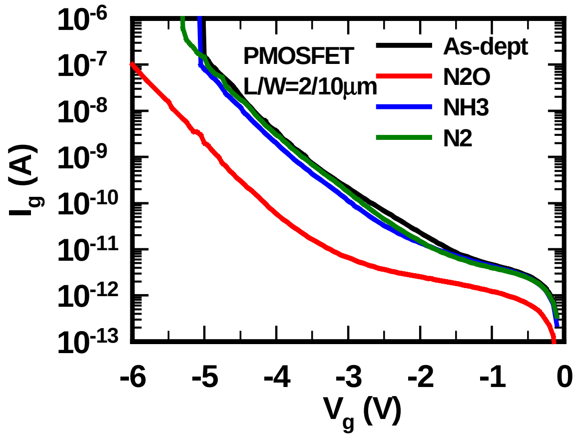

Fig. 2 The gate leakage at inversion region for various gas plasma treatments.

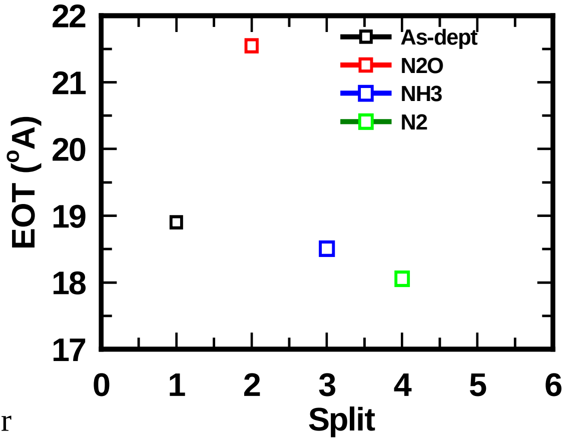

Fig. 5 The EOT values of HfO_2 gate stack with various plasma treatment.

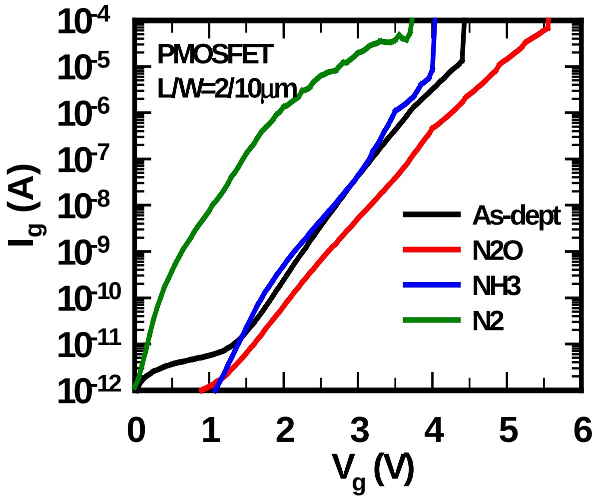

Fig. 3 The gate leakage at accumulation region for various gas plasma treatments.

Method	As-dept	N_2O	NH_3	N_2
Swing value	~81	~76	~87	~87

Table. 1 The swing values of HfO_2 gate stack with various plasma treatment.

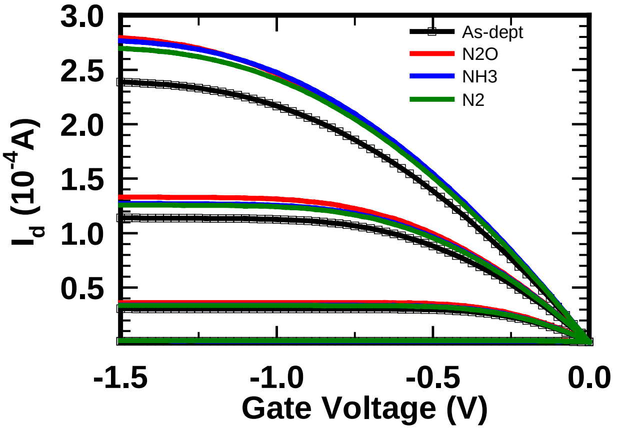

Fig. 6 The output current of HfO_2 gate stack with various plasma treatment.

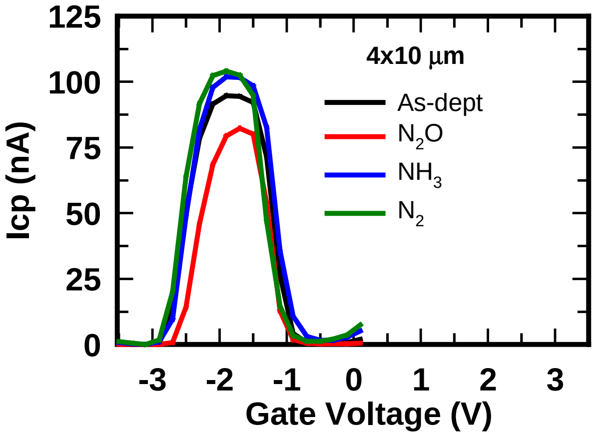

Fig. 9(a) Charge pumping current measured by Fixed amplitude Method.

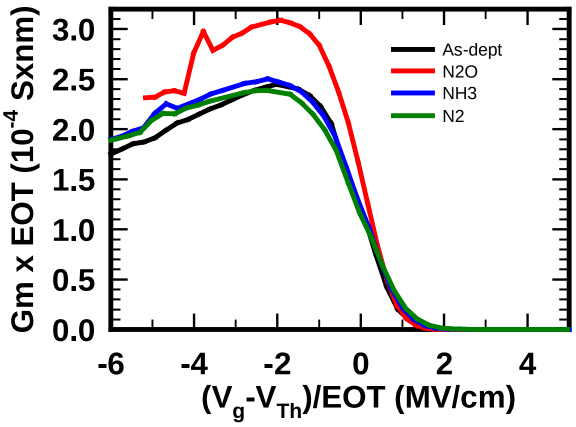

Fig. 7 The normalized Gm of HfO_2 gate stack with various plasma treatment

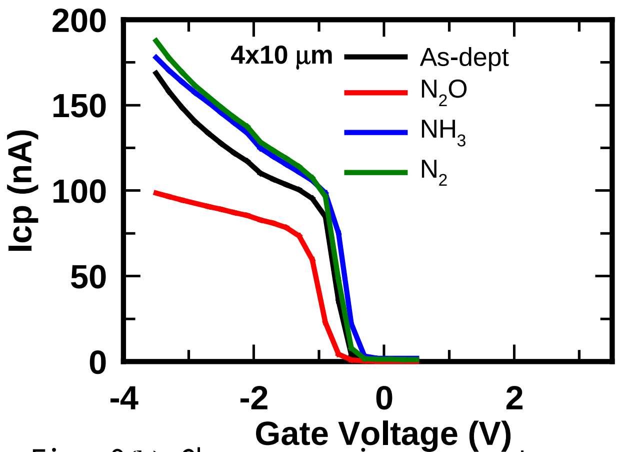

Fig. 9(b) Charge pumping current measured by Fixed peak Method.

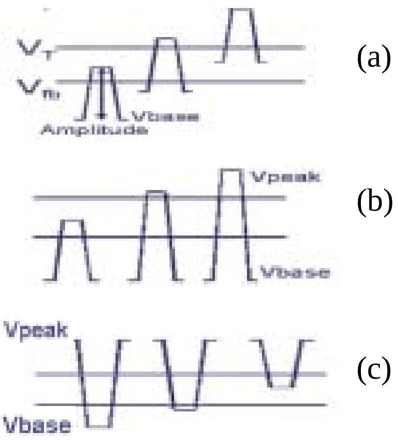

Fig. 8 The methods of various charge pumping measurements.(a) Fixed amplitude (b) Fixed Base (c) Fixed peak。

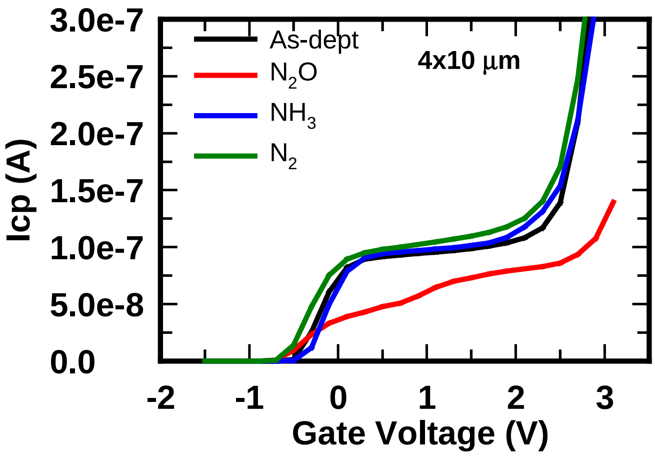

Fig. 9(c) Charge pumping current measured by Fixed base Method.