# 行政院國家科學委員會專題研究計畫　成果報告

## 子計畫八：以微機電技術開發應用於高密度波長多工通訊網路之光切換元件研究(3/3)

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**Abstract**

In this project, a novel fabrication technology using self-aligned multi-layers SOI process is developed to greatly simplify the existing SOI-MEMS fabrication methods in manufacturing MEMS devices. The present fabrication method consists of two major processing steps: (1) Nitride and polysilicon were deposited on SOI wafer with only four masks aligned to construct additional dielectric and structural layers; (2) Oxide is deposited to seal the trench created by first step for the purpose of connecting contact pads and continuing additional fabrication process if needed. A dual comb-drive actuator was fabricated based on the developed process. The actuator is capable of elevating 250 nm vertically with 30 V applied voltage. The dynamic characteristics of the first and the second resonant frequency of the dual comb-drive actuator are 10.5 KHz and 23 KHz respectively. Experimental results indicated that the measured data agreed well with simulation results using the *ANSOFT Maxwell® 2D field simulator*, *ANSYS®* and *Coventor Ware®*.

**中文摘要**

本計畫中，一種可以大大減簡化目前 SOI-MEMS 的新製程技術，已被發展出來。此新技術是使用自動對準的多層 SOI 製程。在本製程中，經由氮化矽以及多晶矽沈積在 SOI 晶片以及四道光罩的對準上製作出額外的界電層以及結構層。利用此製程技術，雙梳狀結構的致動器已被製造完成。在 30 伏特的驅動電壓下，此致動器可達成 250 奈米的垂直移動。此致動器的第一以及第二共振頻率分別為 10.5 千赫以及 23 千赫。實驗的量測數據顯示實際的測試結果與利用 *ANSOFT Maxwell® 2D field simulator*、 *ANSYS®* 以及 *Coventor Ware®* 的模擬結果是一致的。

**關鍵詞**：微機電系統、雙模梳狀致動器

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# 行政院國家科學委員會專題研究計畫成果報告
## 以微機電技術開發應用於高密度波長多工通訊網路之光切換元件研究
## The Study of MEMS Based Optical Cross-Connect Device for DWDM

計畫編號：NSC 92－2215－E－009－009
執行期限：92 年 8 月 1 日至 93 年 7 月 31 日
主持人：邱俊誠教授 交通大學 電機與控制工程學系

### Introduction

High-performance MEMS device can be fabricated and applied widely that heavily dependent on reduced complicated fabrication steps to enhance the reliability and yields of fabricated devices. Of the existing MEMS devices, scanning mirror and accelerometers are thought to be the most important micromachined devices for optical and navigation applications. Here the issues of high aspect ratio in proof mass in accelerometers and uniform flat structure in scanning mirror that is a factor determined the performances of the manufactured devices. Due to the limitations of material residual stress of deposited film and deposition thickness, traditional surface micromachining technology cannot satisfy above-mentioned requirements. SOI-MEMS process has attracted increasingly interests recently as a main fabricating method to overcome the drawbacks of above-mentioned MEMS applications [1-7]. Furthermore, optical devices such as scanning mirror, devices may required to possess large deflection angles or large actuation forces characteristics with multi-directional/axis motion and good reliability [6,10]. For such applications, single-crystal silicon microstructures and three-dimensional processes for fabrication of polysilicon microstructures have been previously demonstrated [1-11]. However, the multi-polysilicon process [10] and polysilicon trench-refill process [11] are not capable of producing thick and long suspending structures to carry out desired motions. The reason is that the residual stress producing by deposited material limits the stability and application of fabrication process. Furthermore, the previous single-crystal silicon microactuators process is only capabilities of producing lateral or rotation motions [1-4, 6-8]. This limitation is due to the fact that there is no isolation to construct additional dielectric and structural layers. With the isolation layers and structural layers, the comb drive fingers design can be separated to obtain different electrode sets, which have the capability to produce multi-directional/axis motions. Moreover, these fabricating methods were so complicated that they can easily produce asymmetric and unreliable driving structures. For example, by fabricating upper and lower comb-finger structures individually, Comant and Lee proposed boning technology to bond both comb-finger structures. The misalignment during the bonding process may easily produce asymmetrical actuation [1,8]. Fabrication methods proposed by [4-7] using bonding and polish technology, special SOI wafer with backup mask and reflow photoresist assembly method can easily resolve the drawbacks observed in the above-mentioned surface micromachining processes. However, these complicated processes reduced the repeatability and yield for realistic

manufacture.

The major drawback of the current SOI-MEMS technology is that there exists only one structure layer such that additional structure layer or connecting wire between two electrodes cannot be produced. The reason is that it is hard to re-apply photolithography upon the completion of the high aspect-ratio single-crystal silicon structure.

In this project, a novel fabrication technology using self-aligned multi-layers SOI process is developed. The fabrication method consists of two major processing steps: (1) Nitride and polysilicon were deposited on SOI wafer with only four masks aligned to construct additional dielectric and structural layers; (2) PECVD oxide is deposited to seal the trench created by first step for the purpose of connecting contact pads and continuing additional fabrication process if needed. Multi-poly layer process like well-known MUMPS can further be processed over the oxide sacrificial layer. Therefore, we are able to manufacture MEMS devices that cannot be fabricated using existing fabrication processes.

In this project, the comb fingers with self-aligned and patterned were completed in a successive etching process and simultaneously separate upper and lower electrodes without critical alignment. It not only greatly simplifies the previous fabricating process but also provides a solution to create multi-directional actuators that will be introduced in the proceeding section.

## Fabrication Technology

*A. Self-Aligned SOI Process*

The present process based on SOI wafer consisted of four photolithography masks: three front side etching masks for contact window, metal pads and ICP etching, and one backside etching mask to release the designed structures. The fabrication processes are schematically depicted in Fig.1. The present process used a high doping SOI wafer with 15μm device layer (0.01~0.005Ω／square) , 3μm buried oxide and 450um substrate. At first, a thin layer of thermal oxide 0.2um and LPCVD nitride 0.5um are deposited on the wafer. In order to protect existed thermal oxide and nitride from front side etching, photoresist is spun on the backside wafer. Here, these deposited layers will be used as a mask for backside anisotropic etching. As illustrated in Fig. 1a, a 0.1μm thickness of silicon nitride and a 2μm thickness of high doping polysilicon are deposited on SOI wafer using LPCVD. The silicon nitride (200~400MPa) and polysilicon can be used as an insulation layer and structure layer. LPCVD polysilicon layer is deposited at 585±5℃ through POCL3 diffusion and 1050℃ 30 min. annealing that produced residual stress less than 100MPa. The polysilicon sheet resistance less than 1Ω／square was measured. Note that, the thickness of polysilicon can be altered depending upon the designed requirements. In other words, the LPCVD method can be replaced by epitaxial method if thicker polysilicon is need. Then, STS ICP and RIE are used to etch polysilicon and silicon nitride respectively. The purpose of the above-mentioned etching steps is to create upper and lower contact-windows so that electrodes of device layer and polysilicon can be patterned simultaneously (Fig. 1b). As shown in Fig. 1c, the Cr/Au layer is deposited and patterned on device layer and polysilicon to form connecting pads. In Fig. 1d, the device-nitride-polysilicon layer is patterned and etched by interchanging STS ICP

and RIE. By changing these etching machines, we are able to use one-mask-alignment to etch polysilicon, nitride and single crystal silicon consecutively. Note that regardless fixed or moving structures / upper or lower electrodes, the present step can be accomplished all in one mask. The advantage of the present step is to construct the fixed and moving structures with upper and lower electrodes all in one mask. As illustrated in Fig. 1e, in order to etch LPCVD nitride and thermal oxide using RIE, the fourth mask is used on the backside of the wafer. Anisotropic etching is applied to etch silicon-substrate using KOH solution where etching stop will be occurred at buried oxide. To avoid KOH attacking, a clamped apparatus is used to protect the front side silicon. Backside etching provides larger motion space for the device and decrease squeeze-film effect. In the final step, HF is used to etch buried oxide below the comb fingers and structures. Note that the present backside etching and HF etching steps can be completed uses both traditional wetting etching or dry etching. To prevent the side sticking of comb fingers produced in HF released step, CO2 critical point dryer is used. Note that in the present self-aligned SOI process, the thickness of device-nitride-polysilicon layer can be altered depending on the characteristic of designed devices.

*B. Trench-sealed process*

Since it is hard to re-apply photolithography upon the completion of the high aspect-ratio single-crystal silicon structure so that additional structure layer or connecting wire between two electrodes cannot be produced. Trench-sealed process is developed to overcome this difficulty. The main focus of the present step is to produce a non-conformal coating characteristic. Here PECVD is applied due to the fact that the deposition pressure is larger than LPCVD in such case short mean free path of reaction gases is obtained. In the present process, 7um PECVD oxide is deposited on the previously fabricated 3um trench high-aspect ratio structures. Here, the oxide is acted as a sealing material and sacrificial layer with additional structure layer can be deposited and released easily in mind. By comparing LPCVD and PECVD in term of deposition rate and material property, we observe that the sealing process in PECVD is better than the refilling process in LPCVD. Thus with the same deposition time frame, PECVD is able to produce flat surface faster than LPCVD. With the present sealing process, we are able to deposit additional layers like the well-known MUMPS process.

## Application Example: Dual comb-drive actuator

A dual comb-drive actuator with a pair spring beam is shown schematically in Fig.2. The comb fingers consist of three structure layers including polysilicon, nitride and single crystal silicon. The fixed and moving comb fingers are separated upper (*V1, V4, V5*) and lower (*V2, V3, V6*) electrodes by nitride layer. The electrodes of the dual comb-drive actuator are divided into six individual contacting pads that are able to produce multi-directional motion. As shown in the Table 1, when voltage is applied between electrodes *V1*, *V2* and *V5*, the imbalance of the electric field distribution results in a vertical induced force. And consequently, moving comb fingers enable upward motion. On the other hand, when voltage is applied between electrodes *V3*, *V4* and *V6*, moving comb fingers enable downward motion. If we apply voltages between *V1, V3* and *V2*,

*V4*, or *V5*, *V6* and *V2*, *V4*, moving comb fingers produce horizontal motion like a lateral-axis comb drive [13]. Furthermore, by applying voltage between *V1*, *V2* or *V6*, *V4*, the structure with moving comb fingers can convert vertical force to clockwise rotation directly. On the contrary, by applying voltage between V5, V2 or V3, V4 that could produce counterclockwise rotation. The simulation results are shown in Fig.3.

Note that, vertical comb-drive actuator with limited displacement is determined by the device layer thickness [12]. The larger thickness of the comb fingers, the more vertical displacement it will produce. In order to evaluate the relationship between voltage and displacement, force balance equation is needed in the present analysis. The electrostatic energy that is used to deflect the actuator is converted to mechanical potential energy. When a voltage is applied between the upper and lower electrodes, the electrostatic force $F_e$ is given by [11, 13]:

$$F_e = \frac{NL}{2}\frac{\partial C}{\partial z}V^2 \tag{1}$$

where *N* is the number of pairs of comb fingers ,*L* is the overlapped length of fixed and moving comb fingers, *C* is the capacitance between the separated electrodes, *z* is the displacement along the actuation direction, and *V* is the applied voltage. By using the *ANSOFT Maxwell® 2D field simulator*, the relationship of capacitance and displacement of the two sidewall capacitors, *C12* and *C34*, i.e. up-capacitor and low-capacitor can be evaluated respectively. According to this relationship, the gradient versus static vertical displacement can also be determined. In the present simulation, the thicknesses of upper and lower electrodes are 2um and 15um thickness with 3um comb finger gap. Fig.4a and 4b are used to show the simulation results of the capacitance versus displacement and the gradient capacitance gradient versus displacement respectively. The maximum displacement is obtained by the intersections of two gradient curves with the z-displacement axis, which occur at –4.14 um and 4.14 um. For a given input voltage, the electrostatic energy ($F_e$) is equal the mechanical energy ($F_m$) stored in the device. The relationship between displacement and applied voltage can be obtained by solving the force balance equation:

$$F_e = F_m = kz \tag{2}$$

where *k* is the spring constant. The result is plotted in Fig.4 (c) for vertical motion of the dual comb-drive actuator with 272 pairs comb fingers. Furthermore, when driving voltage increases, different spring constants will still produce saturated displacements at –4.14 um to 4.14 um.

## Fabrication Results

The proposed self-aligned multi-layers SOI process has been employed to fabricate the dual comb-drive actuator, which is capable of creating piston motion. Figure 5a and 5b show SEM pictures of front and backside of the fabricated dual comb-drive actuators. The dimensions of the designed device included a suspending membrane (1*1 $mm^2$), eight 600um long, 10 um high and 10 um wide springs, and 272 pairs of comb fingers (200 um long, 5 um wide) with 2 um gap. The oblique view of the comb fingers from bottom to top composite of single-crystal silicon; nitride and polysilicon that is shown in Fig. 6a and 6b. The measured dimensions of the

fabricated device of each comb fingers width, air gap and spring width are 3.8um, 3.2um and 9.2um respectively. Fig. 7a and 7b show another device that is the dimensions of the designed device included a suspending membrane (1.5*1.5 $mm^2$), eight 600um long, 10 um high and 10 um wide springs, and 428 pairs of comb fingers (200 um long, 6 um wide) with 2 um gap. The measured dimensions of the fabricated device of each comb fingers width and air gap spring width are 4.32um and 3.44um respectively. The fabrication errors are due to photolithography inaccuracy and ICP undercut effect. The structure is constructed by single-crystal silicon with curvature at 5.7m (Fig. 8a). However upon a 0.2 um thickness gold film has deposited on the suspending structure, the curvature has decreased to 0.83m (Fig. 8b).

A test structure is fabricated to demonstrate trench-sealed technology. PECVD is used to deposit oxide on comb structures with 3um width and 40um trench depth that is fabricated by ICP process. Fig. 9a shows the cross-section of the trench-sealed process. By observing the SEM picture, less 4um thick of PECVD oxide is able to seal a 3um trench window well. To verify the concept of depositing additional layers as in MUMPs process, a second polysilicon layer with 1 um thick is deposited on the existed PECVD oxide by using LPCVD. As shown in Fig. 9b, the flatness of the deposition surface proved that we are able to continue our photolithography to construct additional structure or sacrificial layers. The surface roughness upon the completion of the trench-sealed and LPCVD polysilicon processes is less 0.6um.

## Experimental Results

The test device used in the experiments was designed and fabricated to actuate in z-axis. Eight spring beams that eliminated x-y motions are used to support the suspending structure. As shown in Fig. 10, Laser Doppler Vibrometer (LDV) is used to measure the dynamic characteristics of the dual comb-drive actuators. The first resonant frequency of the device is 10.5 KHz in vertical mode and the second resonant frequency is 23KHz in tilting mode. The corresponding simulations are carried out using *ANSYS*® simulation software. The resonant frequencies of vertical mode and tilting mode are 9.83 KHz and 23.3 KHz (Fig.11). The spring constant of fabricated devices is 180 Nt/m measured by nanoindentor. The displacement-voltage curve for the device is shown in Fig. 12. The simulation data fit the theoretical prediction well. However, in comparison with Coventor Ware simulation software and theoretical calculation to the dynamic experimental results measured by LDV in 4 KHz, a 6.4% RMS error is obtained. By using LDV, the actuator can achieve a 250nm vertical motion at a driving voltage of 30 V.

## Conclusions

This project has reported a self-aligned multi-layers SOI process for MEMS applications. This technology provides several important features such as fixed or moving structures / upper or lower electrodes can be fabricated all in one mask and trench seal technology for further additional deposition layers that enhance yield and variety for high-performance MEMS devices. Furthermore, according to designed requirements, suitable SOI wafer and polysilicon thickness can be used to avoid existing complicated fabrication technology that produce fabrication fault.

Using the proposed fabrication methodology, we are able to manufacture various high-performance and various MEMS devices such as optical phase modulator, micro-interferometer, and scanning mirror.

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## Project result evaluation

In this project, a novel fabrication technology using self-aligned multi-layers SOI process is developed to greatly simplify the existing SOI-MEMS fabrication methods in manufacturing MEMS devices. Based on the developed processes, a dual comb-drive actuator was fabricated. The comb fingers with self-aligned and patterned were completed in a successive etching process and simultaneously separate upper and lower electrodes without critical alignment. The proposed dual comb-drive actuator not only could achieve rotation motion but also could attain piston motion. By applying this actuator and the developed fabrication processes, we are able to manufacture various high-performance and various MEMS devices such as optical switch, optical phase modulator, micro-interferometer, and scanning mirror. Hence, we did practically achieve the project goal.

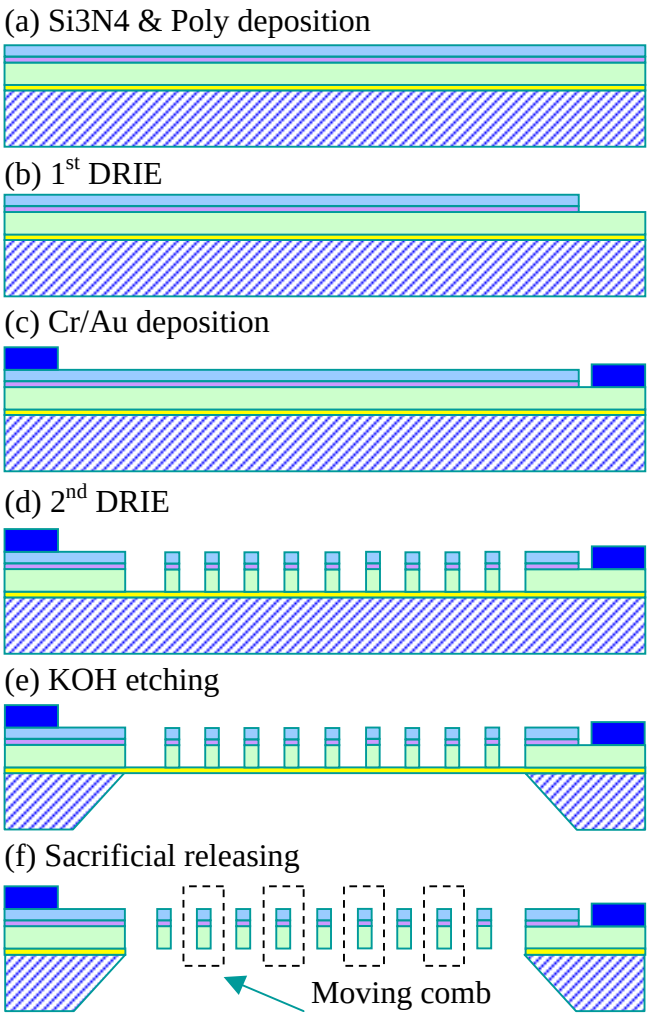



Fig.1 Schematic fabrication processes flow

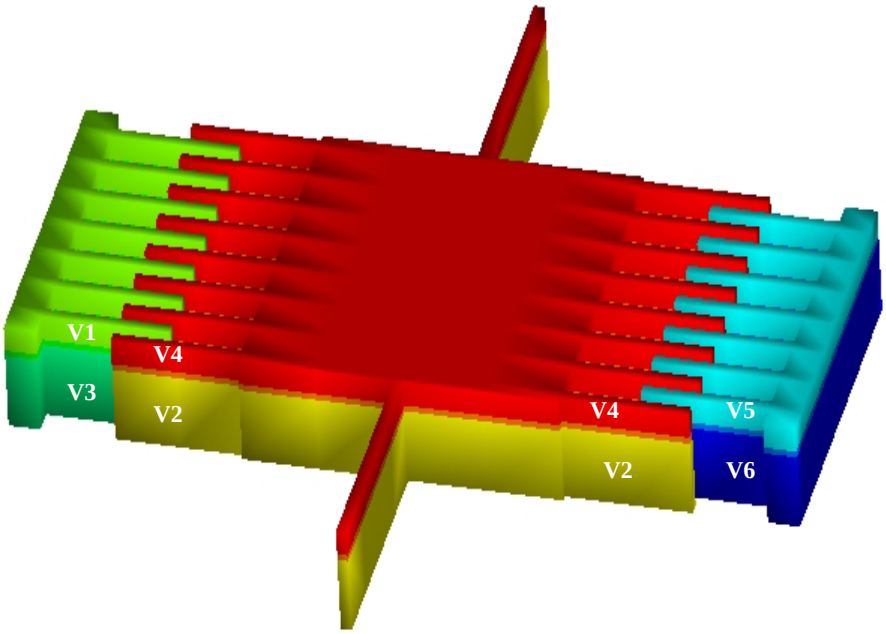



Fig.2 Schematic structure of dual comb-drive actuator

Tab.1 Multi-directional motion principles: (a) upward motion;
(b) downward motion; (c) horizontal motion; (d-e) rotational motion

| | Electrode | V1 | V3 | V5 | V6 | Motion |
|---|---|---|---|---|---|---|
| (a) | V2 | + | − | + | − | ↑ |
| (b) | V4 | − | + | − | + | ↓ |
| (c) | V2&V4 | + | + | + | + | ← → |
| (d) | V2&V4 | + | − | − | + | ↷ |
| (e) | V2&V4 | − | + | + | − | ↶ |

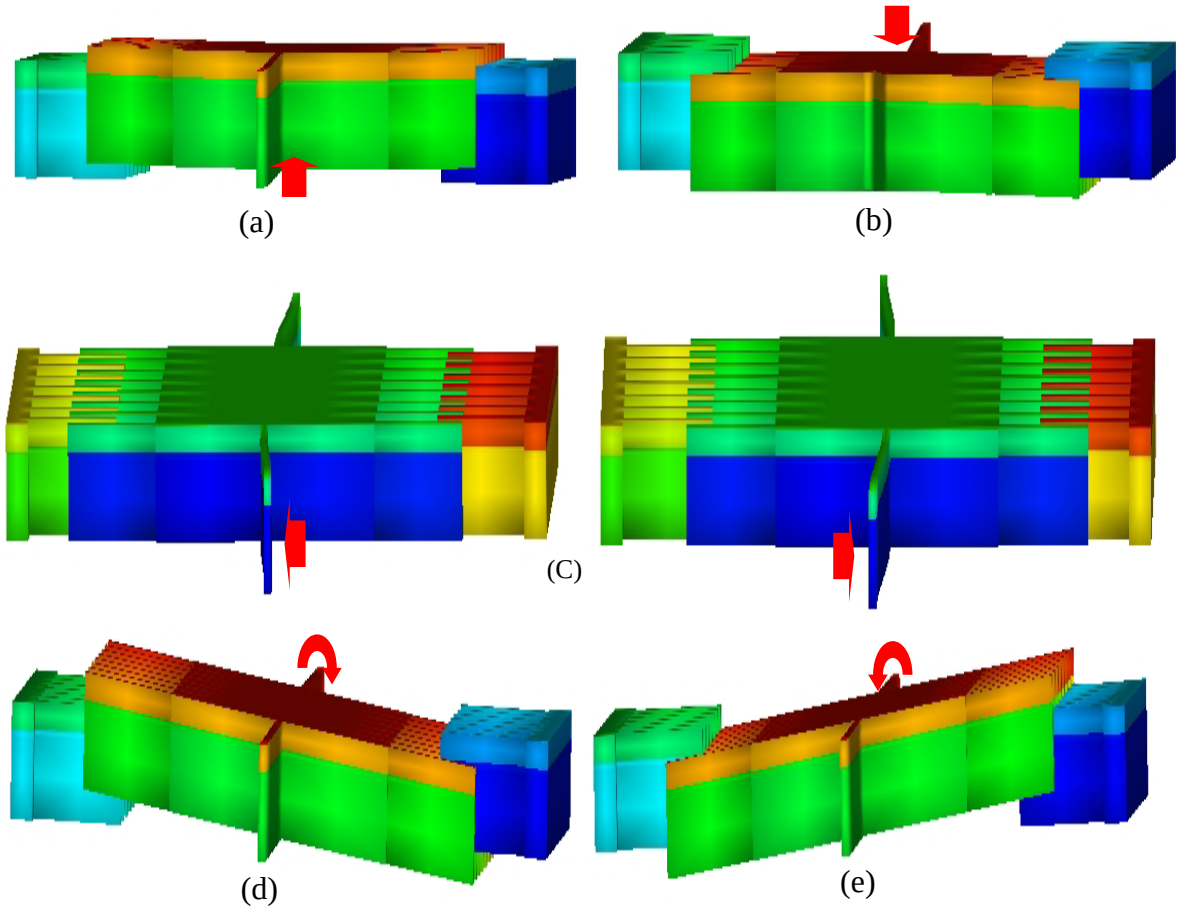
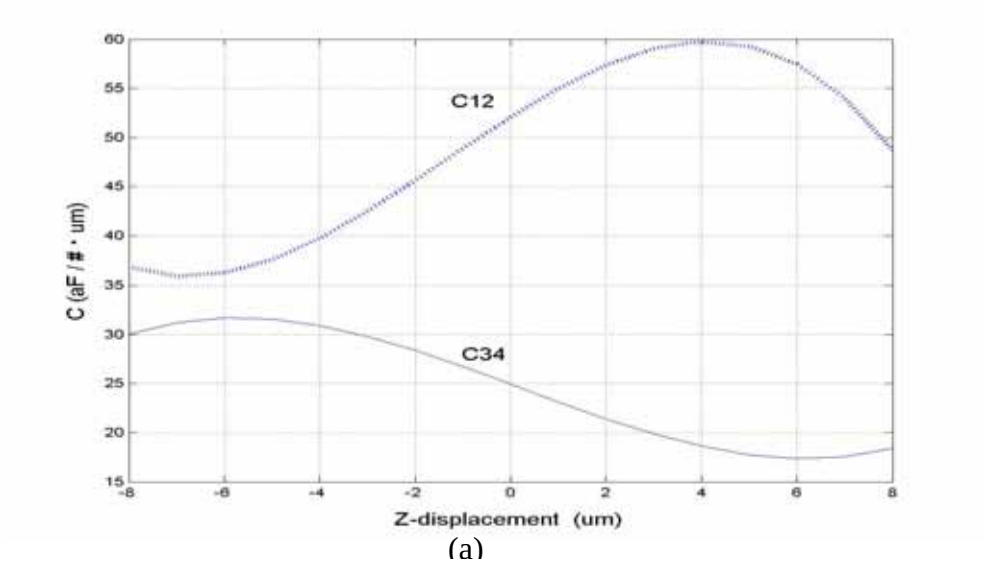
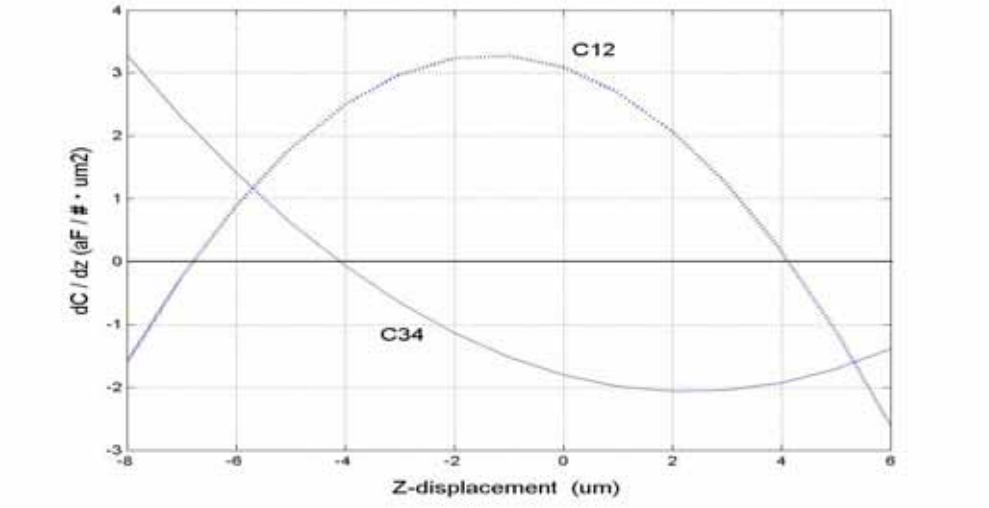


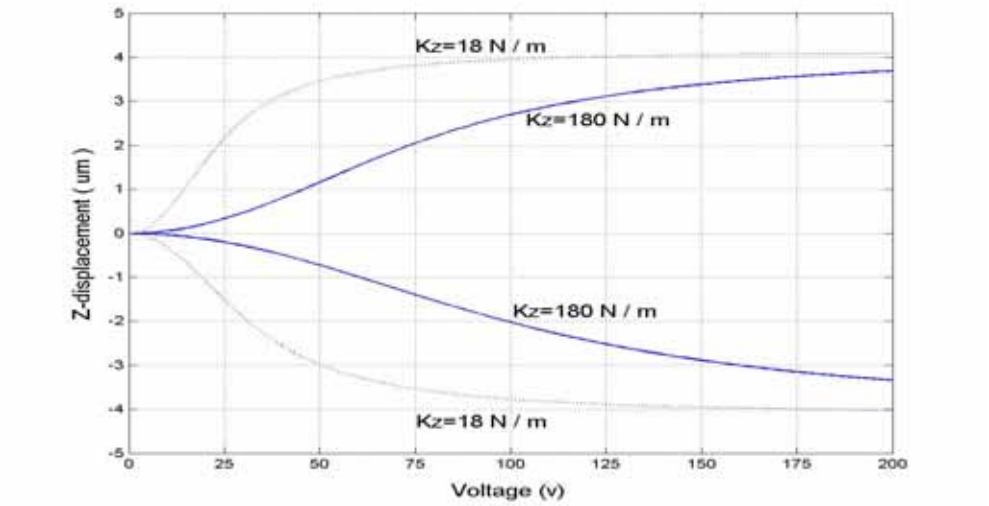

Fig.3 Simulation results of dual comb-drive actuators: (a) upward motion
(b) downward motion (c) horizontal motion (d-e) rotational motion




(a)

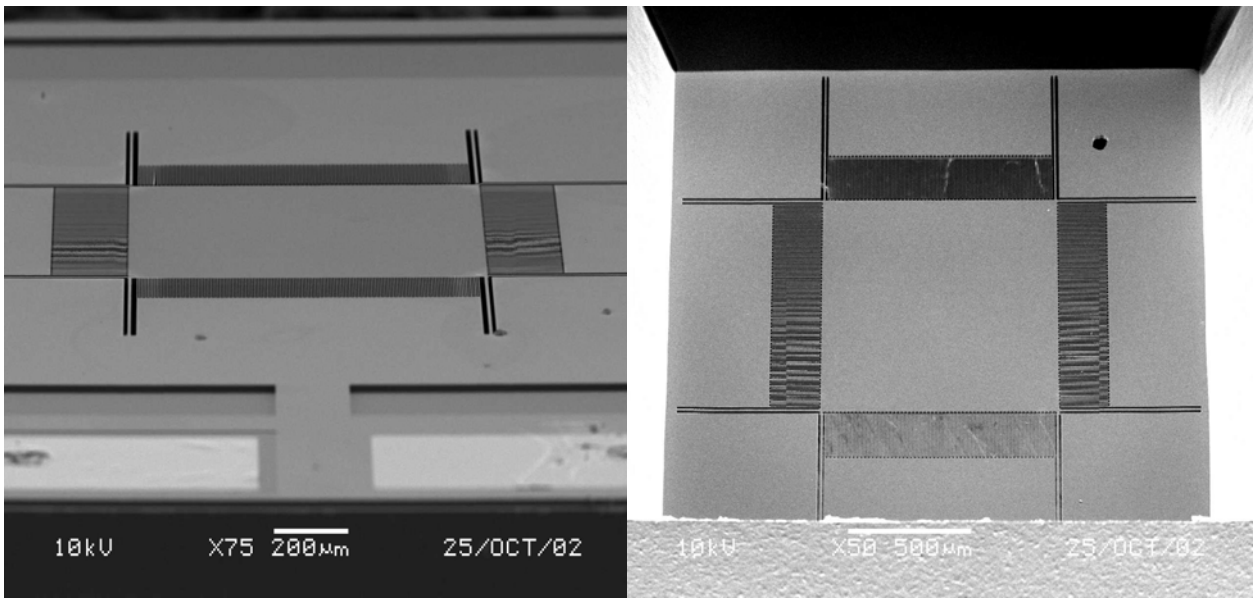



(b)



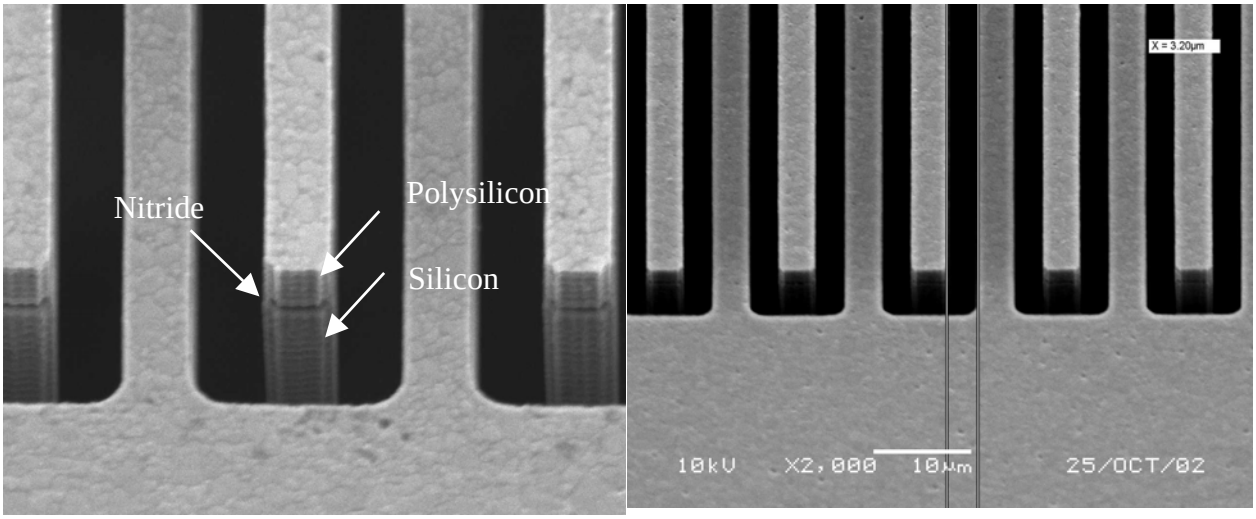

(c)

Fig.4 Calculation results of vertical motion (a) capacitance vs. z-displacement (b) capacitance gradient vs. z-displacement (c) z-displacement vs. applied voltage



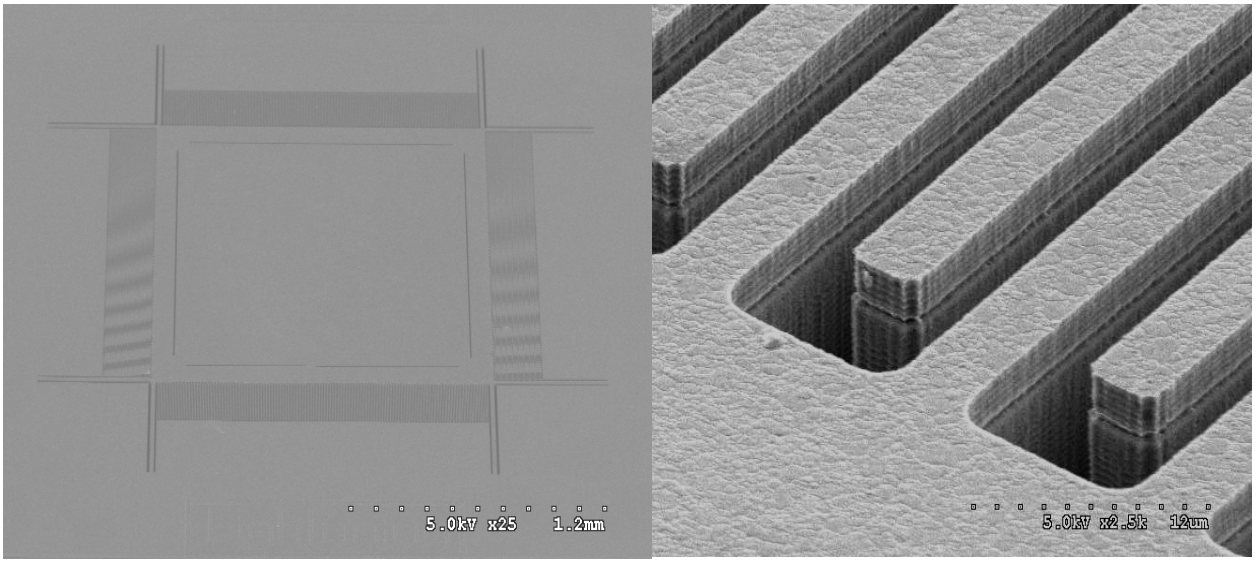

(a) (b)

Fig.5 The SEM pictures of dual comb-drive actuators (a) front side (b) backside



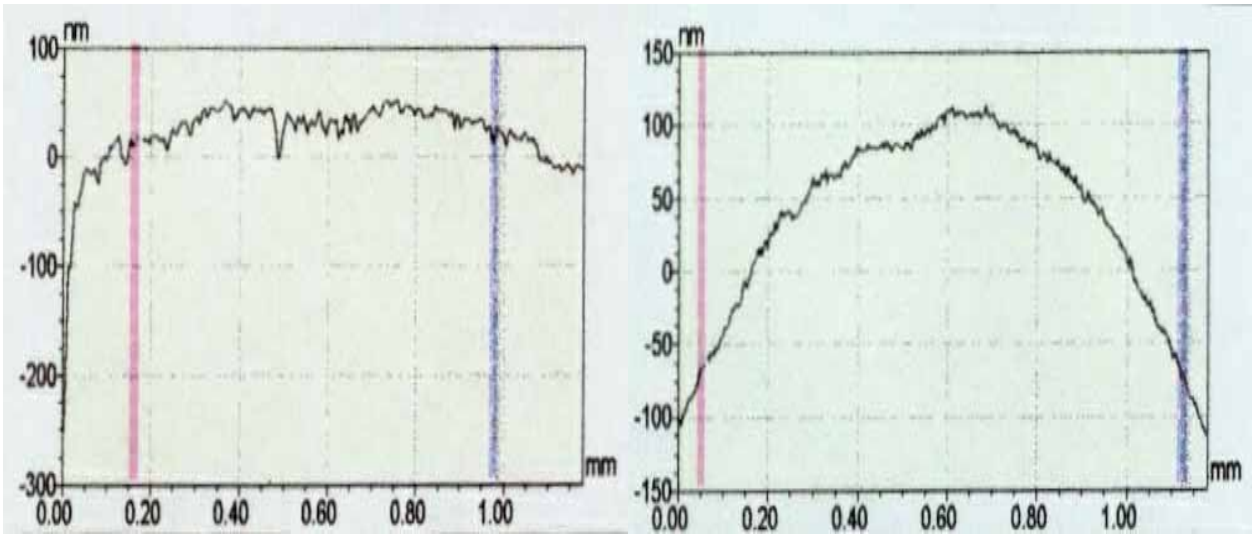

(a) (b)

Fig.6 The SEM pictures of fabricated comb fingers on the dual comb-drive actuators



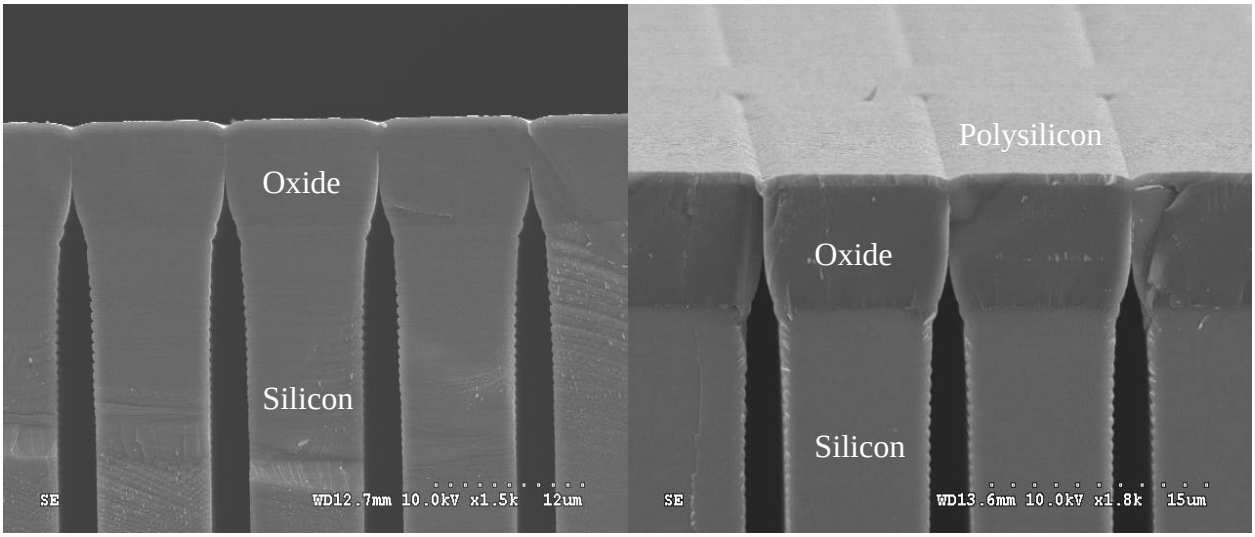

(a) (b)

Fig.7 The SEM pictures of dual comb-drive actuators with 1.5 $mm^2$ fabricated area




(a) (b)

Fig. 8 Single-crystal silicon membrane curve measured by WYKO interferometer (a) without gold; (b) with gold




(a) (b)

Fig.9 The SEM pictures of the cross-section of trench-sealed comb fingers

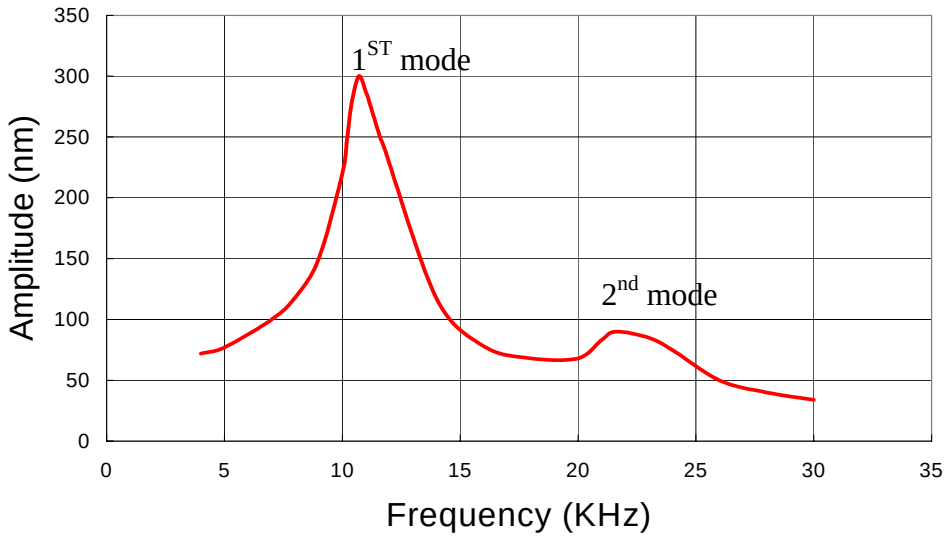
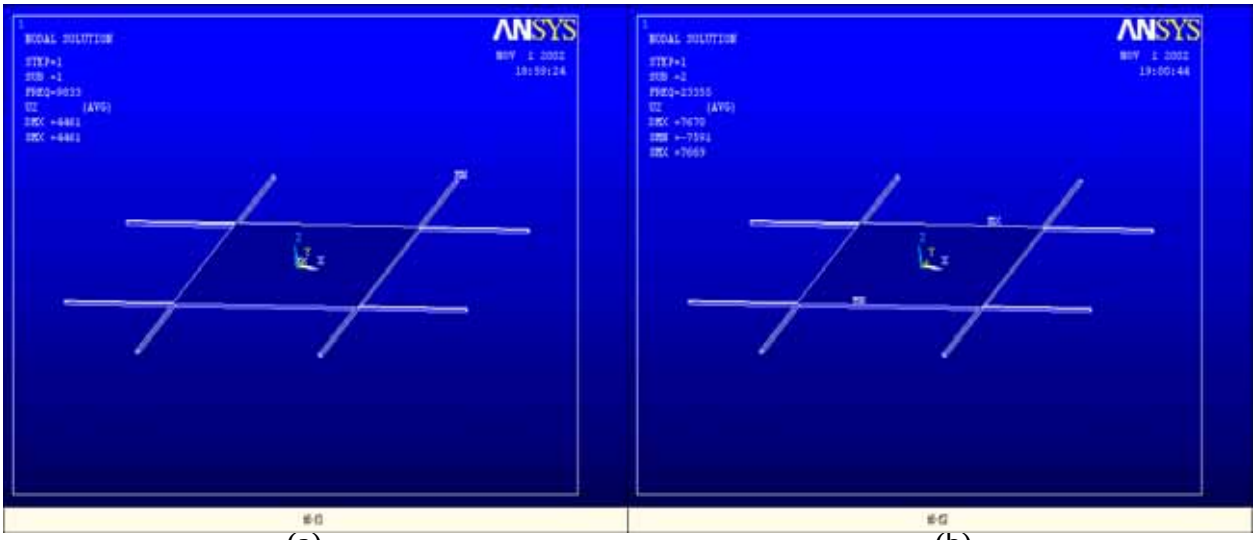



Fig.10 Resonant frequencies of the fabricated device




(a) (b)

Fig.11 Simulations of resonant frequencies by ANSYS (a) 1st mode 9.83KHz (b) 2nd mode 23.3KHz

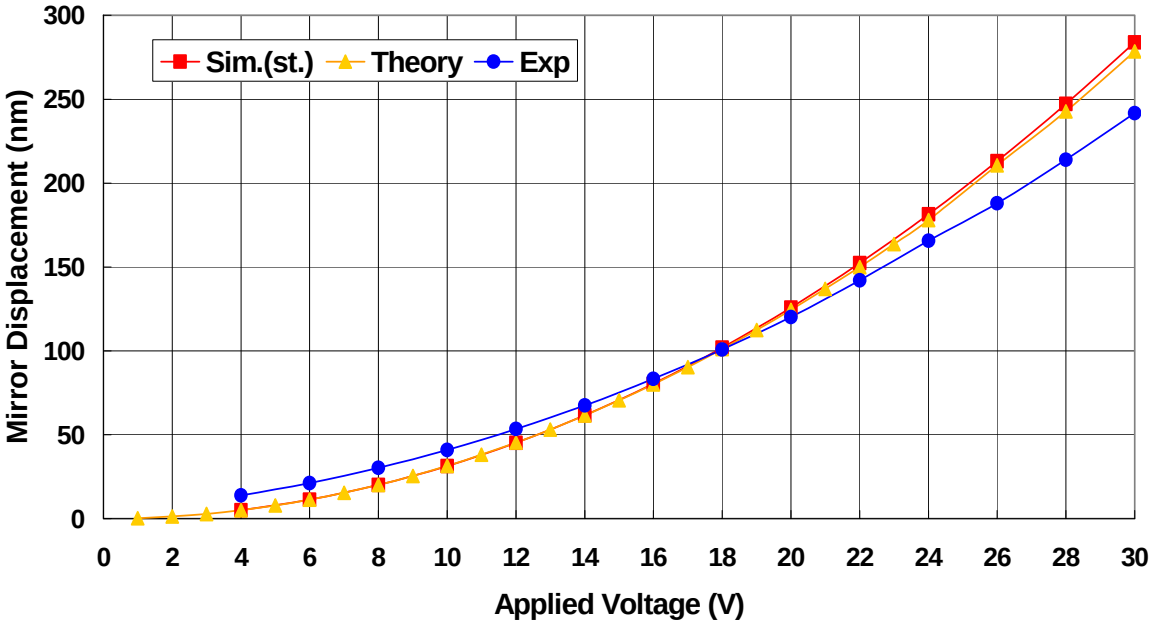



Fig.12 Z-displacement vs. applied voltages include static characterization and dynamic measurement