Charge-Trapping-Induced Parasitic Capacitance and Resistance in SONOS TFTs Under Gate Bias Stress

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***Abstract*—This letter investigates the charge-trapping-induced parasitic resistance and capacitance in silicon–oxide–nitride–oxide–silicon thin-film transistors under positive and negative dc bias stresses. The results identify a parasitic capacitance in OFF-state C–V curve caused by electrons trapped in the gate insulator near the defined gate region during the positive stress, as well as the depletion induced by those trapped electrons. Meanwhile, the induced depletions in source/drain also degraded the I–V characteristic when the gate bias is larger than the threshold voltage. However, these degradations slightly recover when the trapped electrons are removed after negative bias stress. The electric field in the undefined gate region is also verified by TCAD simulation software.**

***Index Terms*—Capacitance–voltage characteristics, semiconductor device reliability, SONOS devices.**

I. Introduction

LOW-TEMPERATURE polycrystalline-silicon thin-film transistors (LTPS TFTs) have been widely investigated for flat-panel applications [1], [2]. Because of their high field-effect mobility and driving current, LTPS TFTs can realize a system-on-panel (SOP) display [3], [4] which is integrated with such functional devices on an LCD panel as a controller and memory [5]. Since SOP technology is primarily used for portable electronics, low power consumption is basically required to ensure long battery life. It is well known that the nonvolatile memory is widely utilized for data storage in portable electronics systems due to its properties of low power consumption and nonvolatility. Unlike conventional nonvolatile floating gate memory, silicon–oxide–nitride–oxide–silicon (SONOS)-type memory has become a promising candidate for SOP application because it is fully compatible with the poly-Si TFTs process. Therefore, the poly-TFTs with ONO dielectric studied in this letter cannot only act as display backplane electronics, including in-pixel switches and peripheral circuits, but also as a nonvolatile memory device. In previous reports, the SONOS TFT for ultradense file storage applications has been proposed [6], and the reliability issues, such as hot carrier degradation and gate/drain disturbance, have been discussed [7], [8]. However, the capacitance-related reliability in SONOS TFTs has not been investigated carefully.

The purpose of our work is to investigate the parasitic capacitances and resistances caused by charge trapping in SONOS TFTs under positive gate bias stress. Experimental results reveal that electrons are trapped at defined and undefined gate regions under positive gate bias stress. In addition, OFF-state capacitance increases due to parasitic capacitances, and on current is degraded due to the parasitic resistances when the device is operated in the ON state. In addition, this study uses a ISE-TCAD simulation to verify the degradation-related electric field.

II. Experiment

In this work, top gate n-channel SONOS TFTs with channel width/length of 6 um/30 um and an overlap structure of 0.75 um were fabricated on a Corning 1737 glass substrate. The silicon oxide buffer layer and a 50-nm-thick undoped amorphous-Si film were deposited by PECVD at 380 °C, followed by dehydrogenation via furnace annealing process at 450 °C. Next, the amorphous-Si film was crystallized by a 308-nm XeCl excimer laser with a line-shaped beam power of 350 mJ/cm^2. The source/drain regions were defined and formed by mass-separated ion implanter technique. Then, the 70-nm-thick ONO multilayer gate dielectric consisting of bottom oxide (10 nm)/silicon nitride (20 nm)/top oxide (40 nm) was deposited by PECVD. MoW was then sputtered and patterned as a gate metal.

All experimental curves were measured using a Keithley 4200 semiconductor parameter analyzer. The stress situation was performed such that dc bias was applied to the gate terminal, while source/drain (S/D) terminals were grounded. During positive stress, the electric field was fixed to 3 MV/cm $(18\ \text{V} + V_{\text{th}})$ for 1000 s, which was smaller than the programming voltage, and an electric field of -4 MV/cm $(-24\ \text{V} + V_{\text{th}})$ was applied at the gate for 1000 s immediately after the positive stress.

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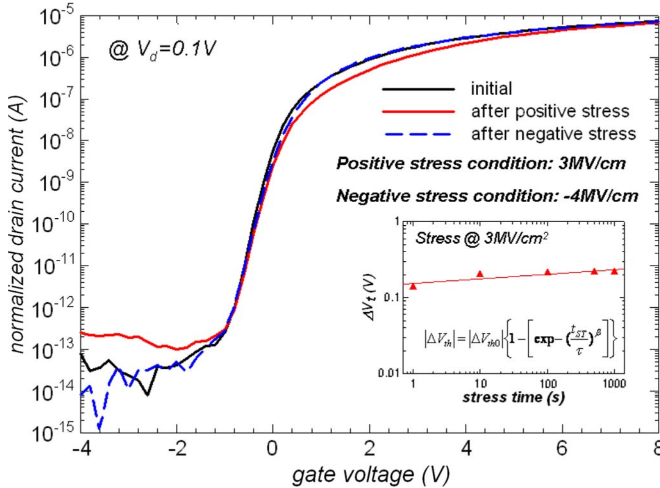

Fig. 1. Normalized I_d–V_g transfer characteristic curves of SONOS TFT, while the drain voltage is 0.1 V under initial and after 1000-s positive and negative stresses.

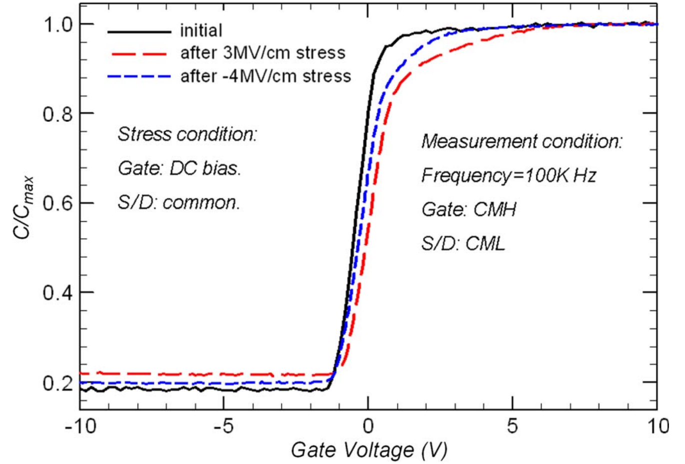

Fig. 2. Normalized C–V transfer characteristics under initial and after positive and negative stresses.

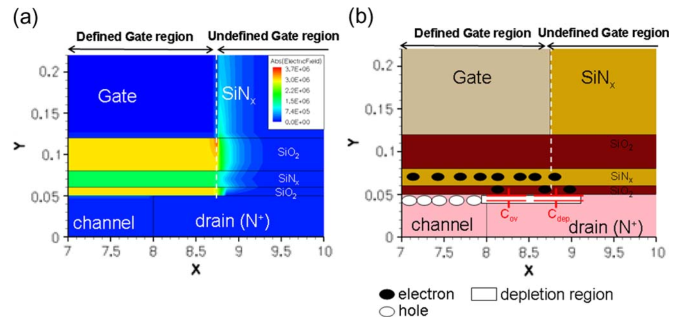

Fig. 3. (a) Distribution of electric field in SONOS TFT while the device is under 3 MV/cm stress. (b) Schematic diagram of the SONOS TFT after 3 MV/cm stress when the device is operated at OFF state.

III. Results and Discussion

Fig. 1 shows the normalized I_d–V_g transfer characteristic curves with 0.1-V drain voltage under the initial and after positive and negative stresses. It can be seen that threshold voltage $(V_{\rm th})$ is slightly shifted to the positive direction, and the on current $(I_{\rm on})$ is degraded after positive stress. Here, the $V_{\rm th}$ is defined as the gate voltage in which the drain current equals 10 nA. However, the $V_{\rm th}$ shift recovers after negative stress. Therefore, the mechanism of the $V_{\rm th}$ shift caused by the state creation is negligible. During positive voltage stress, we can assume that the $V_{\rm th}$ shift is due to the charge trapping in the gate dielectric. The stress time dependence of $V_{\rm th}$ shift is described by the stretched-exponential equation [9], [10]

$$|\Delta V_{\rm th}| = |\Delta V_{\rm th0}| \left\{ 1 - \left[\exp - \left(\frac{t_{\rm ST}}{\tau} \right)^{\beta} \right] \right\} \qquad (1)$$

where $\Delta V_{\rm th}$ is the approximate effect voltage drop across the insulator, τ is the characteristic trapping time, and β is the stretched-exponential exponent. Simulation of the fitting data using (1) was shown in the inset of Fig. 1, which clearly suggests the mechanism of the $V_{\rm th}$ shift after the positive voltage stress is caused by the charge trapping.

Fig. 2 shows the normalized C–V transfer characteristics with a measurement frequency of 100 KHz under initial and after positive and negative stresses. Normalized capacitance is the ratio of the maximum value to measurement capacitance. As can be seen, C–V curve shifts to the positive direction after positive stress, with the capacitance degraded when gate bias was operated from 1 to 7 V. However, these degradations recover slightly after negative stresses. These results are coincident with the I–V curve from Fig. 1. In addition, it is worth mentioning that the OFF-state capacitance is larger than the initial value after the 3 MV/cm stress and slightly decreases after -4 MV/cm stress. In general, the effective OFF-state capacitance in the TFT is the overlapped region between the gate and the S/D, and the increased OFF-state capacitance can be attributed to the trap generation at channel/dielectric interface [11], [12]. Obviously, an increase in the OFF-state capacitance in this work should not be completely ascribed to the mechanism previously mentioned because it is recovered when the -4 MV/cm stress was applied. In order to realize the dominant degradation mechanism in this work, TCAD simulation is employed. In this simulation, the doped profiles of S/D regions in the simulation were assumed to be in a Gaussian distribution.

Fig. 3(a) shows the distribution of the electric field in the SONOS TFT while the device was under 3 M/cm stress. It is obvious that a strong electric field occurs at the corner of the gate electrode. Meanwhile, it can be seen that the stress vertical electric field not only exists in the defined gate region but also in the undefined gate region. Consequently, the electrons will be trapped at the gate-insulator (GI) of both defined and undefined gate regions during the 3 MV/cm stress. Meanwhile, the trapped electrons induce the depletion in the S/D regions because the S/D regions are n^+-type. Therefore, in the C–V measurement, the effective OFF-state capacitance is consisted of the overlap capacitance $(C_{\rm ov})$ and depletion capacitance $(C_{\rm dep.})$ when gate bias was operated at the OFF state, as shown in Fig. 3(b). However, an increase in OFF-state capacitance occurs if the trapped electrons are removed with the application of negative stress.

Fig. 4(a) shows the schematic diagram of the SONOS TFT when the device is operated at ON state, and (b) and (c)

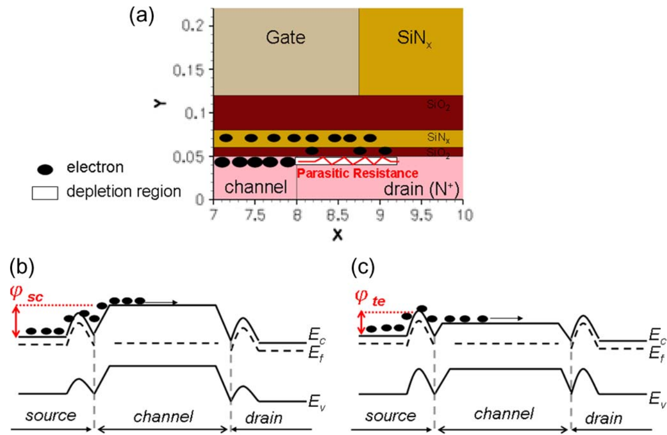

Fig. 4. (a) Schematic diagram of the SONOS TFT after 3 MV/cm stress when the device is operated at ON state, and energy-band diagram of the SONOS TFT when gate bias is (b) smaller than $V_{\rm th}$ and (c) larger than $V_{\rm th}$.

show the energy-band diagram of the SONOS TFT when gate bias is smaller than $V_{\rm th}$ and larger than $V_{\rm th}$, respectively. As can be seen, these trapped electrons at GI induce the parasitic resistances and increase the energy barriers at the S/D regions. Under small gate bias operation $(V_g < V_{\rm th})$, the I–V transfer characteristic curves are mainly controlled by the source/channel barrier $(\varphi_{\rm sc})$. Moreover, the $\varphi_{\rm sc}$ is gradually decreased and lower than trapped-electron-induced barrier $(\varphi_{\rm te})$ when the gate bias was swept further to the positive direction. Consequently, the ON-state degradation of I–V curves caused by $\varphi_{\rm te}$ will be obvious when gate bias is larger than $V_{\rm th}$. This result is demonstrated in Fig. 1.

IV. Conclusion

This letter has investigated the charge-trapping-induced parasitic resistance and capacitance in SONOS TFTs under positive and negative dc stresses. Under positive stress, the electrons are trapped at the GI of both the defined and undefined gate regions due to the vertical electric field; the stressed electric field has been verified by the TCAD simulation software. The trapped-electron-induced depletion in the S/D regions will contribute to the parasitic capacitance when the device is operated at OFF state. Meanwhile, the depletions caused by the trapped electron also degrade the I–V transfer characteristic curve when the gate bias is larger than threshold voltage. Finally, these degradations recover slightly after the trapped electrons are removed with the application of negative stress.

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