Arsenic-Implanted HfON Charge-Trapping Flash Memory With Large Memory Window and Good Retention

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***Abstract*—We have fabricated the TaN–[$SiO_2-LaAlO_3$]–HfON–[$LaAlO_3-SiO_2$]–Si charge-trapping Flash device. A large 6.4-V initial memory window, a 4.3-V 10-year extrapolated retention window at 125 °C, and a 5.5-V endurance window at 10^6 cycles were measured under very fast 100-μs and low $\pm$16-V program/erase. These excellent results were achieved using an As^+ implant into the HfON trapping layer, which were significantly better than those of the control device without ion implantation.**

***Index Terms*—Charge-trapping Flash (CTF), HfON, ion implant, nonvolatile memory (NVM).**

I. Introduction

THE metal–oxide–nitride–oxide–Si (MONOS) charge-trapping (CT) Flash (CTF) devices [1]–[15] have been used for the next-generation nonvolatile memory (NVM) beyond the conventional poly-Si floating-gate Flash memory. This is due to the discrete trapping property of Si_3N_4 that allows the use of a thinner tunnel oxide to improve the erase saturation. However, the much shallower trap energy in Si_3N_4[11] than the deep 3.15 eV in conventional poly-Si floating gates degrades the high-temperature retention characteristics [12]–[15]. The retention can be improved by using a thicker tunnel oxide, but this yields slow erase (10–100 ms). Such a retention and erase-speed tradeoff is a basic limitation of NVM. Furthermore, both a good memory window and a good endurance should be achieved simultaneously. However, a 10$\times$ degradation in endurance is the other limitation for highly scaled CTF memory devices [1] due to the smaller number of electrons stored in the Flash cell.

To address these issues, we previously presented Al(Ga)N or HfON layers with deep trap energies as the trapping layer in MONOS CTF devices [12]–[15]. The better retention of high-κ Al(Ga)N MONOS CTF was confirmed by another group [16] and is listed in ITRS [1]. However, the trapping property of HfON is inferior compared to that of Si_3N_4 which can be seen in a reduced memory window [14], [15]. In this letter, we report a CTF device with an initial 6.4-V memory window, a large extrapolated ten-year retention window of 4.3 V at 125 °C, and 10^6 endurance under fast 100-μs and low $\pm$16-V program/erase (P/E). These excellent results were achieved using an As^+ implant into the HfON trapping layer and show significant improvement compared to the control device without the implant.

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II. Experiments

The TaN–[$SiO_2-LaAlO_3$]–HfON–[$LaAlO_3-SiO_2$]–Si devices were made by growing the double tunnel oxide layers of 2.5-nm thermal SiO_2 on a standard p-Si substrate and 2.5-nm $LaAlO_3$ deposited by physical vapor deposition (PVD). Then, the 30-nm HfON was grown by reactive PVD as the CT layer that gives a small 8.4-nm equivalent Si_3N_4 thickness (ENT). The As^+ implantation into HfON was applied at 10 keV, 1×10^{15} cm^{-2} dose, and 60° titled angle followed by 950 °C 1-s rapid thermal annealing (RTA). Next, 8-nm $LaAlO_3$ was deposited by PVD, and a 7-nm TEOS ($Si(C_2H_5O)_4$) oxide was deposited by chemical vapor deposition to form the double blocking dielectric layers. Finally, 200-nm TaN was deposited by PVD, followed by gate definition, reactive ion etching, self-aligned 25-keV As^+ implantation at 5×10^{15} cm^{-2} dose, and 900 °C 30-s RTA to activate the dopant at the source–drain region. The capacitor size is 100 μm $\times$ 100 μm and is isolated by a field oxide. The CTF device has the same layout as that of a MOSFET with a 10-μm gate length and a 100-μm width and is isolated by a field oxide.

III. Results and Discussion

Fig. 1 shows the C–V hysteresis of HfON CT stack capacitors with and without the As^+ implantation. The C–V hysteresis window increases with increasing voltage, indicating the good trapping property. A large C–V hysteresis window of 11.1 V was obtained in As^+-implanted CT stack capacitors under $\pm$16-V sweep. The large hysteresis window is not due to device variations, as evident from the close capacitance density in control devices. The large increase in the hysteresis window may be due to the forming deep energy levels [17] in the HfON trapping layer by the As^+ implant with 950 °C RTA.

Fig. 2 shows the J_g–V_g characteristics of the HfON MONOS CTF devices with and without the As^+ implant. The J_g–V_g was measured at a sweep rate of 2.5 V/s. The gate leakage current obtained on As^+-implanted devices is close to that on

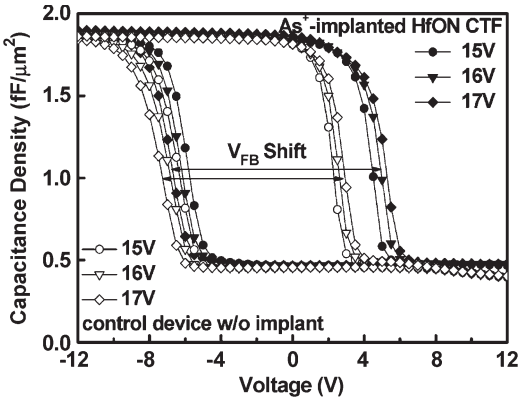


Fig. 1. C–V hysteresis of HfON CT stack capacitors with and without As^+ implant.

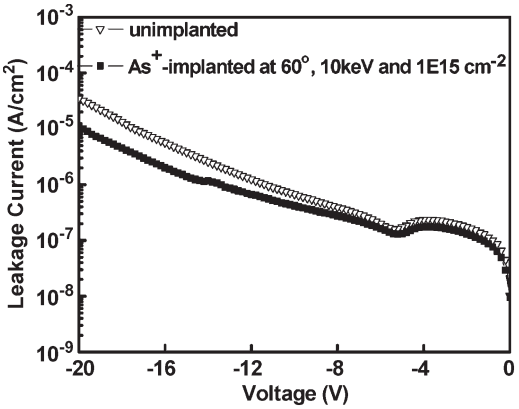


Fig. 2. J_g–V_g curves of HfON MONOS CTF devices with and without As^+ implant.

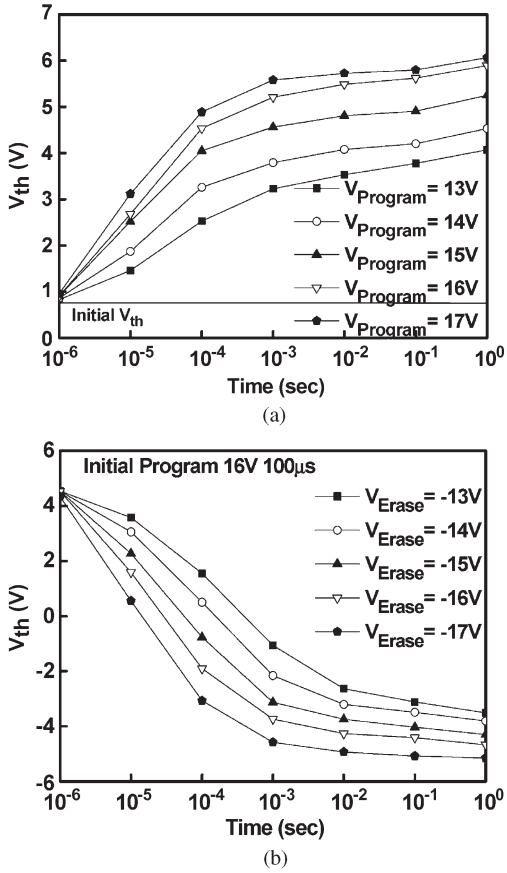


Fig. 3. (a) Program and (b) erase characteristics of As^+-implanted HfON MONOS CTF devices for different voltages and times. For erase, the device was initially programmed at 16 V for 100 μs.

the control devices, indicating that the 60-tilted and 10-keV As^+ implant did not reach or damage the tunnel oxide layers. The slightly lower leakage current in As^+-implanted devices at high V_g is related to the better electron trapping efficiency shown in Fig. 1, which results in an increased effective barrier height by Columbic repulsive force.

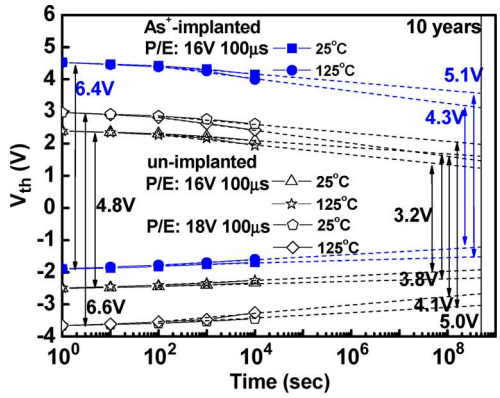
Fig. 3(a) and (b) shows the program and erase characteristics of As^+-implanted HfON CTF devices. The threshold voltage $(V_{\rm th})$ increases with increasing P/E voltage and time with a small saturation effect. At $\pm$16-V and fast 100-μs P/E, a large $\Delta V_{\rm th}$ memory window of 6.4 V is obtained. Such a large memory window is even better than that of the Si_3N_4–HfON double-trapping-layer CTF device [15]. The fast 100-μs P/E speed is due to the additional conduction and valance band discontinuity (ΔE_C and ΔE_V) in $LaAlO_3$ and SiO_2 barriers for easier tunneling during program and erase, respectively.

Fig. 4(a) and (b) shows the retention and endurance characteristics. For As^+-implanted HfON devices at $\pm$16-V and 100-μs P/E, large ten-year extrapolated memory windows of 5.1 and 4.3 V were obtained at 25 °C and 125 °C, respectively, which are better than the retention window of control devices. The good retention is due to the physically thicker double $LaAlO_3-SiO_2$ for carrier confinement, while the ΔE_C and ΔE_V in $LaAlO_3/SiO_2$ improve the program and erase speed. This large ten-year retention window with a small 8.4-nm ENT trapping layer allows multilevel cell storage even at 125 °C [15].

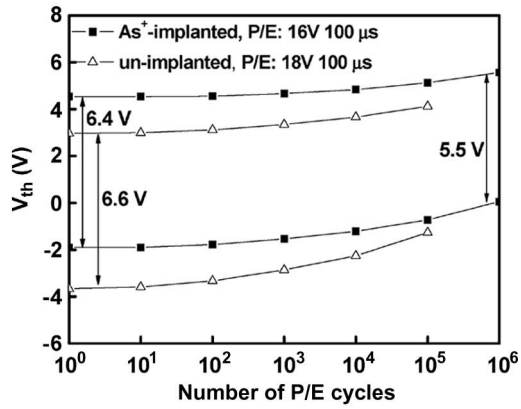
At the same $\pm$16-V and 100-μs P/E condition, the control device without the As^+ implant shows significantly smaller initial and ten-year retention memory windows. The control device can also be programmed to reach a larger memory window at $\pm$18-V and 100-μs P/E, but the retention characteristics are slightly inferior to those of the As^+-implanted device. This may be due to the generation of deep levels [17] in the trapping layer due to the As^+ implantation. Additionally, the control device can only be cycled up to 10^5 cycles at $\pm$18-V and 100-μs P/E pulse duration, which is a typical value for CTF memory cells. In sharp contrast, the As^+-implanted device has $10\times$ better endurance with a large 10^6 cycled window of 5.5 V at $\pm$16-V and 100-μs P/E. This excellent 10^6 cycling is vital to allow further endurance improvement in highly scaled CTF devices with fewer electrons. Such good endurance is due to the high CT efficiency, allowing low P/E voltage, fast 100-μs P/E speed, and the existing ΔE_C and ΔE_V for easy tunneling that leads to less stress in the $LaAlO_3-SiO_2$ tunnel oxide.

IV. Conclusion

Using As^+ implantation into the HfON trapping layer of the MONOS CTF device, a large 6.4-V initial memory window, a 4.3-V 10-year extrapolated retention window at



(a)



(b)

Fig. 4. (a) Retention and (b) cycling characteristics of HfON MONOS CTF devices with and without As^+ implant.

125 °C, and a 5.5-V endurance window at 10^6 cycles have been demonstrated under a fast 100-μs speed and a low P/E voltage of $\pm$16 V.

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