Comparison of 4T and 6T FinFET SRAM Cells for Subthreshold Operation Considering Variability—A Model-Based Approach

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***Abstract*—This paper investigates the cell stability of recently introduced four-transistor (4T) and conventional six-transistor (6T) fin-shaped field-effect transistor static random access memory (SRAM) cells operating in a subthreshold region using an efficient model-based approach to consider the impact of device variations. Compared with the 6T cell, this paper indicates that 4T SRAM cells exhibit a better nominal READ static noise margin (RSNM) because of the reduced READ disturb. For 4T cells, the nearly ideal values of $V_{\mathrm{write},0}$ and $V_{\mathrm{write},1}$ guarantee the positive nominal WRITE static noise margin (WSNM) for selected cells. For half-selected cells on the selected bit line, a sufficient margin is observed between WRITE time (for selected cells) and WRITE disturb (for half-selected cells). Using the established model-based approach, the variability of subthreshold 6T and 4T SRAM cells is assessed with 1000 samples. Our results indicate that the 4T driverless cell with a larger μRSNM and a slightly worse σRSNM shows a comparable μ/σ ratio in RSNM with the 6T cell. Furthermore, for a given cell area, 4T SRAM cells using relaxed device dimensions with reduced σRSNM can outperform the 6T cell. For WRITE operation, 4T SRAM cells exhibit a superior WSNM, whereas the design margin between WRITE time and WRITE disturb needs to be carefully examined to ensure an adequate margin considering device variability.**

***Index Terms*—Fin-shaped field-effect transistor (FinFET), static noise margin (SNM), subthreshold static random access memory (SRAM), variability.**

I. Introduction

FOR ultralow-power applications in portable devices, implanted medical instruments, and wireless body sensing networks, operating circuits with the supply voltage V_{dd} below the threshold voltage V_T has emerged as an effective solution to reduce power consumption [1]. However, the reduced $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio and aggravated device variations in a subthreshold regime become serious concerns, particularly for static random access memory (SRAM) cells with minimum-size or sub-groundrule devices. The cell stability deteriorates with decreasing V_{dd}, and several novel bulk eight/ten-transistor cell structures have been proposed to replace the conventional six-transistor (6T) SRAM cell for subthreshold applications [2]–[5].

Due to its superior gate control, a fin-shaped field-effect transistor (FinFET) exhibits better subthreshold slope, reduced leakage current, and higher $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio. In addition, the use of a lightly-doped silicon fin improves the immunity to random dopant fluctuation, making a FinFET a promising candidate for emerging subthreshold SRAM applications [6], [7]. To assess and establish the feasibility of FinFET-based subthreshold SRAM cells, an extensive investigation considering the impacts of device variations on cell stability is required. Unlike bulk metal–oxide–semiconductor field-effect transistor, the SPICE model for an extremely scaled FinFET device incorporating crucial quantum–mechanical effects is lacking. Therefore, technology computer-aided design (TCAD) atomistic Monte Carlo mixed-mode simulations considering various variation sources are often used to assess the statistical characteristics of SRAM cells [8]–[11]. However, limitations on the computational efficiency, storage capacity, and sample size have hindered the feasibility of quick assessment for SRAM cell design.

In this paper, a model-based approach is developed and employed to efficiently investigate the impacts of device variations on the cell stability of four-transistor (4T)/6T subthreshold FinFET SRAM cells. The model is physically derived from the fundamental equations without fitting parameters. Compared with the SPICE approach, the model shows superior scalability and predictability. The remainder of this paper is organized as follows: Section II describes the framework of our model-based approach used in this study. With the established methodology, two recently introduced 4T FinFET SRAM cells and the conventional 6T FinFET cell are compared in Section III. The advantages of 4T FinFET SRAM cells are demonstrated using our model-based approach considering the impact of fin line-edge roughness (fin LER) on the cell stability. Finally, we draw the conclusion in Section IV.

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II. Framework of the Model-Based Approach

A. Atomistic TCAD Monte Carlo Simulation

To capture the atomic-level imperfections of each microscopically different device, sophisticated TCAD simulations [12] are needed. The discreteness of ionized dopant, ragged line edge, and interface have been known to cause a mismatch in

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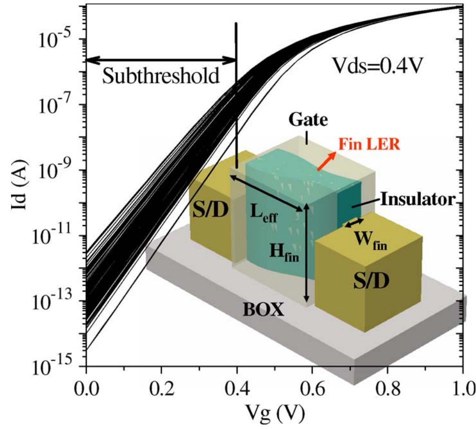

Fig. 1. I_d–V_g characteristics of FinFET device considering fin LER. (Inset) Example of the FinFET samples with fin LER simulated in this work.

neighboring devices [13]. Among various local random variation sources, LER-induced variation on the fin width (fin LER) of FinFET devices is the dominant variation source [8]. Hence, fin LER is considered in this paper to evaluate the robustness of FinFET cell stability.

To simulate LER, rough line-edge patterns are generated by the Fourier synthesis approach [14] with a correlation length of 20 nm and a root-mean-square amplitude of 1.5 nm [8]. Atomistic TCAD Monte Carlo simulations with 200 samples are then performed. Fig. 1 shows the I_d–V_g subthreshold characteristics of FinFET suffering from fin LER, and the inset illustrates one of the simulated FinFET samples with fin LER.

B. Model Library Buildup

The analytical FinFET subthreshold drain-current model derived in [15] and [16] is used to bridge the gap between atomistic TCAD and circuit-level simulations in this model-based approach. The proposed FinFET subthreshold drain-current model has been shown to be capable of accurately describing subthreshold drain-current characteristics for tied- and independent-gate modes of operation [6]. In the subthreshold region, the device I_d–V_g characteristic can be described by the subthreshold swing (S.S.) and the OFF-state current $I_{\rm off}$. Hence, the characteristic of each device with an irregular fin pattern can be captured by a set of effective fin width $W_{\rm fin}$ and gate work function (WF), which result in the same S.S. and $I_{\rm off}$ as the TCAD result. Fig. 2(a) compares the calibrated model with TCAD simulations for three extreme cases (maximum, medium, and minimum currents). As can be seen, the model shows a fairly good agreement with TCAD simulation results at $V_{ds} = 0.05$ and 0.4 V.

Following the same procedure, each device in Fig. 1 can be characterized with the corresponding parameters ($W_{\rm fin}$ and WF) to build up the model library. Fig. 2(b) examines the discrepancies of S.S. and $I_{\rm off}$ between the calibrated model and TCAD simulations for each device from 200 samples. It can be seen that the errors are negligible, thus validating the feasibility of this approach.

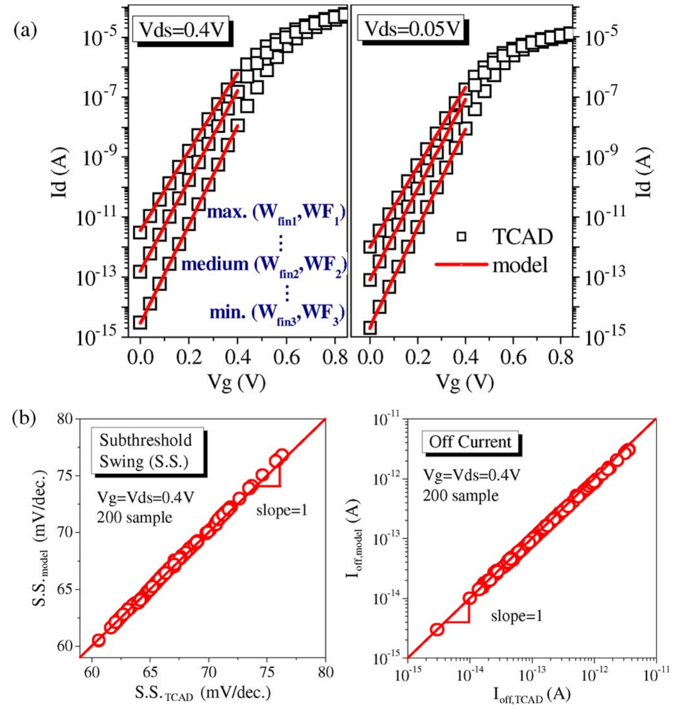

Fig. 2. Model calibration with TCAD simulations to build a model library for the (a) three extreme cases and (b) error analysis of S.S. and $I_{\rm off}$ for each sample.

C. SRAM Level Simulation

Using the established model library, we can analyze the influence of device variations on the cell stability instead of employing the time-consuming TCAD mixed-mode simulations. The transistors in the SRAM cell are randomly selected from the model library and are used to construct the butterfly curve, as described in [6]. Fig. 3(a) compares the READ static noise margin (RSNM) variation of the conventional tied-gate 6T FinFET cell [see Fig. 3(b)] between the model-based approach and TCAD simulations. It can be seen that the model-based approach shows very good agreement with TCAD results (error $(\mu) = 0.9$ mV, and error $(\sigma) = 0.1$ mV). More importantly, our model-based approach provides significantly better computational efficiency (~45X) compared with TCAD simulations. Thus, the samples size can be easily increased to 1000 or more, which is significantly larger than the TCAD simulation can reasonably provide (typically limited to 100–200) [8]–[11].

Fig. 4 summarizes the flow of our model-based approach. In the following section, the potential of two reported 4T FinFET SRAM cells is investigated for subthreshold operation ($V_{dd} =$ 0.4 V) using the model-based approach. The analysis is based on a FinFET device designed with $L_{\rm eff} = 25$ nm, $W_{\rm fin} = 7$ nm, $H_{\rm fin} = 20$ nm, and EOT $= 1$ nm (see Fig. 1).

III. Analysis of Subthreshold 4T FinFET SRAM Cells

A. Stability of Subthreshold 4T FinFET SRAM Cells

In Fig. 3(b), the conventional 6T SRAM cell is composed of pull-up (PL, PR), pull-down (NL, NR), and pass-gate (AXL,

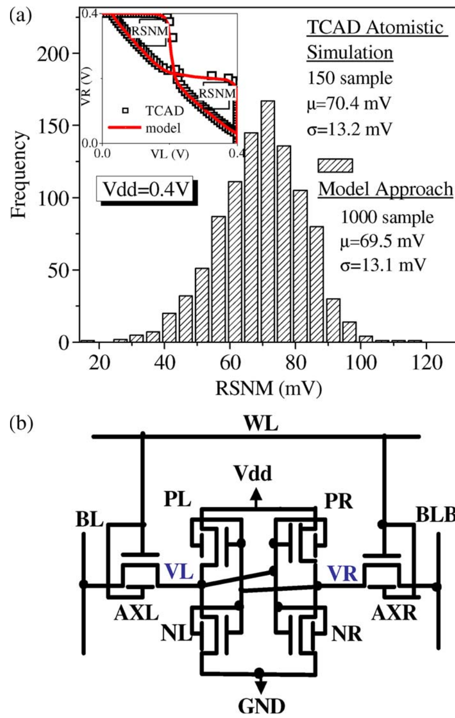

Fig. 3. (a) Comparison of the RSNM variation between TCAD mixed-mode simulations and the model-based approach. (b) Schematic of the conventional tied-gate 6T FinFET SRAM cell.

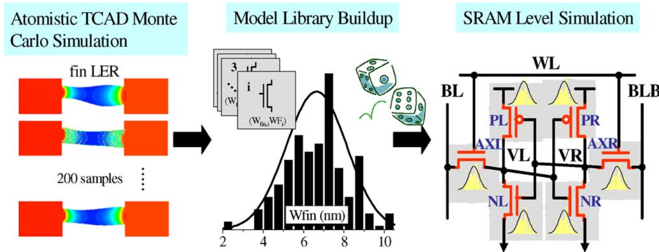

Fig. 4. Flow of the model-based approach to consider the impacts of device variations.

AXR) transistors. Pull-up and pull-down transistors form the cross-coupled inverter latch to store the data, and the cell is accessed by pass-gate devices. Due to the capability of independent-gate control, a single FinFET device has been proposed to replace the function of two traditional transistors [17] to reduce the transistor count and the circuit area. Similarly, the conventional 6T SRAM cell can also be reduced to 4T cells. Fig. 5 illustrates two types of recently introduced 4T FinFET SRAM cells reported in the literature [18].

The 4T loadless (LL) cell, as shown in Fig. 5(a), combines the function of the p-channel FET (PFET) pass-gate device with a PFET pull-up transistor using one single independent-gate controlled transistor (PL, PR). Notice that the source nodes of PL/PR are connected to the bit-line BL/BLB, which are precharged to "High" (V_{dd}). The cell is activated when the word line (WL) goes to "Low." Fig. 6(a) shows the READ butterfly curve of 4T LL cell. As can be seen, the READ disturb voltage $V_{\mathrm{read},0}$ of the 4T LL cell is negligibly small as it is determined by the voltage divider effect between the single-gate (SG)-mode pass-transistor PFET (one gate of

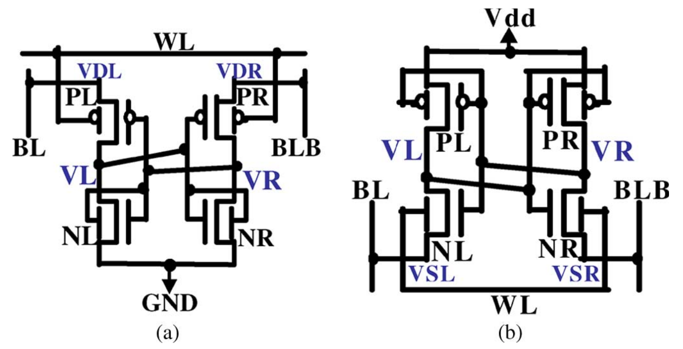

Fig. 5. Novel 4T SRAM cells using independent-gate control technique. (a) 4T LL cell. (b) 4T DL cell [18].

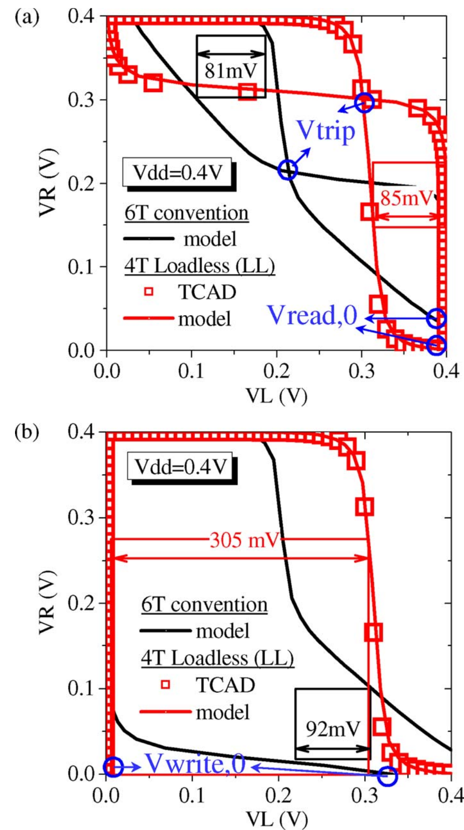

Fig. 6. Comparison of butterfly curves for 4T LL cell with conventional 6T SRAM cell. (a) RSNM. (b) WSNM.

PL/PR) and the double-gate (DG)-mode pull-down n-channel FET (NFET) (tied-gate NL/NR). In addition, owing to the fully-conducting back gates (serving as pass-gate devices), the strength of the front-gate devices of PL/PR (serving as pull-up devices) is enhanced, thus increasing the trip voltage of the cell. Compared with the conventional 6T cell, the 4T LL cell exhibits a better nominal RSNM. During WRITE operation, the virtual supply node VDL/VDR connecting to the low-going bit-line is pulled down to GND by the WRITE driver, thus facilitating the pull-down of the cell storage node. As such, $V_{\mathrm{write},0}$ becomes very low, resulting in a significantly larger/better WSNM than that in the conventional 6T cell [see Fig. 6(b)].

In Fig. 5(b), the 4T driverless (DL) cell uses the back gates of the pull-down transistors (NL, NR) as pass-gate transistors.

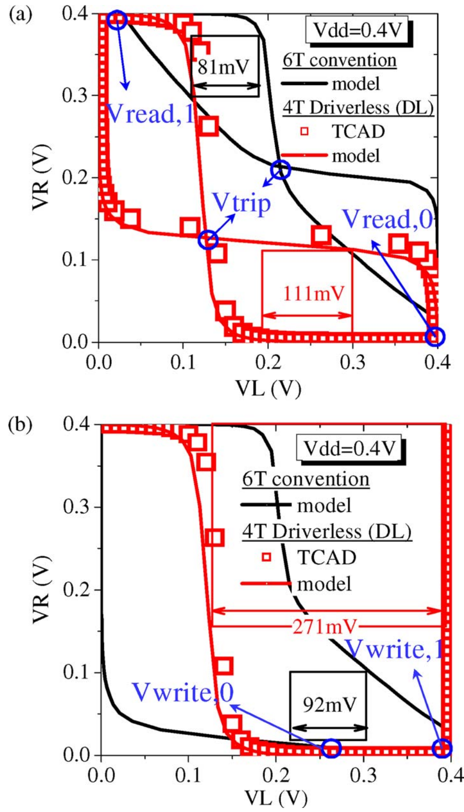

Fig. 7. Comparison of butterfly curves for a 4T DL cell with the conventional 6T SRAM cell. (a) RSNM. (b) WSNM.

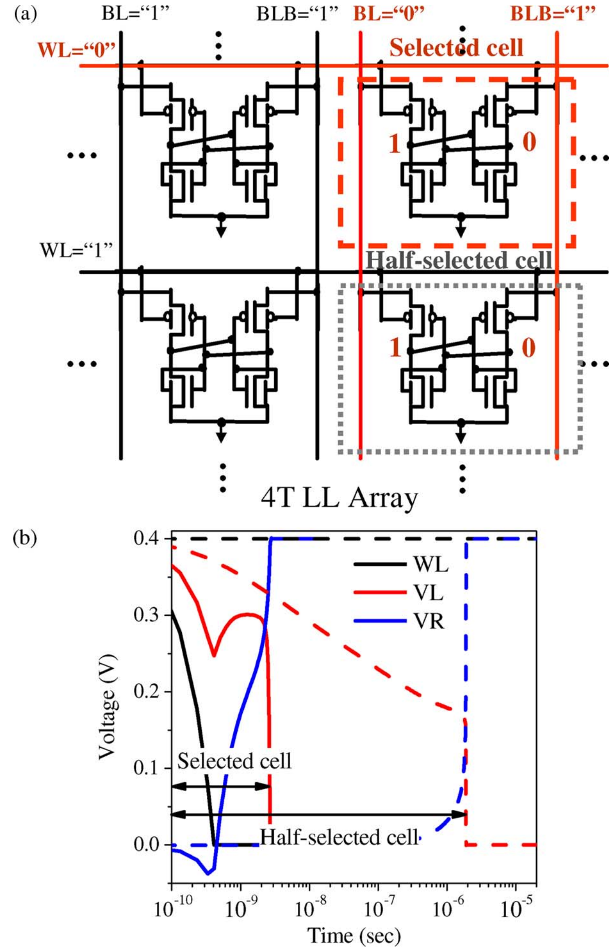

Fig. 8. (a) Illustration of WRITE disturb in half-selected cells during WRITE operation. (b) Comparison of the required time to flip the states of the selected and half-selected cells (TCAD simulations).

The source nodes of NL/NR are connected to bit-line BL/BLB, which are predischarged to "Low" (GND). During READ operation, the WL goes to "High" to access the cell. In contrast to the 4T LL cell, the READ disturb of the 4T DL cell comes from the storage node holding "1" (Read disturb $= V_{dd} - V_{\mathrm{read},1}$). As shown in Fig. 7(a), $V_{\mathrm{read},1}$ is close to V_{dd} as it is determined by the voltage divider effect between the DG-mode pull-up PFET (tied-gate PL/PR) and the SG-mode pass-transistor NFET (one gate of NL/NR), resulting in a superior RSNM. During WRITE operation, the virtual ground node VSL/VSR connecting to the high-going bit-line is pulled up to V_{dd} by the WRITE driver, thus facilitating the pull-up of the cell storage node. As such, $V_{\mathrm{write},1}$ becomes very close to V_{dd}, resulting in a significantly larger/better WSNM than that in the conventional 6T cell [see Fig. 7(b)]. Moreover, the comparisons and excellent agreement between the model and TCAD simulations for READ/WRITE operations of 4T cells are illustrated in Figs. 6 and 7.

Notice that, in the 4T LL (or 4T DL) cell, during WRITE operation, as the virtual supply node VDL/VDR (or the virtual ground node VSL/VSR) is pulled down (or pulled up) by the WRITE driver along with the low-going (or high-going) bit-line, the half-selected cells on the selected bit-line with stored data identical to that of the selected cell suffer WRITE disturb. Fig. 8(a) illustrates the WRITE disturb of the half-selected cells (enclosed by dotted lines) on the selected bit-line in a 4T LL cell array. For the case shown, VDL for the half-selected cell (which connects to BL) is pulled down by the WRITE driver, whereas the front gate of PL is at "0," thus forming a leakage path to discharge its left storage node VL (supposedly to maintain its "1" state). Notice that this WRITE disturb is essentially a "Weak WRITE" through the front gate of PL, whereas the selected cell is written by the DG mode of PL. Thus, in order to have a viable design margin between "Writing selected cell" and "Not flipping the half-selected cells," it is essential to have a large current ratio between the DG and SG modes for PL/PR. This can be achieved by using asymmetrical DG devices (different V_T for front and back gates), different oxide thickness for front and back gates, or by using high-V_T DG devices. To investigate the design margin of WRITE disturb, selected and half-selected cells are examined by TCAD transient simulations and compared in Fig. 8(b). As can be seen, the time required to flip the stored data in a half-selected cell is 1000X longer than that of the selected cell. The large nominal margin between WRITE time and WRITE disturb is necessary to ensure an adequate margin considering the variability addressed below.

B. Variability Analysis of Subthreshold 4T FinFET SRAM Cells

In this section, the impact of device variations on the stability of the conventional 6T and 4T FinFET SRAM cells is examined using the model-based approach. Fig. 9(a) illustrates the layouts of 6T and two recently introduced 4T cells based on scaled

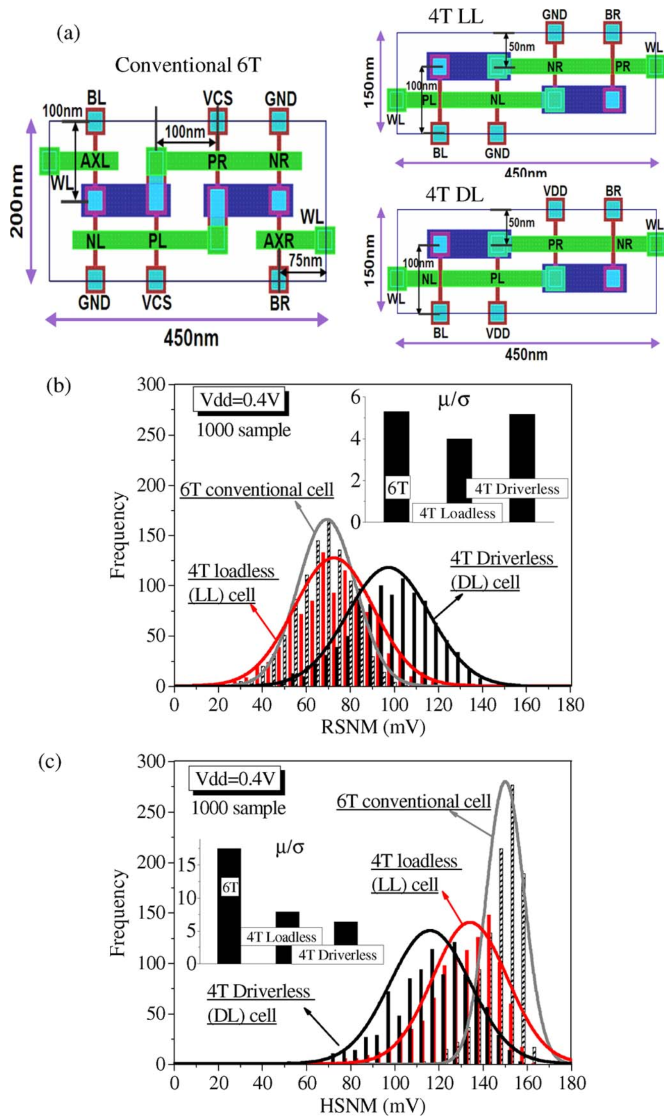

Fig. 9. (a) FinFET cell layouts for the conventional 6T, 4T LL, and 4T DL cells with identical device sizes. (b) and (c) RSNM/HSNM variability comparisons of the cells [see (a)] with the same device sizes ($L_{\text{eff}} = 25$ nm and $W_{\text{fin}} = 7$ nm).

design rules from the published 32-nm technologies [19] and the scaling factor from the International Technology Roadmap for Semiconductors roadmap. Compared with the 6T cell, the 4T cells show 25% area reduction.

Fig. 9(b) illustrates the RSNM variability of the cells with 1000 samples for the same device sizes. Owing to the worse electrostatic integrity of independent-gate operation, 4T SRAM cells show broader dispersion, thus larger σRSNM. If we target the value of the μ/σ ratio to be 5–6 for robust cell design, the calculated μ/σ ratio of the 4T DL cell, with a larger/better nominal RSNM and a slightly larger/worse σRSNM, is comparable to the 6T cell and meets the requirement. The hold static noise margin (HSNM) variations are also assessed [see Fig. 9(c)] for various cells. It can be seen that HSNM, with a larger μHSNM, is better, as expected in general.

If the cells are compared based on the same cell area (chip density), 4T SRAM cells with fewer transistors have the flexibility of relaxing device size and the potential of reducing variations. Fig. 10(a) illustrates the layouts for 6T and relaxed 4T SRAM cells with comparable cell areas. The transistor size in 4T SRAM cells can be loosened from $(L_{\text{eff}}, W_{\text{fin}}) = (25\text{ nm}, 7\text{ nm})$ to (32 nm, 10 nm) with identical subthreshold slopes. In Fig. 10(b) and (c), the variability of RSNM/HSNM for 6T and relaxed 4T SRAM cells is examined. As expected, the relaxed 4T cells exhibit a tighter distribution due to less variation sensitivity in the larger device. In addition, the calculated μ/σ ratios of RSNM/HSNM increase and outperform the 6T cell.

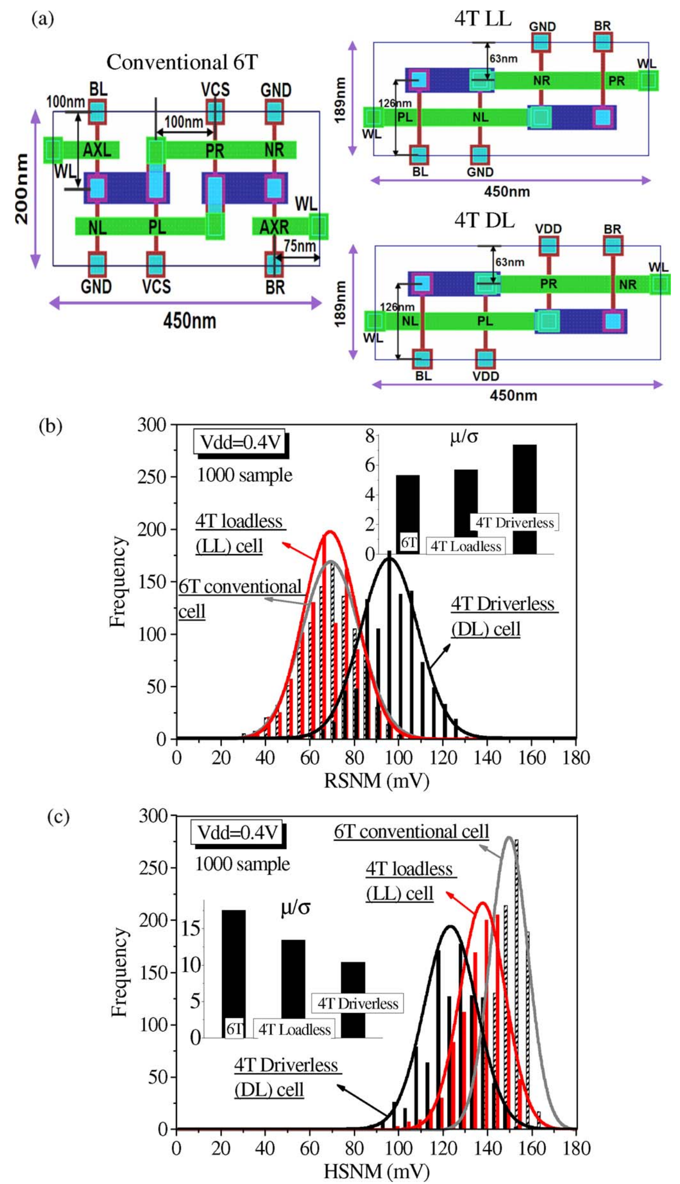

Fig. 10. (a) FinFET cell layouts for the conventional 6T, 4T LL, and 4T DL cells with identical cell areas. (b) and (c) RSNM/HSNM variability comparisons with the same cell area (4T cells with $L_{\text{eff}} = 32$ nm and $W_{\text{fin}} = 10$ nm).

In Fig. 11(a)–(c), the WSNM variations are analyzed for the 6T and reported 4T SRAM cells. For selected cells, the low value of $V_{\text{write},0}$ and the high value of $V_{\text{write},1}$ for 4T LL and DL cells guarantee successful WRITE. 4T SRAM cells exhibit a better WSNM than that for the conventional 6T cell [see Fig. 11(a)]. However, the WRITE disturb in the half-selected cells on the selected bit-line may become a concern with device

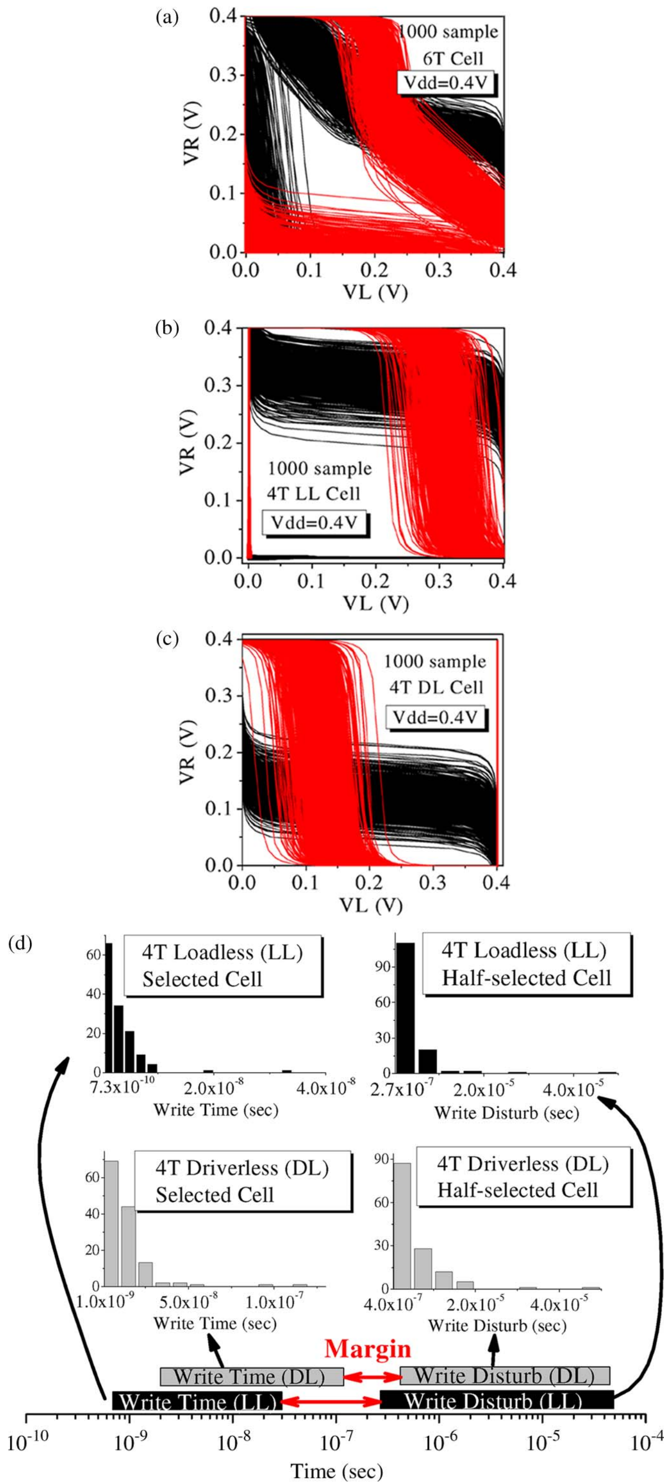

Fig. 11. Direct-current transfer characteristics of (a) conventional 6T, (b) 4T LL, and (c) DL cells during WRITE with identical device sizes. (d) Transient analysis of Write time and WRITE disturb for 4T LL and DL cells (TCAD simulations with 150 samples).

variations. Fig. 11(d) examines the WRITE time and WRITE disturb of 4T SRAM cells using TCAD transient Monte Carlo simulations. As expected, the margin between WRITE time and WRITE disturb decreases under the influence of device variations for 4T LL and DL cells. It can also be seen that the 4T LL cell exhibits a larger margin (about one order of magnitude

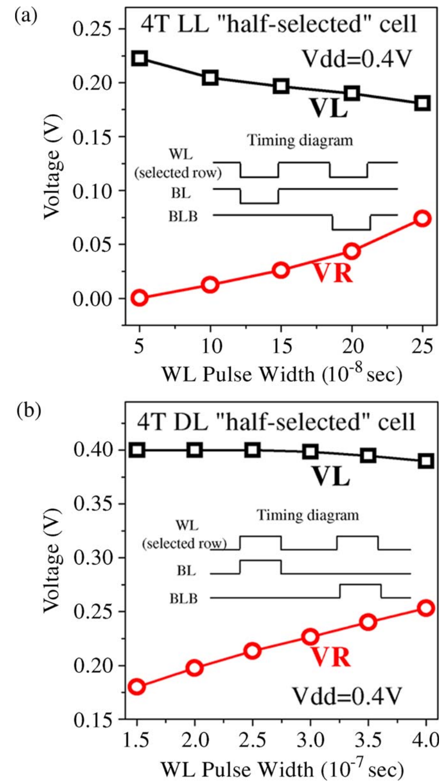

Fig. 12. Stored states in the worst-case half-selected cells with various WL pulsewidths for 4T (a) LL and (b) DL cells. (Inset) Timing diagrams.

difference between WRITE time and WRITE disturb) than the 4T DL cell.

Based on the analysis in Fig. 11(d), the WL pulse-width should be carefully controlled within the margin to maintain the data storing in the half-selected cells. In Fig. 12, the worst case (the tail of the distribution) of the half-selected cells from Fig. 11 is investigated. Fig. 12(a) and (b) illustrates the stored states in the worst-case half-selected cells and the corresponding timing diagrams with various WL pulse-widths for 4T LL and DL cells, respectively. As can be seen in the timing diagrams, in the 4T LL (or DL) cell, the WL goes to "Low" (or "High") to activate the selected row and execute WRITE operation. During the WL "ON" period, the stored states in the half-selected cells suffer WRITE disturb. The activated WL pulse-width should be properly designed to avoid the flipping of the stored states in the half-selected cells. In Fig. 12, the voltages in the stored nodes (VL/VR) of the worst-case half-selected cell at the tail of distribution are shown versus the WL pulse-width. It is found that the data stored in the worst-case half-selected cell are maintained if the WL pulse is chosen properly.

IV. Conclusion

We have employed an efficient model-based approach to consider the impact of device variations on the FinFET SRAM cell stability. Specifically, the stability of two recently introduced 4T FinFET SRAM cells has been investigated and compared with the conventional 6T cell in the subthreshold region. Owing to the reduced READ disturb, 4T SRAM cells exhibit a better nominal RSNM than the conventional 6T cell. Moreover,

the nearly ideal values of $V_{\text{write},0}$ and $V_{\text{write},1}$ guarantee the positive WSNM for selected 4T LL and DL cells. For half-selected cells on the selected bit-line, the margin between WRITE time and WRITE disturb has been assessed by TCAD simulations. The variability of the 4T and conventional 6T cells has also been assessed using the model-based approach with 1000 samples for each case. Our results indicate that the 4T DL cell with a larger μRSNM and a slightly worse σRSNM shows a comparable μ/σ ratio in RSNM with the conventional 6T cell. Furthermore, for a given cell area, 4T cells with fewer transistors have the flexibility of using relaxed device design. Thus, σRSNM can be reduced, and the μ/σ ratios in RSNM for 4T cells can outperform the conventional 6T cell. For WRITE operation, 4T SRAM cells show a superior WSNM for selected cells, whereas the margin between WRITE time (for selected cells) and WRITE disturb (for half-selected cells on selected bit-line) needs to be carefully examined to ensure an adequate margin under variability.

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