行政院國家科學委員會專題研究計畫　成果報告

跨越 KU(12-18GHZ)之 CMOS 震盪器及相關射頻元件之 IC 設計

(3/3)

計畫類別： 個別型計畫
計畫編號： NSC92-2213-E-009-020-
執行期間： 92 年 08 月 01 日至 93 年 07 月 31 日
執行單位： 國立交通大學電信工程學系

計畫主持人： 莊晴光

報告類型： 完整報告
報告附件： 出席國際會議研究心得報告及發表論文
處理方式： 本計畫可公開查詢

中　華　民　國 93 年 11 月 1 日

行政院國家科學委員會專題研究計畫成果報告

跨越 KU(12-18GHZ)之 CMOS 震盪器及相關射頻元件之 IC 設計(3/3)

Design and development of low-noise CMOS oscillators and RF components beyond Ku-band(3/3)

計畫編號：NSC 92-2213-E-009-020

執行期限：92 年 8 月 1 日至 93 年 7 月 31 日

主持人：莊晴光教授　國立交通大學電信工程學系

This work proposes a radio frequency angle modulator with a direct digital data interface using 0.18 μm CMOS technology. It consumes 42mW, occupies a chip size of 0.936 mm x 0.935 mm, and shows a measured EVM (error vector magnitude) of 0.55% at 2.468 GHz with 5.5 Mbps data rate.

Abstract:

A compact, fully integrated 5.2 GHz CMOS oscillator based on 0.25μm 1P5M foundry technology is presented. The recently proposed two-dimensional transmissionline, called complementary-conducting-strips (CCS), replaces the conventional inductor-capacitor tank circuit, resulting in a first-pass design for the CMOS oscillator, of which the simulated and measured power level and oscillation frequency agree to within 1%.

Introduction:

This report summarizes the progress in advancing arts of CMOS RFIC's (Complementary Metal-Oxide-Semiconductor Radio-Frequency-Integrated-Circuits) in three parts. Parts 1 and 2 of this report focus on two aspects that were partially reported last year. Part 1 concerns primarily on new RFIC modulator/transmitter architecture; therefore lower operating frequencies at 2.5 GHz was adopted for proof-of-concept in view of its complexity. The results show that the concept of direct data control of self-locked octant-phase oscillator offers efficient alternative to the conventional DSP implementation of digital modulation followed by RF carrier translation to any desired RF channel [1]. Part 2 investigates feasibilities and potentials of a new guiding structure called complementary-conducting-strips (CCS) as a main transmission line element that constitutes passive circuits and matching networks necessary for extending the CMOS RFIC into X band and beyond [2-3]. The results, not reported here, have also been diverted to the research and development of miniaturized W-band GaAs transceiver RFIC chipset with more than 80% chip area reduction. Part 3 presents theoretical data, partially disclosed to the 2003 APMC (Asia-Pacific Microwave Conference) recently, that reflects the continuing works of year 2002 in PBG (photonic band gap) inductor that demonstrated CMOS inductor of Q near 10 be attainable with good substrate shielding [4]. Here we show how complex modes may exist in the stopband of periodical arrays and why they can't propagate electromagnetic energies in the stopband [5]. With obtained properties of complex modes in the stopband, this report will briefly explain the on-going research activities applying these complex modes for low phase-noise oscillator designs at various frequency bands.

Part 1: Direct Radio-Frequency Digital Angle Modulator [1]

Aim and Conventional Approaches:

The digital radio frequency (RF) modulator has been the backbone of modern radio communication systems, for which linear modulation and angle modulation are two widely applied modulation schemes. Linear modulation involves the amplification of the amplitude of an information signal. Angle modulation, however, projects the instantaneous signal vector

in polar coordinates onto the In-phase (I) and Quadrature (Q) axes, where signals are typically up-converted and combined to form the desired modulated RF signals. While providing highly versatile modulated-carrier generation, these I/Q-based modulators of homodyne, heterodyne and harmonic-rejection types [6] require sophisticated mixed-signal electronics and microwave engineering, such as digital generation of I/Q signals, digital-to-analog converters, mixers, filters and oscillators. The second approach to the RF modulator design is the phase lock loop (PLL)-based modulators [7], which become adaptive to produce stable angle and amplitude modulations. Similarly, mixed-signal electronics are complex and the effects of environmental conditions and the aging of components must be compensated for.

Proposed Direct Digital RF Modulator:

This work proposes a direct RF modulator, which is compact for CMOS RFIC integration and is capable of processing binary data to producing angle-modulated RF signals directly. The proposed direct RF modulator is neither I/Q-based nor PLL-based architecture. Figure 1 presents the architecture and circuit of the RF angle modulator with a direct digital interface. The unmodulated, digital, raw data enter the digital encoder, which is an encoded logic that results in M digital outputs in a manner determined by the modulation scheme. The core of the generic RF angle modulator is the constellation oscillator, which has M RF output ports synchronized by RF carrier stabilizer. The RF carrier stabilizer is implemented by injecting a stable carrier into the RF angle modulator. Each RF output port of the constellation oscillator has the same frequency with different phase circling on the unit circle of the normalized constellation diagram with M states separated by $\frac{360^\circ}{M}$. For M equal to eight, the phase increment between adjacent states is 45°. As shown in Fig. 1, a constellation map controller controls the mapping of RF output ports to the modulated RF output. The constellation map controller is RF switch arrays (Sw1-Sw8) in a switched source-follower fashion that accepts the encoded M-bit (b1-b8) digital data and transfers the digital data into the desired RF output port. Only one of the M RF switches is turned on in each symbol period, yielding the desired angle-modulated RF output.

Implementation:

The constellation oscillator consists of four differential CMOS LC oscillators connected in a ring-oscillator [8-9]. It provides eight RF outputs synchronously. Thus, when locked in a synchronized oscillation state, each CMOS LC oscillator is phase shifted by 45° with complementary outputs. For the digital encoder, the FPGA (field programmable gate arrays) board is applied to encode the $\pi/4$ DQPSK and produces eight digital control bits to control the constellation map controller of the RF angle modulator. Figure 2 shows the die photo of the RF angle modulator manufactured by Taiwan Semiconductor Manufacturing Company (TSMC), using 1P6M (one poly and six metal layers) 0.18 μm CMOS technology. The chip size including pads is 0.936 mm x 0.935 mm. The constellation oscillator is enclosed by dashed line. The rectangular shapes indicate the arrays of switch, which are main components of constellation map controller and the ellipse shapes indicate the varactors.

Measurements:

The center frequency of the constellation oscillator is 2.468 GHz. The power consumption is 42 mW with a 1.8V power supply. The locking range of the varactor is around 100 MHz. The signal analyzer FSIQ7 of ROHDE SCHWARZ^{TM}, which provides a maximum data rate of 7 MHz in the demodulation of $\pi/4$ DQPSK is applied to measurements. Figure 3(a) and (b) are constellation diagram of 1 Mbps and 5.5 Mbps demodulation of $\pi/4$ DQPSK, respectively. The demodulation is combined with a raise cosine filter to provide an EVM of less than 0.55% at 2.468 GHz.

Conclusion:

Part 1 of this report presents a direct digital RF angle modulator, based on 0.18 μm CMOS technology, which does not require DAC and mixer devices. Effectiveness of the direct digital RF angle modulator is demonstrated in the measured constellation diagram with π/4 DQPSK demodulation of different data rates, using the FSIQ7 of ROHDE SCHWARZ^{TM}.

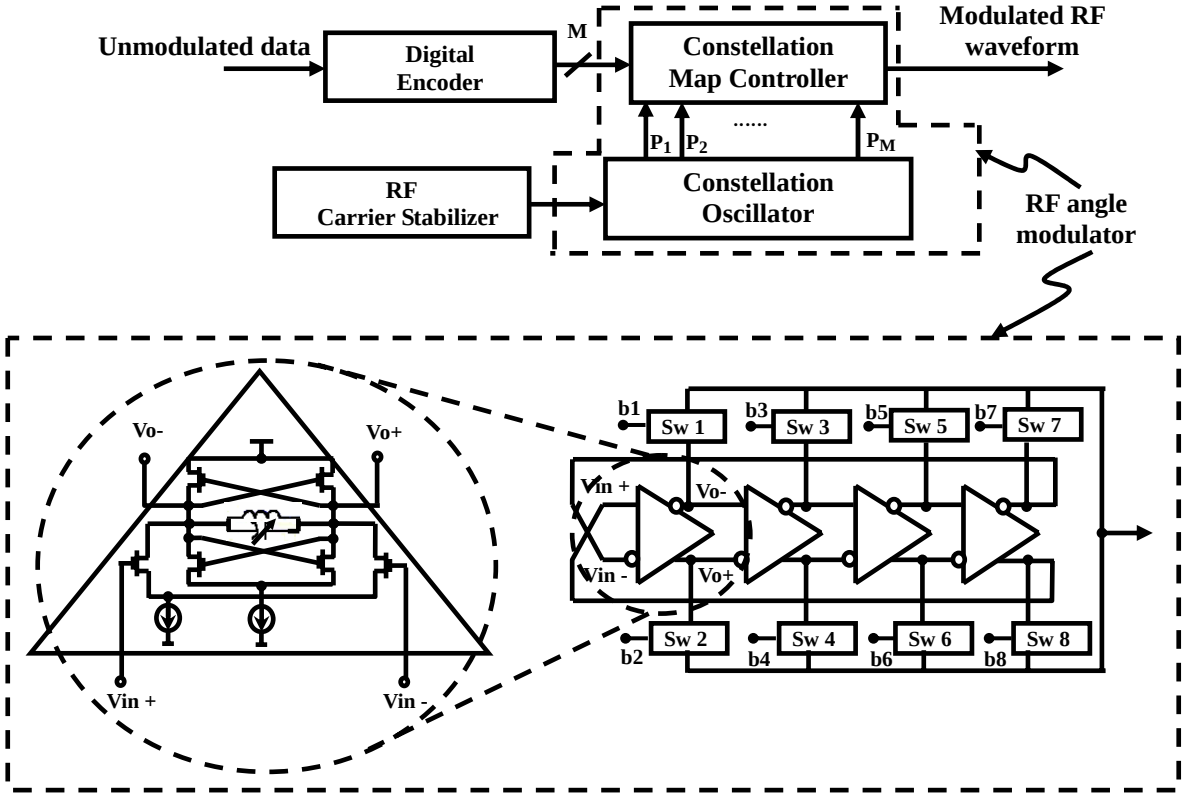


Fig. 1 The architecture and circuit of RF angle modulator with direct digital interface.

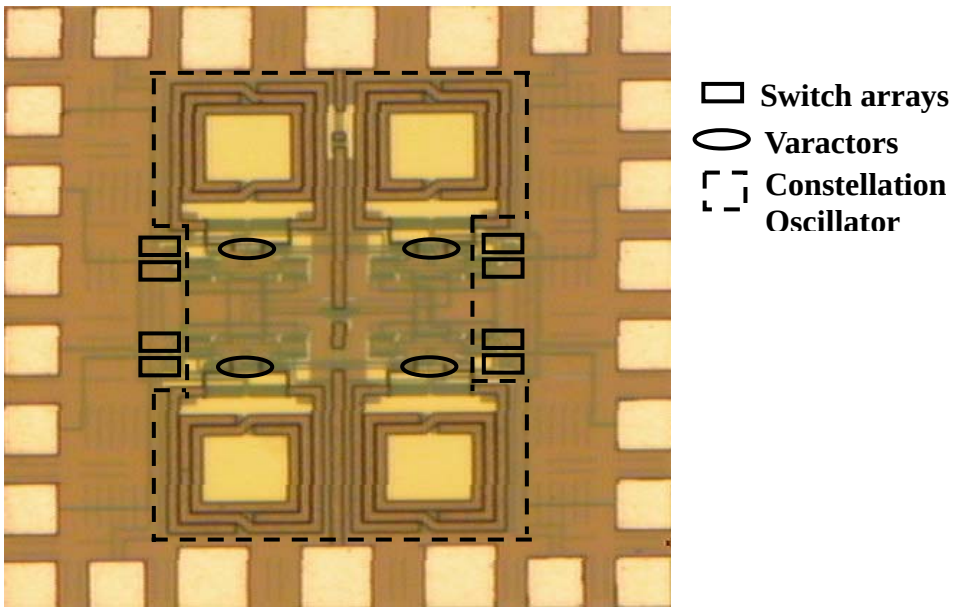


Fig. 2 The die photo of the RF angle modulator

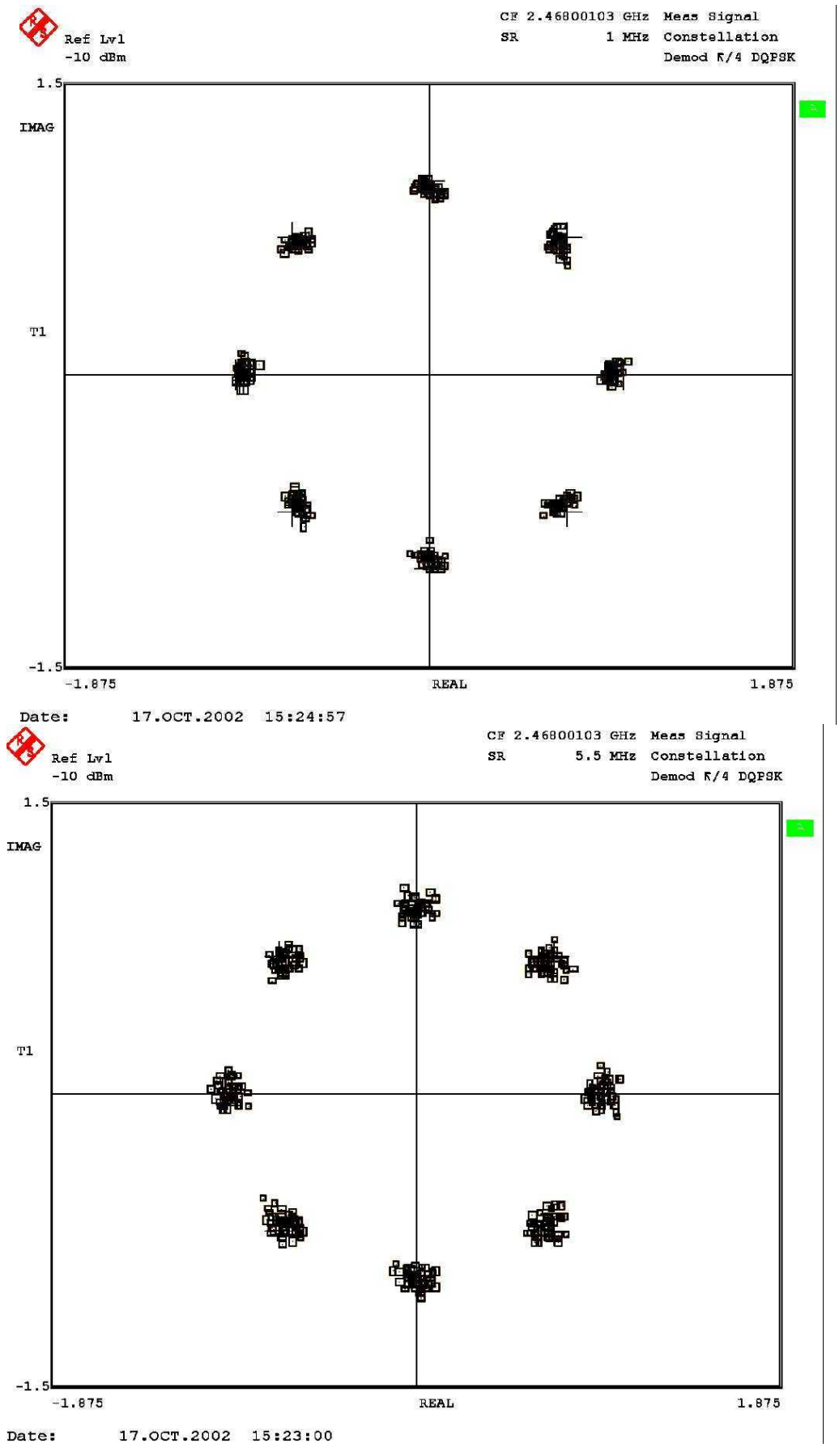


Fig. 3 Measurements of the π/4 DQPSK modulator with different data rate (a) 1 Mbps. (b) 5.5 Mbps.

Part 2: Transmission-Line-Stablized CMOS Oscillator

Aim and Conventional Approaches:

Communication system-on-chip (SOC) plays a key role for the proliferation of miniaturized products available in the market today. The trend toward the system chip integration of wireless RF equipments and devices is also inevitable in view of overall costs and labors of making them [10]. When developing communication SOC's, RFIC (radio-frequency integrated circuit) in particular, designers and managers have to decide what technology should be applied; whether III-V compound device or silicon-based IC is preferred. This project adopts the silicon RF CMOS integration of wireless communication IC's [10], since mixed-signals circuits can be integrated on the same chip. Despite that NMOS or PMOS have low breakdown voltages, transmission line and inductors are highly lossy, and substrate couplings are great concerns in CMOS technology, CMOS RFIC has increasingly gained popularity among RF designers [11]. One of the important RFIC building blocks is oscillator or voltage-controlled oscillator (VCO). To achieve low phase noise, tuned oscillator is desirable. Thus high-performance oscillator often needs high-Q (quality factor) resonator, which is not available in modern CMOS technology. If high-Q resonators are removed from monolithic integration, issues such as reliability and repeatability arise.

To date CMOS cross-coupled tuned L-C oscillator is a mature choice for fully monolithic integration of oscillator, in which the cross-coupled CMOS pairs create sufficient amount of negative conductance to compensate the losses of the low-Q LC tank circuit [12]. Accurate design of on-chip inductors and capacitors is therefore of primary importance, since RF CMOS foundry often lacks support of scalable inductors and capacitors with very limited choices. Another problem is the repeatability of the inductors and capacitors; the characteristics of these passive components may vary from lot to lot and wafer to wafer. As the operating frequency increases, the behavior of inductor is more distributive rather than lumped, as it was initially intended. This further complicates the monolithic CMOS oscillator design at higher microwave frequencies.

This project presents a CMOS RFIC guided wave structure that is fully compatible with the existing CMOS fabrication without special needs for mask change or process tuning. The proposed guiding structure has the following features: 1) The characteristics impedance of the transmission line is controlled by the unit-cell pattern in contrast to the conventional one-dimensional transmission line whose characteristics impedance is adjusted by the width of transmission line, when substrate height had been defined by foundry process; 2) The unit-cell of transmission line, having its transverse and longitudinal dimensions much larger than the height of the transmission line, makes the transmission line a two-dimensional structure, although it can be modeled one dimensionally; 3) The coupling of the adjacent cells is negligible, thereby a very compact layout of transmission line circuit is achieved.

When incorporating the proposed two-dimensional CMOS transmission line structure into the CMOS oscillator design, the LC tank of the conventional, tuned, cross-coupled CMOS oscillator can be replaced by the proposed transmission line of appropriate length as shown in Fig.4. Since the frequency of oscillation is determined primarily by the length of transmission line, not the parallel combination of inductor and capacitor, the sensitivity of oscillating frequency to process variation is largely reduced.

Next section reports the design of two-dimensional transmission line in a 0.25μm 1P5M CMOS foundry process. We then describe the LC-free CMOS oscillator design and compare the simulated and measured results followed by conclusion.

Extension of RFCMOS performance to higher microwave bands using newly proposed complementary-conducting surfaces (CCS) transmission lines:

Transmission lines such as microstrip and coplanar waveguide (CPW) have been widely applied

in GaAs or III-V-based IC's, since the semi-insulating substrates are low-loss dielectric materials and the resultant quality factors of microstrips and CPW's have acceptable Q values. This is, however, not the case for CMOS RFIC. The finite substrate losses seriously limit the Q-factor of a typical CMOS microstrip line or CPW above the CMOS SiO_2 layer to approximately six-to-ten, or even worse, depending on how the transmission line is actually built. In CMOS process, much thinner metal layers than those incorporated in III-V-based ICs are typical in standard foundry processes. This makes improvement of Q-factor of CMOS transmission line a difficult task unless the process is modified. If one raises the back plating layer of a typical CMOS microstrip to one of the five metal layers of the 1P5M CMOS technology, the resultant new thin-film microstrip will show shrinking cross-sectional geometry. Thus microstrip of much smaller width will have the same characteristic impedance as that of a much wider microstrip on CMOS substrate. The penalty of doing this is the substantial increase in attenuation constant, which can produce disastrous electric performances. Nevertheless the thin-film microstrip is still attractive [13], since certain miniaturized passive components can be integrated. This project proposes a new guiding structure that compromises guided-wave losses and size, and results in flexibility of current handling capability and choice of characteristic impedance.

Fig.5 illustrates the unit cell of one example incorporating the proposed transmission line in the LC-free CMOS oscillator. On the bottom layer is the connected unit cell as shown by the crosshatched surface, which consists of the lowest M1 and M2 layers of the 1P5M CMOS process. On the top surface of the unit cell is patterned to make a 50-Ωtransmission line for the particular application. When viewed from the cross section of the unit cell, the unit cell comprises of a raised CPW and a thin-film microstrip connected in series. The ground planes of the raised CPW and that of the thin-film microstrip are connected on the bottom metallic plane. The proposed transmission line is the series connection of such unit cells, which may have signal paths in straight line or bent fashions; thus theses cells constitute the complete guiding structure in periodic arrangement. When looking into the top surface, we observe the top metal layer and bottom metal surface complement each other; therefore we name the proposed guiding structure the complementary conducting strips (CCS) transmission line, which has been incorporated into various miniaturized RFIC designs operated at microwave and millimeter-wave frequencies. The CCS transmission line is a periodical array, along which the guided wave experiences perturbation in the longitudinal direction. Therefore the proposed guiding structure is two-dimensional, increasing degrees of freedom for designing transmission line of various characteristic impedance and current handling capability. As will become clearer in the next section, very compact layout of transmission line equivalent of LC-tank circuit can be obtained owing to the fact that the adjacent cells have negligible coupling, typically well below –20 dB of coupling.

Implementation of miniaturized CMOS RFIC free of lumped elements:

As shown in Fig.6, complementary cross-coupled transistors, M_1, M_2, M_3, and M_4, form dual positive feedback loops and generate negative conductance, which cancels the losses of the transmission line resonator. Proper sizing of transistors, NMOS 100/0.25 and PMOS 160/0.25, assures sustained oscillation. At 5.2 GHz, the capacitive loading of transistors to the resonator is fairly large and the length of transmission line resonator is reduced from half wavelength when free of loading effect to approximately one ninth of guided wavelength. As in Fig.6, the CMOS oscillator, on top of which is a 15 by 15 CCS (complementary conducting strips) array acting as a transmission line resonator, occupies 225 by 225 μm^2 area. The bottom plate of the adjacent cells connects the unit cells, thus rendering very compact layout. Total active chip area is 500 μm by 600 μm, including all the external pads.

Measurements:

The bias condition for the oscillator core is set at 20 mA from a 3 V supply. A microwave probe station with ground-signal and signal-ground probes is applied to the differential RF output ports. The output signals are attenuated before reaching the probes to prevent loading to the oscillator. An HP 8565E spectrum analyzer is used to measure the oscillation frequency and the output power. The

measured insertion loss from the probes to the spectrum analyzer is 1.53 dB at 5.2 GHz. Therefore, the measured power on the spectrum analyzer should be compensated by the probe losses. Fig.7 shows the measured output power spectrum of one RF output. The oscillation frequency is 5.2 GHz, which is 40 MHz away from the simulated frequency, and the output power is –25.3 dBm against –26.0 dBm in theory. Figure 8 plots the preliminary result for the single sideband (SSB) phase noise. The phase noise is –96 dBc/Hz at 1MHz offset from the carrier.

Conclusion:

Power spectrum measurement of the new oscillator design without use of timing reference elements using passive inductor-capacitor shows excellent agreements with the simulated results. The proposed approach incorporating the so-called complementary conducting strips transmission line sheds the light for designing high-performance, miniaturized RFIC approaching upper microwave bands with digital CMOS foundry process with mediocre RF performance as compared to good RF processes such as SiGe BiCMOS and GaAs HBT and HEMT technologies.

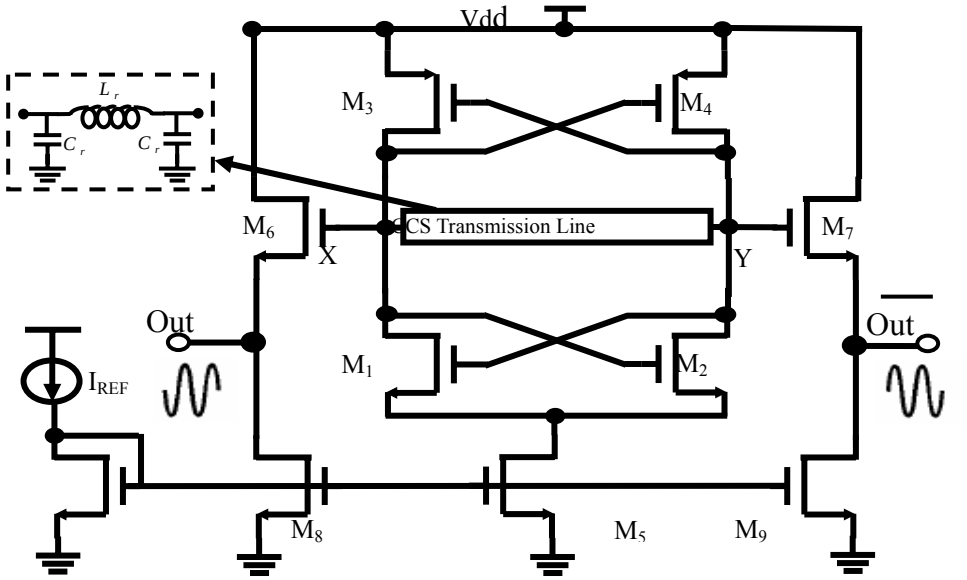


Fig. 4 CMOS oscillator employing CCS

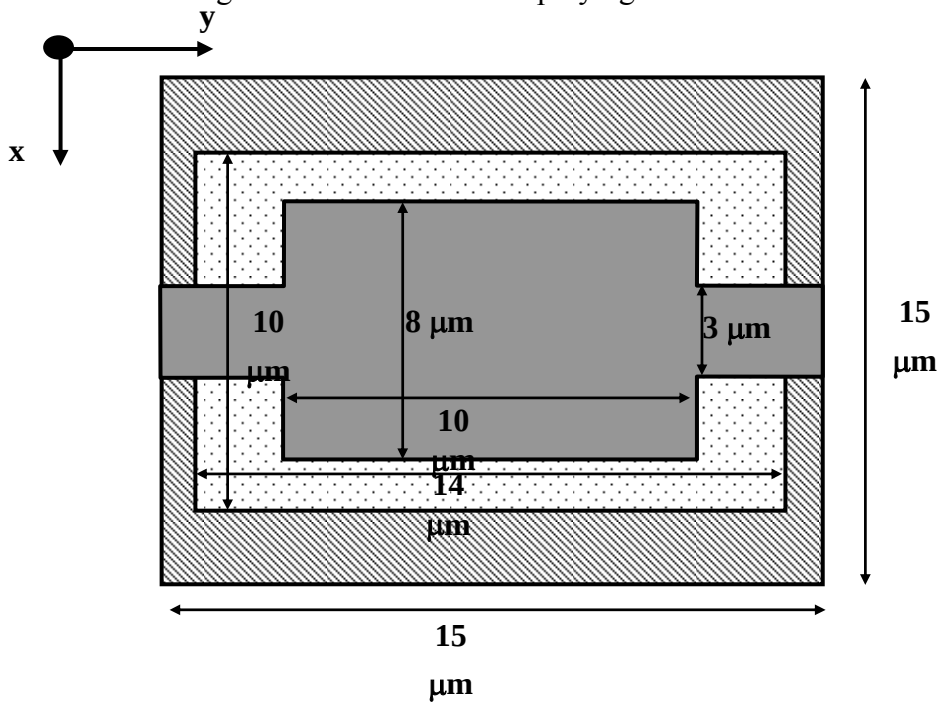


Fig. 5 Unit cell of the Complementary Conducting Strip(CCS)

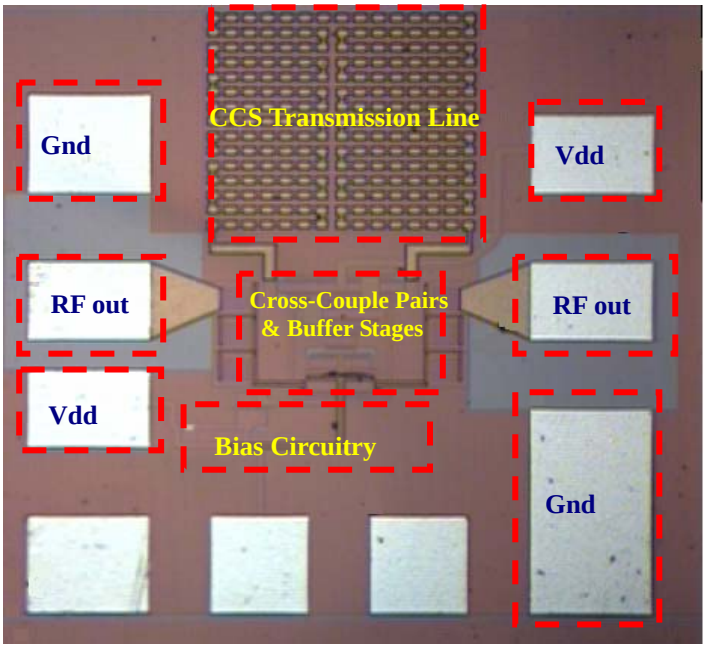


Fig. 6 Chip photograph of the fabricated oscillator

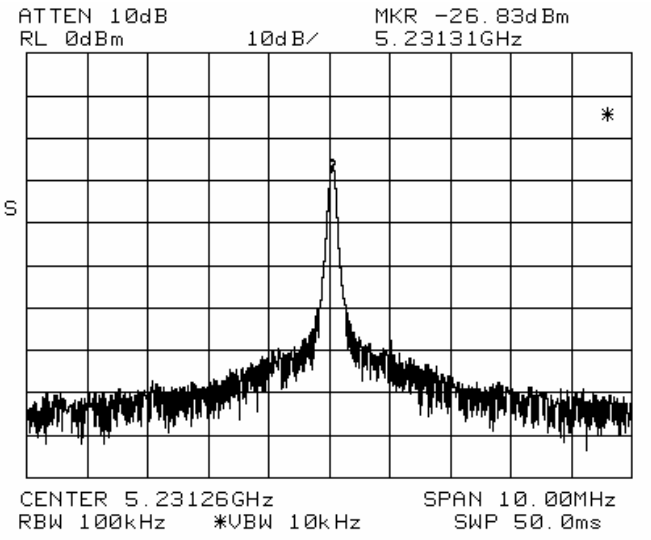


Fig. 7 Measured single-ended output power spectrum

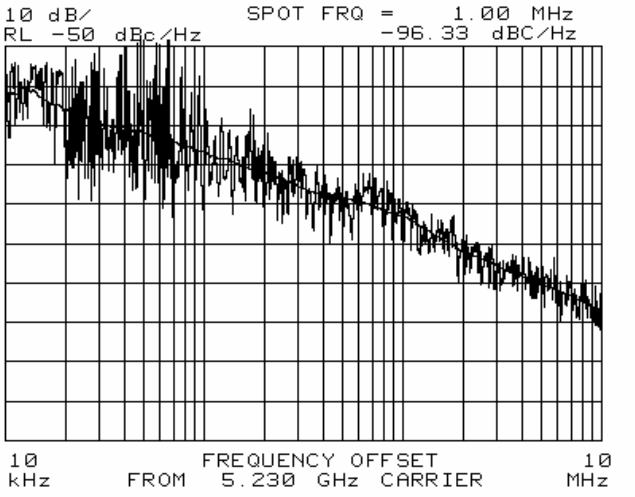


Fig. 8 Measured SSB phase noise

Part 3: Complex Modes and Orthogonal Design of High-Performance CMOS Oscillator (the on-going research and development of advanced RF CMOS technology)

The third part this report briefly discusses the recently discovered complex modes in the stopband of a periodical array [5]. As its importance is waiting for elaborate exploration, we have identified one area of application of such complex modes for advanced RF CMOS design beyond X band using the existing 0.18 mm 1P6M CMOS foundry. In the first year of this project, we reported the high-Q PBG inductor, which in every aspect, beats the conventional inductor realized by both hybrid (PCB) and monolithic (CMOS) technologies. It is interesting to note that, if we move the operating frequencies to much higher than what the previous PBG inductor structure has been meant for, the PBG transmission line will experience an entirely different phenomenon called stopband characteristics. This is, however, not new, as such stopband properties have been incorporated in many interesting microwave circuit designs [Itoh, PBG]. What is new is the fact that complex modes do exist in the stopband. Fig. 9 illustrates one such example with enlightening physical consequence and engineering application. As expected for a typical periodical structure, a one-dimensional microstrip loaded with regular, even-symmetric notches, do show a stopband near half wavelength frequency of the periodic loading. In the stopband, we locate pairs of complex modes that represent the results of mode coupling of pairs of a forward (space harmonic) wave and a backward (space harmonic) wave. Detailed analyses show that the complex waves are in the forms of $j\alpha$ +/- β and – ($j\alpha$ +/- β), where $e^{j\omega t}$ factor is assumed, and β and α respectively represents the phase constant and attenuation constant. The complex waves in complex conjugate forms resemble the complex modes in the attenuated zone with exchange of power in a reactive manner, thus no real power propagating in the guiding structure displaying very high impedance state in the stopband, which covers a broad spectrum in sharp contrast to a high-Q resonator associated with a single frequency. One significant physical consequence is that the introduction of losses in the guiding structure, regardless of the magnitude, has no fundamental effects on changing the state in which complex modes represent. This suggests complex modes are insensitive to finite conductivity of CMOS metal interconnect layers. Fig.10 shows an application of using the characteristics of complex modes and changes the conventional wisdom of making well-known complex-poles oscillator. The new low-phase noise oscillator adopts single pole design as a timing reference and the broadband resonator created by the complex modes in the stopband synchronizes the oscillator by electromagnetic coupling as shown in Fig.10, thus rendering lower phase noise than what a stand-alone one-pole oscillator can normally achieve.

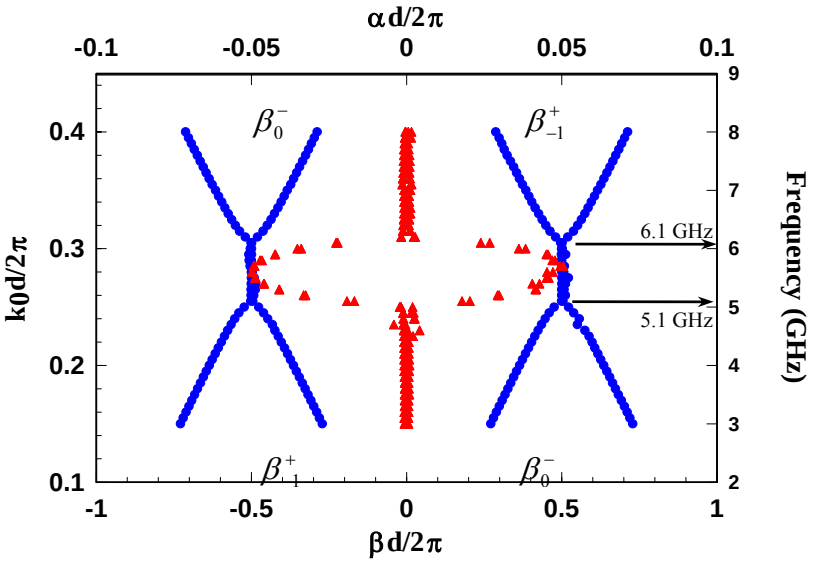


Fig.9 Complex modes in the stopband for a periodically loaded transmission line

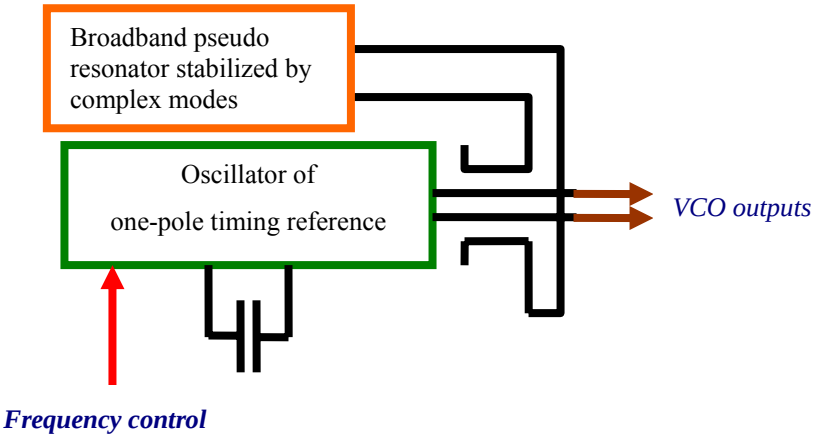


Fig.10 Block diagram for an orthogonal low-phase noise oscillator synchronized by complex-modes resonance

References:

[1] Tzu-Huei A. Ou and Ching-Kuang C. Tzuang, "Direct Radio-Frequency Digital Angle Modulator", Vol. 39, No.7 3rd, pp. 594-595, April 2003, in Electronics Letters. (89-E-FA06-2-4, NSC 90-2213-E009-063)

[2] Chih-Chiang Chen, and Wen-Yi Chien, "LC-free CMOS Oscillator Employing Two-dimensional Transmission Line",

[3] Ching-Kuang C. Tzuang and Chih-Chiang Chen, "Minlaturized Microwave Integrated Circuit Using Complementary Conducting Surfaces," under deferred publication in Taiwan's patent.

[4] Hsien-Shun Wu and Ching-Kuang C. Tzuang, "PBG-enhanced Inductor, " Proc. of the 2002 IEEE MTT-S International Microwave Symposium, PP1087-1089, we4c, Seattle, Washington, June 2-7, 2002.

[5] Yu-Chiao Chen and C-K C. Tzuang,"Stopband complex modes in microstrip with periodical perturbations," submitted to 2003 APMC

[6] Weldon J. A., Rudell J. C., Li Lin, Sekhar Narayanaswami R., Otsuka M., Dedieu S., Luns Tee, King-Chun Tsai, Cheol-Woong Lee, and Gray P. R.," A 1.75 GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, 2001, **36**, (12), pp. 2003-2015

[7] Razavi, B. " RF transmitter architectures and circuits, "IEEE Custom Integrated Circuits Conference, 1999, pp. 197 -204

[8] Ahmadreza Rofougaran, Jacob Rael, Maryam Rofougaran, Asad Abidi; " A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," IEEE International Solid-State Circuits Conference (ISSCC), February 1996, pp. 316-317

[9] Jae Joon Kim and Beomsup Kim, "A low-phase-noise CMOS LC Oscillator with a Ring Structure, " IEEE International Solid-State Circuits Conference (ISSCC), February 2000, pp. 430-431

[10] Jan. Sevenhans, Frank Op't Eynde, Peter Reusens," The silicon radio decade," IEEE MTT-T transaction, vol. 50, no. 1, pp.235-244, Jan 2002.

[11] T. H. Lee, Hirad Samavati, Hamid R. Rategh, "5-GHz cmos wireless lans," IEEE MTT-T transaction, vol. 50, no. 1, pp.268-280, Jan 2002.

[12] T. H. Lee, "The design of cmos radio-frequency integrated circuits," Cambridge University press, Chapter 16, pp.512-514, 1998.

[13] K. Nishikawa, *et al*., "Miniaturized millimeter-wave masterslice 3-D MMIC amplifier and mixer," IEEE MTT-T transaction, vol. 47, no. 1, pp.1856-1862, Sep 1999.

Part 4: Passive and Active CMOS CCS Transmission Line and It's Application

Aim and Conventional Approaches:

Advance in SiGe and CMOS technologies have made silicon-based microwave and millimeter-wave RFIC (radio frequency integrated circuit) a reality. However low resistive silicon substrate prevents the utilities of passive on-chip interconnections at millimeter-wave range. Thus, Thin Film Microstrip (TFMS) and Conductor Backed Coplanar waveguide (CB-CPW) have been popular choices. Due to the narrow separation between the signal and ground layers, nominally 3.24 μm from a 4 layer metal process SiGe HBT technology and 6.75 μm from a 6 layer metal process 0.18 μmCMOS technology. To design a 50Ω CB-CPW for the mentioned SiGe HBT technology, a very narrow signal width, about 7 μm, has to be applied to the signal trace in metal 4. And this geometrical structure is inherently to cause the high order propagating modes and results in large losses about 15dB/λg at 110 GHz [1]. For CMOS technology, a high slow-wave-factor coplanar stripline (HS-CPS) requiring no underlying ground metal had been reported recently [2]. Besides a low loss characteristic about 1.4B/λg at 40GHz is achieved. However its high slow-wave-factor, 7-8 from 1 to 50GHz, is accommodated in the cost of the embedding metal-dielectric-metal capacitor (MIM) cells. Moreover, one has to trade off the characteristic impedance with the corresponding slow wave factor by adjusting the signal line's width and the MIM cells' area. Which may cause further design difficulties.

The active filter, due selectivity and agility realized in chip, could be applied to more compact, less complex and more cost effective radar and wireless systems. Recently some well established recursive-typed topologies of GaAs technologies have been transformed to SiGe BiCMOS process [3]. The topology that adapting passive 3dB-Coupler design results in a relative large circuit area and a poor transmission gain due to the loss from silicon substrate. And the other one that adapting active-matching methods still requires a varactor-tuned LC delay network to provide a positive feedback loop. The filter's response could hardly be controlled with acceptable accuracy due to the inadequate behaviors of semiconductor devices at millimeter-wave range. Another newly proposed topology by cascading a passive low-order filter and an active interference stage does increase the selectivity of the overall filter response [4]. However, it still can't be applied to silicon technologies immediately because of the weakness of silicon lossy transmission lines. Which are essential in the passive low-order filter and interference stages of this newly proposed topology.

This project presents a synthesized High-Impedance CMOS Thin-Film Transmission lime with superior loss characteristics than the conventional Thin Film Microstrip and comparable to that of the HS-CPS under 50Ω case. Besides, our structure's characteristic impedance requires no trade-off with the slow wave factor but more flexible in choosing signal line width and layout compactness. Then we demonstrate a new CMOS active filter prototype that

requiring no artificial active matching elements and easy to integrate the active circuit components with the proposed synthesized High-Impedance CMOS Thin-Film Transmission lines.

Passive CMOS CCS TL:

The synthetic transmission line (TL) has been recently reported for realizing a miniaturized PCB (printed-circuit board) rat-race hybrid and a LC-free 5.23 GHz CMOS oscillator, respectively [5]. The synthetic CMOS TL is made of series or parallel connections of unit cells as illustrated in of Fig. 10, which in the particular case study, consists upper M5 metal layer of 1.5 μm in thickness and lower 0.53μm thick M1 metal layer. The meshed ground plane constitutes the bottom layer, whereas the connecting arms and central patch form the top layer. Both patch and meshed ground plane are in complementary arrangement and much smaller than wavelength, thus forming a complementary–conducting -strips (CCS) synthetic TL.

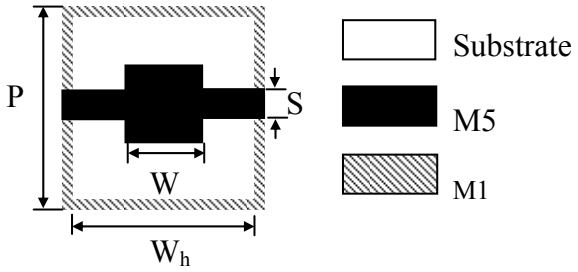


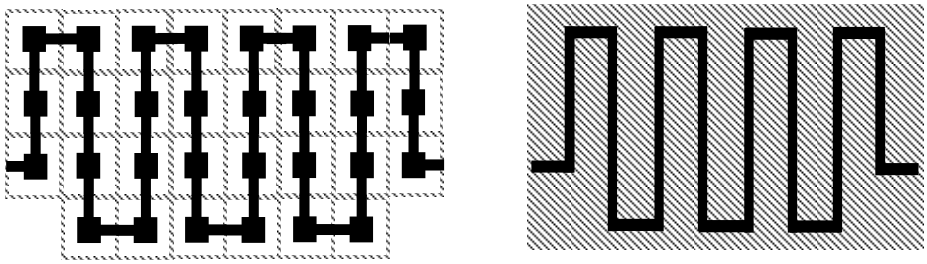
Fig.10 Unit cell of CCS TL: central patch = W mm, connecting arm = S mm, periodicity = P mm, meshed ground plane = Wh mm.

As the guided electromagnetic wave traverses the unit cells, it experiences the alternating types of guiding structures of different characteristic impedance levels in distances far less than the equivalent wavelength of the resultant transmission line. Since microstrip with and without tuning septa support quasi-TEM mode and discontinuities inherent in the unit cell is comparably small against the equivalent wavelength, the combined guiding structure of unit cell supports the quasi-TEM mode by merging two types of guiding structures. In this case the discontinuities associated with the proposed guiding structure will not cause significant radiation losses or stop-band characteristics frequently or typically observed in the periodical structures.

Furthermore, in the interested frequency range of this paper, only the quasi-TEM propagating mode dominates the guiding characteristics of CCS structures, where many

useful applications are desirable. Through proper design of CCS cells, it is capable of alleviating the drawbacks of conventional thin-film microstrips by improving the distributed inductance and reducing the losses when compared to transmission lines of equal characteristics. Another advantage of the synthetic CCS TL lies in the fact that the CCS TL is less sensitive to the meandering of TL for miniaturizing TL components.

Part (a) and (b) of Fig.11 show the comparative studies of CCS TLs and the conventional meandered thin-film microstrip. The meandered physical parameters including substrate thickness, relative dielectric constant of the substrate, and metal thickness of the two guiding structures are set according to those of the CMOS 0.25um technology. Through our analysis, for current-handing reliability concern, the smallest width (W) of the meandered microstrip TL and that of the central patch of CCS TL are 1μm. Which can sustain a maximum DC current of 1 mA.

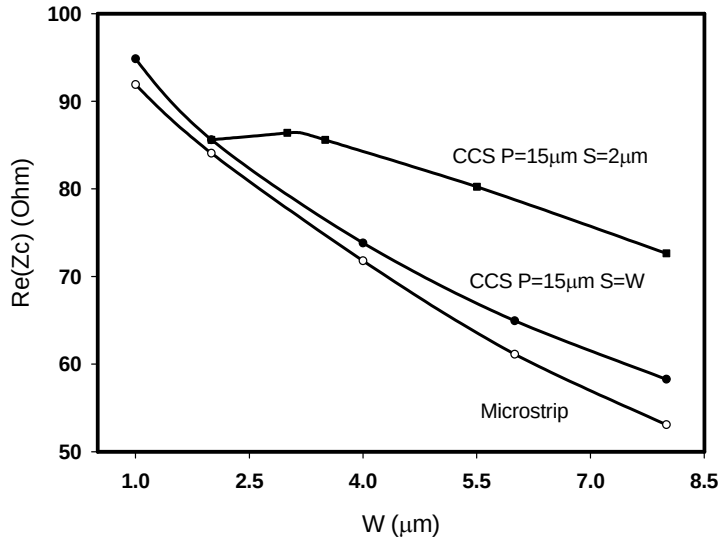


(a) (b)

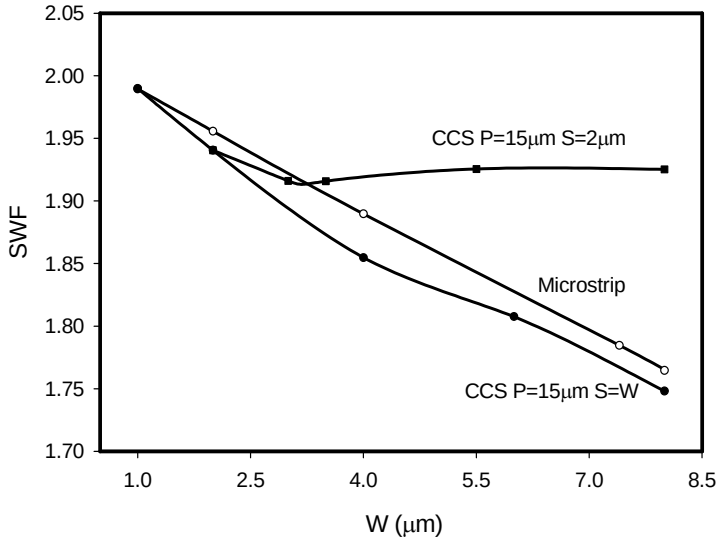
Fig.11 (a) Meandered CCS TL. (c) Meandered microstrip: line width = W μm, line spacing = P-W μm.

The flexibility of connecting arms (S) on CCS TL is investigated by two design examples. First, one assumes connecting arms (S) having a fixed value of 2μm while central patch (W) varying from 2μm to 8μm. Second, one leaves both S and W the same value ranging from 1μm to 8μm. The effective complex propagation constant and complex characteristic impedance are extracted from the equivalent complex ABCD matrix transferred from the scattering parameters [3].

Fig. 12(a) and (b) plots the real part of characteristic impedance (Re(Zc)) and slow wave factor (SWF) at 40GHz against the design parameter W of the meandered CCS and microstip TLs in Fig. 11(a) and (b), respectively. For W is 8μm, the first meandered CCS TL design example, has a 36% higher Re(Zc) than that of the corresponding meandered microstrip TL. Even W is 1μm, Re(Zc) of the second meandered CCS TL design example reaches 95 Ω and still outgoes 3% higher.



(a)



(b)

Fig.12 Characteristics of meandered CCS TL in Fig. 11(a) and meandered microstrip in Fig. 11(b) at 40 GHz. (a) Real part of characteristic impedance (Re(Zc)). (b) Slow wave factor (SWF).

Notice that the SWF of the first meandered CCS TL design example almost immunizes against the change of central patch, from 3μm to 8μm. While for the second meandered CCS TL design example, it behaves very like the meandered microstrip TL. Their increasing ratios of SWF against W are about 13%.

Fig. 13 plots the loss per guiding wavelength (dB/λg) against Re(Zc). When Re(Zc) beyond 80.24 Ω, the first meandered CCS TL design example begins to have a lower dB/λg than that of the meandered microstrip TL. For the particular case of 86.4 Ω, CCS TL's central

patch (3μm) and connecting arm (2μm) are averagely 40% much wider than the width (1.75μm) and of the comparing microstrip TL. It's dB/λg reaches the lowest value of 1.86 comparing to 2.1 of the counterpart of microstrip TL, which is an improvement about 13%. Even further shrinking central patch's width downwardly to 2μm, meandered CCS TL possesses a much stable Z_c (variation less than 1%), as shown in Fig. 12(a). At lower Re(Zc) region of Fig. 13, for instance, the second meandered CCS TL design example with 58.3 Ω is still 6% less lossy than the meandered microstrip TL.

To summarize, the observations reported in this study clearly indicate that meandered CCS TL, especially of high Re(Zc) impedance, has more advantages than conventional meandered microstrip TL including dB/λg, SWF, and design flexibility.

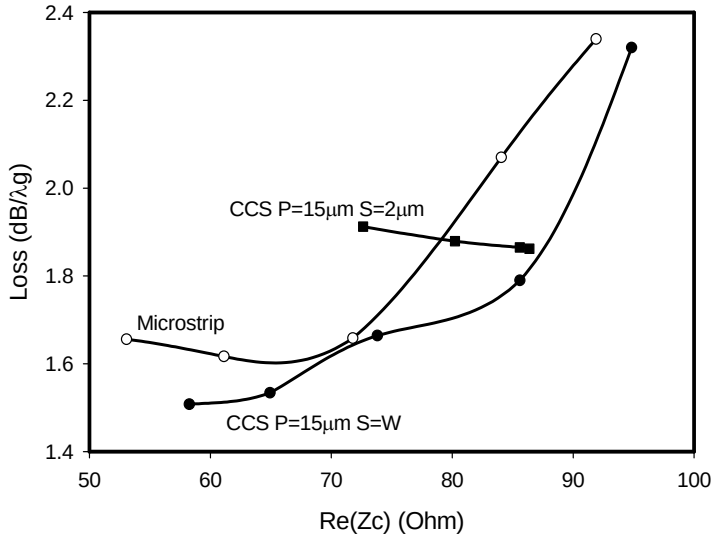


Fig13. Loss per guiding wavelength (dB/λg) of meandered CCS TL in Fig. 1(b) and meandered microstrip in Fig. 1(c) at 40 G.

Active CCS TL:

In the conventional electrical circuit theory, the four real circuit parameters C, L, G and R are used to represent the distributed shunt admittance and series impedance of a transmission line. Which are defined by $j\omega C + G \equiv \gamma / Z_o$, $j\omega L + R \equiv \gamma \cdot Z_o$, and $\gamma = \alpha + j\beta$. Where Z_o, γ, α, and β are the characteristic impedance, propagation constant, attenuation constant and phase constant respectively.

To obtain more physical understanding, as is done by [6], the R, L, G and C circuit parameters are given exactly by

$$C = \frac{1}{|v_o|^2}\left[\int_S \varepsilon' |e_t|^2 dS - \int_S \mu' |h_z|^2 dS\right], \quad (1)$$

$$L = \frac{1}{|i_o|^2}\left[\int_S \mu' |h_t|^2 dS - \int_S \varepsilon' |e_z|^2 dS\right], \quad (2)$$

$$G = \frac{\omega}{|v_o|^2}\left[\int_S \varepsilon'' |e_t|^2 dS + \int_S \mu'' |h_z|^2 dS\right], \quad (3)$$

and $$R = \frac{\omega}{|i_o|^2}\left[\int_S \mu'' |h_t|^2 dS + \int_S \varepsilon'' |e_z|^2 dS\right]. \quad (4)$$

Here $\varepsilon \equiv \varepsilon' - j\varepsilon''$ and $\mu \equiv \mu' - j\mu''$ are complex numbers relating to material properties. In passive media, the four real components ε', ε'', μ', and μ'' are positive numbers. Metal conductivity is not included as an explicit term in ε but is instead absorbed in ε''. If the guiding material is passive, then Eqs. (3) and (4) ensure that G and R are both nonnegative. For the lossless TEM transmission lines, in which $\varepsilon''=\mu''=0$, G and R vanish, as do the second integrals in C and L. Hence $\gamma = j\omega\sqrt{L \cdot C}$ is positive imaginary and $Z_o = \sqrt{L/C}$ is positive real. When the dielectric is lossy but μ'' is zero, the mode may remain TEM but a shunt conductance G, given by the first term of Eq. (3) is present. A nonzero series resistance R, given by the second integral in Eq. (4), may also appear whenever e_z and ε'' are nonzero. The integral extends over a lossy dielectric as well as an imperfect conductor, which is known as the proximity effects. C and L are typically positive for quasi-TEM propagating modes of common interest, in which the energy is primarily carried in the transverse fields and the second integrals of (1) and (2) are relative small. And Z_o could only be positive real for a lossy transmission lines when $G/(\omega \cdot C) = R/(\omega \cdot L)$ is satisfied.

However to compensate the losses of the lossy quasi-TEM transmission line, a circuit element with negative real admittance could be loaded along with the transmission line's physical structure in a distributed way. The resulting propagation constant could be derived in the very similar way as the unloaded case. Which could be easily be shown that the required negative conductance for a zero attenuation constant equals to $-(R \cdot C/L)$. When $-gm \langle -(R \cdot C/L)$, the loaded transmission line has gain, which means the attenuation constant is negative real. It should be point out that the positive real characteristic impedance for this loaded transmission line could hardly be achieved. Since the $-gm/(\omega \cdot C)$ factor

now has the opposite sign with the $R/(\omega \cdot L)$ factor. Thus the resulting $Z_o = \sqrt{(R + j\omega L)/(-gm + j\omega C)}$ always has a nonzero imaginary part.

To validate this concept, a meandered CCS TL composed of 56 CCS unit cells is implemented in the M6 and M2 metal layer of the UMC 0.18μm 6 metal layer process. The parameters of each CCS unit cell are P=30μm, S=W=10μm and W_h=28μm. Then the active circuit element is loaded with the meandered CCS TL in every three CCS unit cells as depicted in Fig. 14. The derived equivalent complex input admittance of this active circuit is plotted in Fig. 15 from 1 to 10 GHz. As a result of small biasing current, the absolute value of the negative conductance, Re(Yin), decreases 50% when frequency reaches 10GHz. However the corresponding imaginary part, Im(Yin), increases 5 times under the same condition. Which may sever degrade the overall gain of the loaded CCS transmission line at 10 GHz comparing to that at 1 GHz.

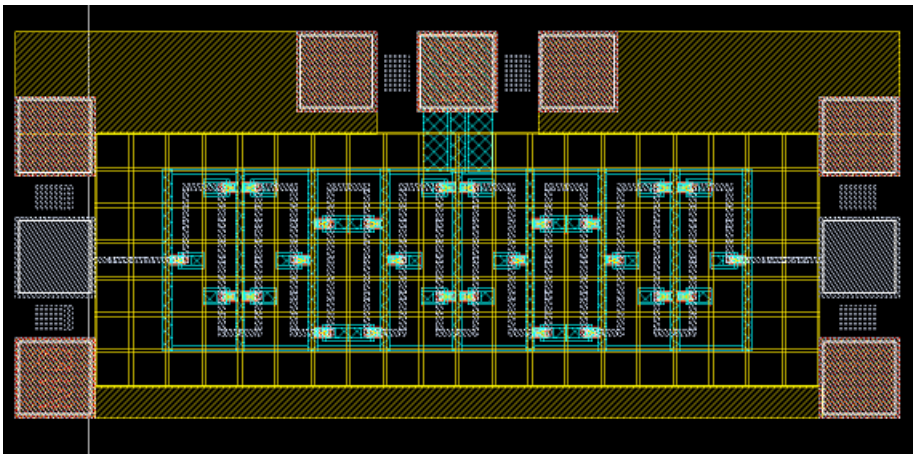


Fig14. The 0.18μm CMOS meandered CCS TL loaded with active circuit components. The parameters of a CCS unit cell are P=30μm, S=W=10μm and Wh=28μm. And the active circuit element is loaded in every three CCS unit cells.

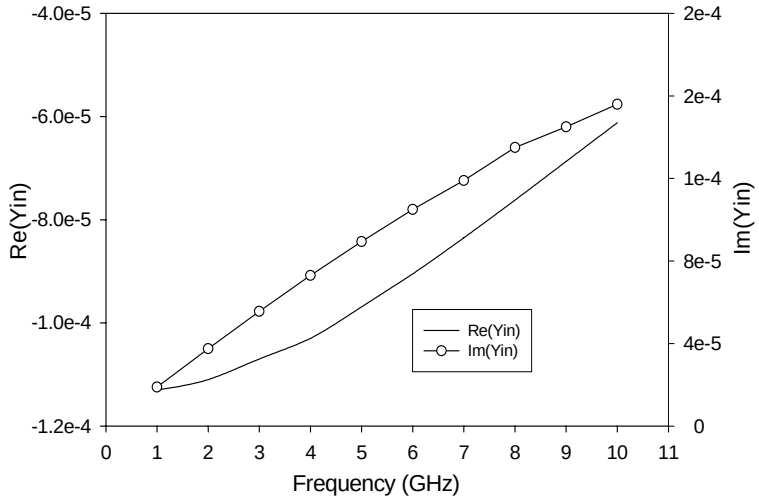
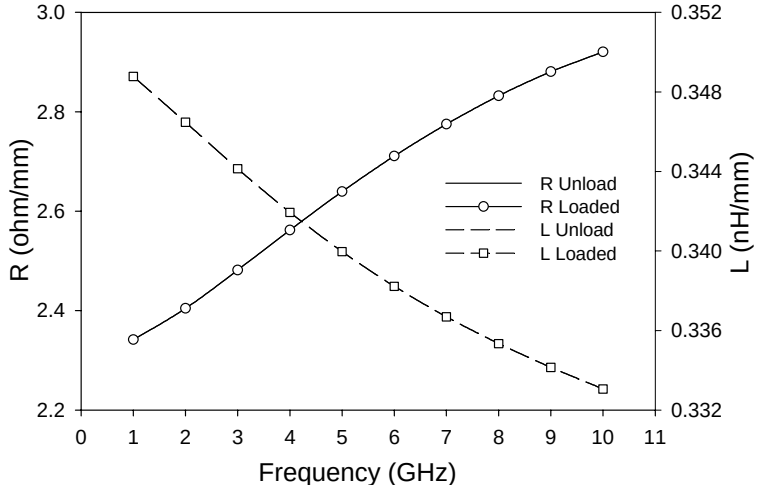
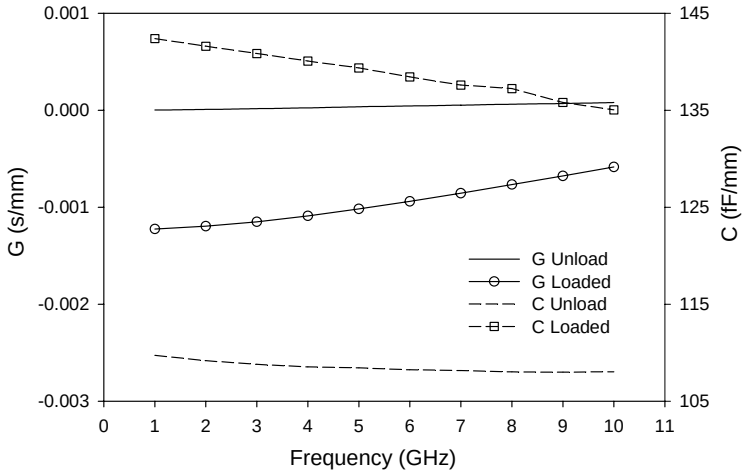


Fig15. Equivalent complex input admittance of the active circuit element apllied to the meandered CCS TL in Fig. 14 form 1 to 10 GHz.

Fig. 16(a) and (b) depicts the resistance, inductance, conductance and capacitance per unit length of the loaded and unloaded cases of the meandered CCS TL in Fig. 14. According to the above electrical circuit analysis, the distributed serial impedance, $R + j\omega L$, have negligible difference between the loaded and unload cases. But the conductance per unit length, G, decreases from zero to negative value, -0.001 s/m, due the negative conductance from the active circuit element. However the capacitance per unit length, C, increases from 107fF/mm to 140fF/mm, a 35% increment, under the same condition.



(a)



(b)

Fig16. The resistance, inductance, conductance and capacitance per unit length of loaded and unloaded cases of the meandered CCS TL in Fig. 14 from 1 to 10GHz. (a) R and L, (b) G and C.

As shown in Fig. 17 the normalized phase constant, β/ko, increase from 1.8 to 2.0 at 10 GHz. The effective gain has a drastically improvement over the entire 1 to 10 GHz frequency range. It is worthy to mention that almost a 0 dB/λg active CCS transmission line in 0.18μm CMOS technology is achieved at 5.5 GHz. Which could be further applied to many useful applications.

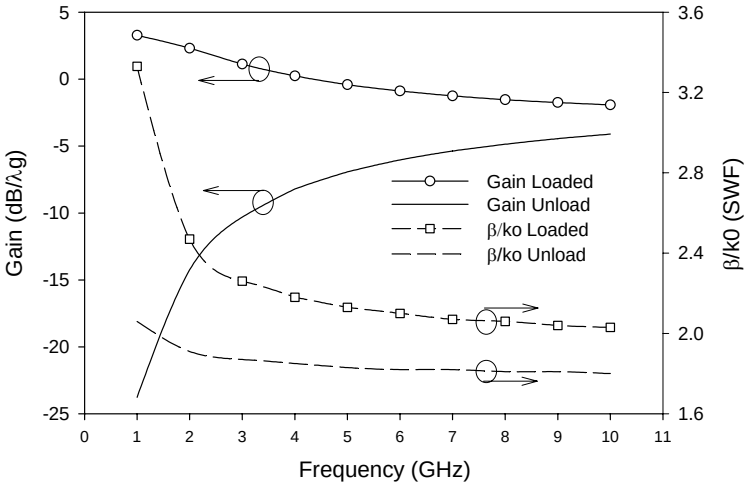


Fig17. The gain (dB/λg) and normalied phase constant (β/ko) of loaded and unloaded cases of the meandered CCS TL in Fig. 14. from 1 to 10GHz.

A Bandpass filter prototype at 5.5 GHz utilizing the mentioned active CCS TLs in CMOS 0.18μm technology is shown in Fig. 17. This active filter contains 285 active circuit

elements with a total current consumption of 42.3mA and the whole chip area about 1.24x0.96 mm^2. Fig. 18(a) and (b) plot the magnitudes and phases of S21 and S11 parameters based on a 50Ω system against frequencies form 3 to 9 GHz. There are two transmission zeros locate at 3.8 and 8.5GHz respectively. Also the center frequency gain of this active CCS transmission line band pass filter is 0 dB at 5.5 GHz.

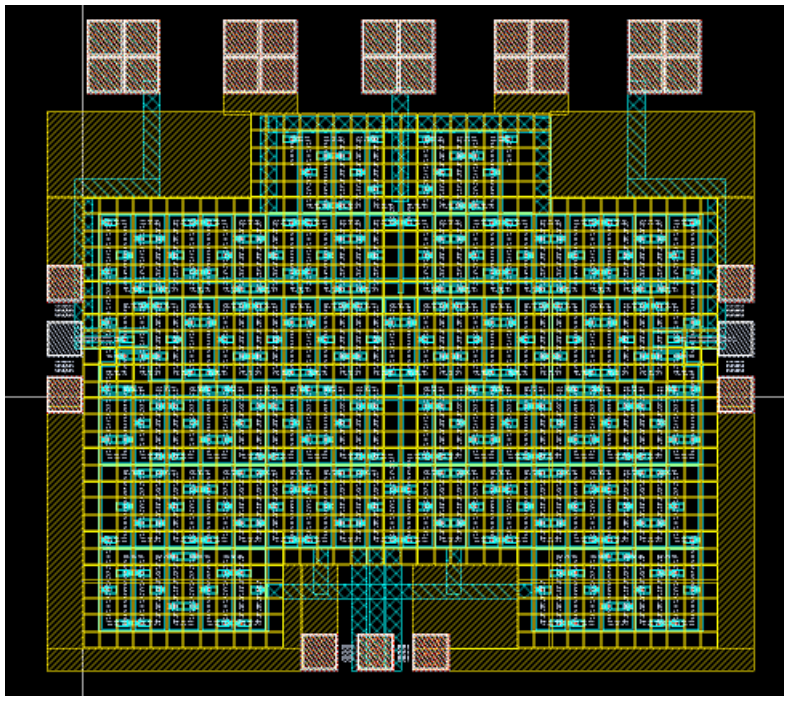
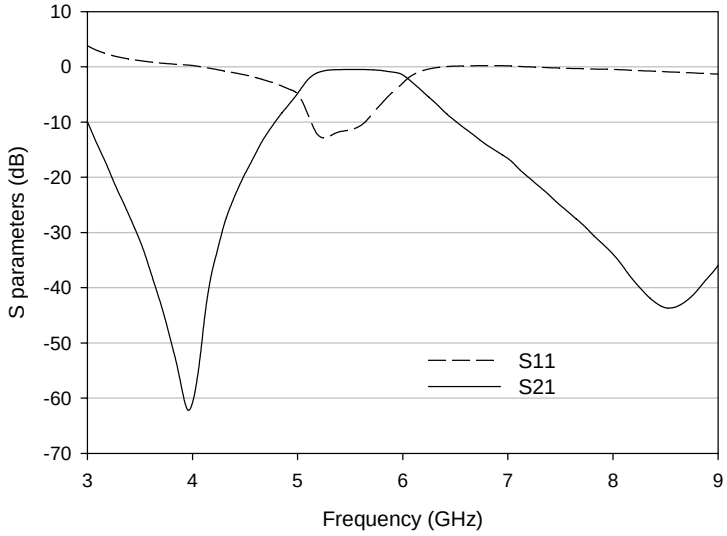
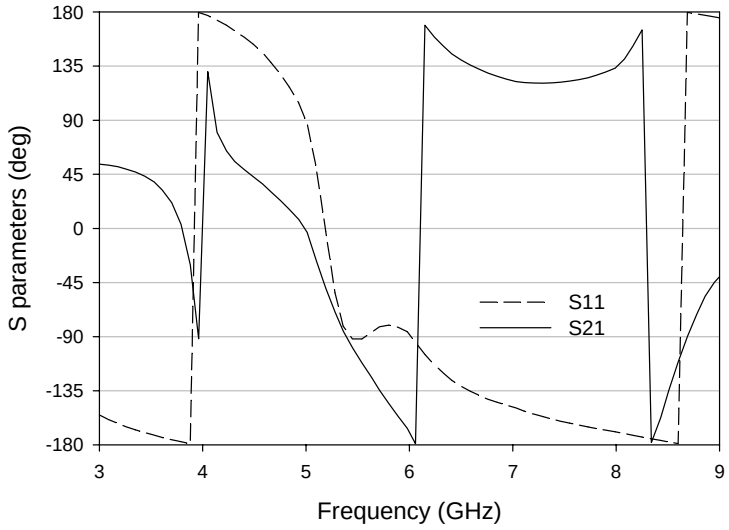


Fig17. The circuit diagram of the Bandpass filter composed of active CCS TLs in Fig. 15. The band pass filter contains 256 active crcuit elements and the chip area is 1.24x0.96 mm^2.



(a)



(b)

Fig18. The S21 and S11 parameters based on a 50Ω system of the Bandpass filter in Fig. 17 form 3 to 9 GHz. (a) magnitudes (b) phases

Conclusion:

Theoretical data at 40 GHz show that, by varying the central patch (W) from 2 μm to 8 μm, meandered CCS TL has characteristic impedance 3 % to 36 % higher than that of the meandered microstrip. Additionally, the CCS TL has loss (dB/λ_g) 13 % and 6% lower than that of meandered microstrip at Z_c of 86.4 Ω and 58.3 Ω, respectively. Implying that the optimization for obtaining high Z_c, high SWF with low loss can be achieved by designing unit cell of CCS TL with proper central patch, and connecting arms.

Also the CMOS CCS TL's loss phenomena could be further improved through loading active circuit elements with negative conductance in a distributed way. Analytic and simulation results show the resulting gain of the active CMOS CCS TL is above 0 dB/λg from DC to 5.5 GHz. The proposed configuration has been proven to be useful in the design and construction of a Bandpass filter prototype at 5.5 GHz in CMOS technology.

References:

[1] Matt Morton *et a*l., "On the Design and Implementation of Transmission Lines in Commercial SiGe HBT BiCMOS Processes," 5th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Atlanta, pp.53~56, Sep 2004.

[2] Hung-Ta Tso and Chien-Nan Kuo, "40 GHz Miniature Bandpass Filter Design in standard CMOS Process," 5th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Atlanta, pp.239~242, Sep 2004.

[3] Robert Malmqvist1, Martin Hansson2, Carl Samuelsson1, Mattias Alfredson, "Some

Important Aspects on the Design of Active Microwave Filters using Standard RF Silicon Process Technologies," 34th European Microwave Conference, Amsterdam, pp.941~944, Oct 2004.

[4] Roberto G´omez–Garc´ýa, Jos´e I. Alonso, "High–selective microwave active bandpass filter using transmission line interference sections," 34th European Microwave Conference, Amsterdam, pp.721~724, Oct 2004.

[5] Chih-Chiang Chen, Ching-Kuang C. Tzuang, "Synthetic quasi-TEM meandered transmission lines for compacted microwave integrated circuits," IEEE Trans. on Microwave Theory and Tech.,vol. 52,pp.1637~1647, Jun 2004.

[6] Roger B. Marks, Dylan F. Williams, "A General Waveguide Circuit Theory," Journal of Research of the National Institute of Standards and Technology, Vol. 97, No. 5, pp.533~562, Sep-Oct, 1992.