A Novel Random Telegraph Signal Method to Study Program/Erase Charge Lateral Spread and Retention Loss in a SONOS Flash Memory

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***Abstract*—A novel random telegraph signal (RTS) method is proposed to characterize the lateral distribution of injected charge in program and erase states in a NOR-type silicon–oxide–nitride–oxide–silicon Flash memory. The concept of this method is to use RTS to extract an oxide trap position in the channel and then to use the trap and RTS as internal probe to detect a local channel potential change resulting from injected charge during program/erase. By using this method, the lateral width of the injected charge-induced channel potential barrier is shown to be around 20 nm in channel hot electron (CHE) program. Our method also confirms that Channel Initiated Secondary ELectron (CHISEL) program has a broader injected charge distribution than CHE program. A mismatch of CHE program electrons and band-to-band tunneling erase holes is observed. Program-state V_t retention loss models, charge vertical loss versus lateral migration, are reexamined by using this method. The polarity of a program-state charge distribution along the channel is explored within 10–20 program/erase cycles. Nitride charge vertical loss is verified by this method.**

***Index Terms*—Charge lateral distribution, random telegraph signal (RTS), retention loss, silicon–oxide–nitride–oxide–silicon (SONOS).**

I. Introduction

NITRIDE-BASED trapping storage Flash memory has received much attention recently because of its immunity from stress-induced leakage current and the coupling of floating gates in conventional Flash memory [1]. Two-bit/cell NOR-type silicon–oxide–nitride–oxide–silicon (SONOS) Flash memory has been realized by storing bit charges in two sides of a channel by channel hot electron (CHE) program and band-to-band tunneling (BTBT) hot hole erase [2]. Control of program/erase charge lateral distributions of each bit is a major thrust to improve cell performance and scalability [3]. Many attempts have been made in the past to characterize a trapped charge lateral profile in a SONOS cell [4]–[11]. Two lateral profiling techniques were often used, i.e., a charge pumping (CP) method [7] and an inverse I–V modeling approach [4]. The CP method provides a direct measurement result but has the following drawbacks: First, the profiling method is based on an assumption that interface traps have a uniform distribution along the channel [12]. This assumption is not true in certain device fabrication conditions, e.g., pocket-implanted cells in a buried diffusion bit-line array, where interface traps are distributed near the source–drain junctions of a cell. Second, a CP current is hardly sensed in a small-area SONOS cell due to a few interface traps in a cell. Third, the CP profiling technique is applicable only when a charge density increases monotonically along the channel [6]. For a two-pole charge profile in erase state, the CP method is not appropriate. On the other side, the inverse I–V modeling is an indirect method. A charge lateral distribution is extracted from a 2-D device simulation by fitting the simulated subthreshold and gate-induced drain leakage characteristics to the measurement results. The inverse I–V modeling also suffers from some limitations. First, it requires the knowledge of a 2-D device doping profile in device simulation. A specific shape of a program/erase charge distribution is usually given *a priori* in simulation, e.g., a rectangular charge packet or a Gaussian-like charge distribution [4], [5]. Second, the method does not yield a unique solution. The simulated width of a program-state charge distribution varies considerably in literature, from 20–40 nm in [4]–[6] to 85 nm in [13]. In this paper, we will propose a new charge profiling technique based on random telegraph signal (RTS). This technique is very sensitive to injected electrons or holes in program/erase operation and charge loss during retention. Moreover, this technique is suitable for a small-area cell and does not need a 2-D numerical device simulation.

RTS in the channel current of a SONOS cell arises from electron emission and capture at an oxide trap near the SiO_2/Si interface. Recently, it has been recognized as a major scaling concern in Flash memories [14] since V_t fluctuations originated from a large amplitude RTS will cause a read error in a multilevel cell Flash memory [15], [16]. On the other hand, since RTS is very sensitive to a local potential change near the trap, it can be used as an internal probe to detect variation in a trapped charge density during program, erase, and retention. The waveform of RTS may exhibit two-level or multilevel switching in a current, depending on the number of traps in a

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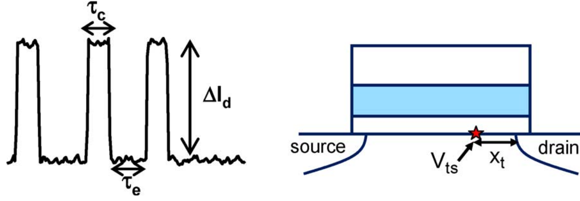

Fig. 1. Two-level RTS waveform resulting from electron emission and capture at an oxide trap. τ_c and τ_e are electron emission time and capture time. The trap position is x_t from the drain junction. The channel potential right below the trap is denoted by $V_{\rm ts}$.

device. For simplicity, only devices with two-level RTS (single trap) are chosen in this paper. In this way, we can clearly measure trap emission time and capture time. In this paper, we determine a trap position in the channel from RTS and then use the trap and RTS as internal probe to detect a local potential change due to injected program/erase charge or charge retention loss. A program charge lateral profile is obtained by collecting the measured potential changes in devices with different trap positions. By using this method, we compare the width of the charge distributions by CHE program and Channel Initiated Secondary ELectron (CHISEL) [17] program. A misalignment between CHE program electrons and BTBT erase holes will be characterized. Finally, mechanisms of program-state V_t retention loss will be reexamined by using this technique.

II. Extraction of an Interface Trap Position

Measurements were carried out on SONOS Flash cells with an ONO thickness of 8.5 nm (top oxide), 7 nm (nitride), and 5.5 nm (bottom oxide), respectively. The channel width and length are $W/L = 0.11\ \mu$m/0.1 μm. The CHE program condition is $V_{gs} = 8$ V and $V_{ds} = 3.7$ V. The BTBT hot hole erase is at $V_{gs} = -4$ V and $V_{ds} = 5$ V. RTS is measured at a small V_{ds} that the device is operated in the linear region, and the channel electric field is rather uniform. A typical two-level RTS waveform is shown in Fig. 1. The average electron capture time $\langle\tau_c\rangle$, as illustrated in Fig. 1, can be expressed as

$$\langle\tau_c\rangle = \frac{1}{{\rm n}_e \sigma \upsilon_{\rm th}} \tag{1}$$

where σ is a trap cross-section, $\upsilon_{\rm th}$ is a thermal velocity, and n_e is an electron concentration in the channel right below the trap. n_e is a function of a gate overdrive, i.e., $n_e = f(V_{gs} - V_{ts})$, where V_{ts} is the channel potential at the trap position and is equal to $(1 - x_t/L)V_{ds}$. x_t is the distance of the trap from the drain edge, and L is the channel length, as shown in Fig. 1. It should be mentioned that a uniform channel electric field is assumed here. A pocket implant may induce a nonuniform electric field. This nonuniform electric field effect, however, can be reduced by using a larger gate overdrive voltage in RTS measurement.

A trap position (x_t) in the channel can be extracted in a way similar to [18]. Two different drain voltages ($V_{ds} = 0.05$ V and 0.3 V) are used in RTS and $\langle\tau_c\rangle$ measurement. Since τ_c depends on the electron concentration n_e or a voltage drop between the gate V_{gs} and the channel right below the trap $V_{\rm ts}$, the amount of the lateral shift of these two curves $(\Delta V_{\rm ts})$ in Fig. 2 is equal to

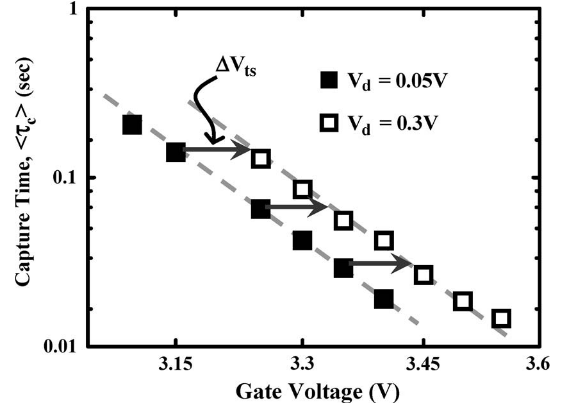

Fig. 2. Gate voltage dependence of the average capture time in RTS at two drain voltages $V_{ds} = 0.05$ V and 0.3 V. The lateral shift of these two curves corresponds to $\Delta V_{\rm ts}$.

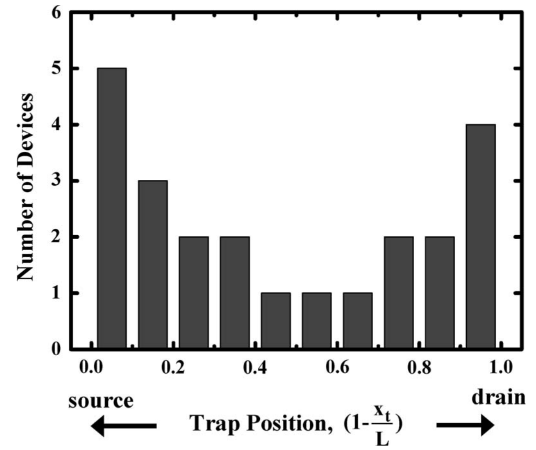

Fig. 3. Cumulative trap position distribution along the channel. $L = 0.1\ \mu$m is the channel length, and x_t is the distance of a trap from the drain.

the difference of the voltages at the point of the trap x_t, which is raised by the two drain voltages. Therefore, the trap position in the channel can be extracted from $\Delta V_{\rm ts}/\Delta V_{ds} = 1 - x_t/L$. In this paper, the RTS extraction is conducted in more than 150 fresh cells. For simplicity, we only record devices with two-level RTS (i.e., a single trap). The trap lateral position distribution along the channel is shown in Fig. 3. In fresh SONOS cells, more process-induced interface traps are found near the source–drain junctions. The trap vertical positions, which are extracted by using a method in [19], are within a distance of 0.9–1.5 nm from the Si/SiO_2 interface. With the information of a trap position in each device, we choose devices with appropriate trap positions as internal probes to investigate program/erase charge lateral spread. The local channel potential at the trap position can be extracted from the ratio $\langle\tau_c\rangle$ to $\langle\tau_e\rangle$ in RTS according to the following equation:

$$\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle} = g \exp\left(\frac{E_T - E_F}{kT}\right) \tag{2}$$

$$\frac{\left.\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle}\right|_{\rm prog}}{\left.\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle}\right|_{\rm fresh}} = \exp\left(\frac{q\Delta\varphi_s}{kT}\right) \tag{3}$$

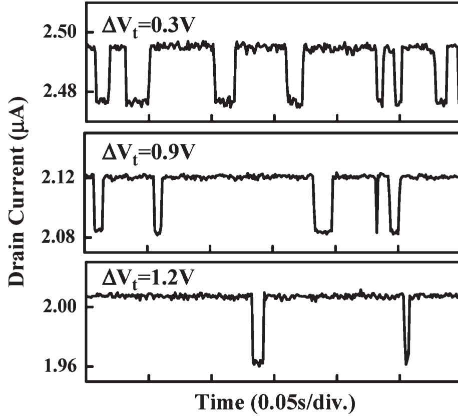

Fig. 4. RTS patterns at three program $\Delta V_t = 0.3$, 0.9, and 1.2 V in a CHE program cell. The RTS measurement condition is $V_{gs} = 3.5$ V and $V_{ds} = 0.05$ V. $x_t = 0.2L$.

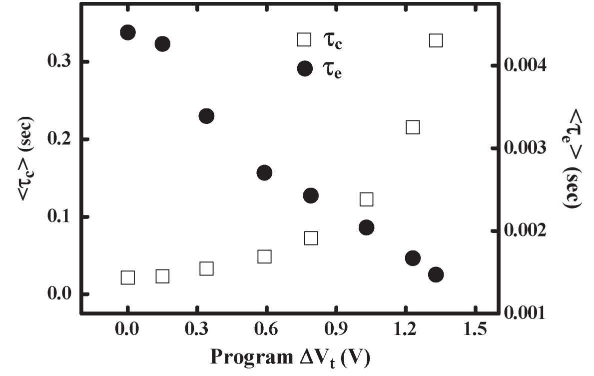

Fig. 5. Average capture time τ_c and emission time τ_e versus program ΔV_t in a $x_t = 0.2L$ cell.

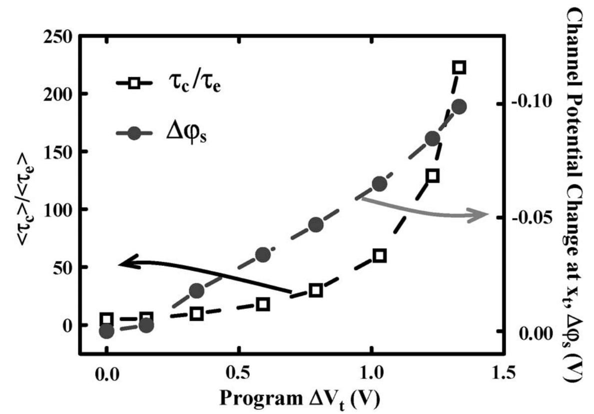

Fig. 6. Ratio $\langle\tau_c\rangle/\langle\tau_e\rangle$ and a local surface potential change ($\Delta\varphi_s$) at the trap position ($x_t = 0.2L$) versus program ΔV_t. The local potential change is calculated from (3).

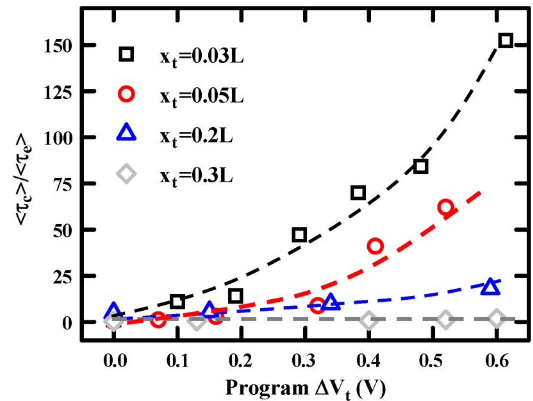

Fig. 7. Evolutions of $\langle\tau_c\rangle/\langle\tau_e\rangle$ with program ΔV_t at four different trap positions $x_t = 0.03$, 0.05, 0.2, and 0.3 L.

where g is a degeneracy factor [20], [21]. E_T is a trap energy, and $\Delta\varphi_s$ is a local potential change at the trap position due to injected program charge. The trap energy does not need to be known. In this paper, it is the ratio of $(\langle\tau_c\rangle/\langle\tau_e\rangle)_{\mathrm{prog}}$ to $(\langle\tau_c\rangle/\langle\tau_e\rangle)_{\mathrm{fresh}}$ rather than the absolute value of $\langle\tau_c\rangle/\langle\tau_e\rangle$ that matters. We extract the relative change of a trap energy level with respect to E_F from the ratio of $(\langle\tau_c\rangle/\langle\tau_e\rangle)_{\mathrm{prog}}$ to $(\langle\tau_c\rangle/\langle\tau_e\rangle)_{\mathrm{fresh}}$. Since E_F is invariant after programming, ΔE_T should be equal to $q\Delta\phi_s$. Note that (3) still holds, even though a phonon-assisted transition process is considered.

III. Results and Discussion

A. CHE Program Charge Lateral Profile

To profile the lateral charge distribution by CHE programming, four SONOS cells are used with a respective trap position at $x_t = 0.03$, 0.05, 0.2, and 0.3 L from the drain junction. Fig. 4 shows RTS traces of the channel current at three program $\Delta V_t (= 0.3\text{ V}, 0.9\text{ V}, 1.2\text{ V})$ in the $x_t = 0.2L$ cell. The RTS measurement is fixed at $V_{gs} = 3.5$ V and $V_{ds} = 0.05$ V. The device is in strong inversion at the measurement biases. The program window is limited to about 1.2 V. The reason is that the ratio of $\langle\tau_c\rangle/\langle\tau_e\rangle$ is sensitive to a local potential change and varies considerably with a program window. The $\langle\tau_c\rangle/\langle\tau_e\rangle$ might be out of a measurement range if a program ΔV_t is too large. Fig. 5 shows the measured average capture time $\langle\tau_c\rangle$ and emission time $\langle\tau_e\rangle$ versus program ΔV_t. The minimum integration time is 0.5 ms, and the total sampling period is 10 s. The observed trends in the $\langle\tau_c\rangle$ and $\langle\tau_e\rangle$ versus program ΔV_t are similar to previous results [22]. The ratio of average capture time to emission time $\langle\tau_c\rangle/\langle\tau_e\rangle$ and a corresponding surface potential change ($\Delta\varphi_s$) at x_t from (3) are plotted in Fig. 6. As more electrons are injected into the nitride layer, the conduction band edge at x_t and the trap level move upward with respect to the Fermi level. Thus, the $\langle\tau_c\rangle/\langle\tau_e\rangle$ ratio increases with ΔV_t. The measured $\langle\tau_c\rangle/\langle\tau_e\rangle$ versus ΔV_t in the four cells are shown in Fig. 7. For an x_t closer to the drain junction, e.g., the $x_t = 0.03L$ cell, the τ_c/τ_e ratio increases more rapidly with ΔV_t, implying a higher program charge density at the trap position $x_t = 0.03L$. In contrast, the τ_c/τ_e remains almost unchanged in the $x_t = 0.3L$ cell, which means that the injected program charge does not reach the trap point during program. The surface potential energy change along the channel for a program window of $\Delta V_t = 0.6$ V is presented in Fig. 8. The program charge-induced potential barrier is within 30 nm. Our result is consistent with most of published results from the inverse I–V method [4]–[6] and from Monte Carlo simulation [6], [23].

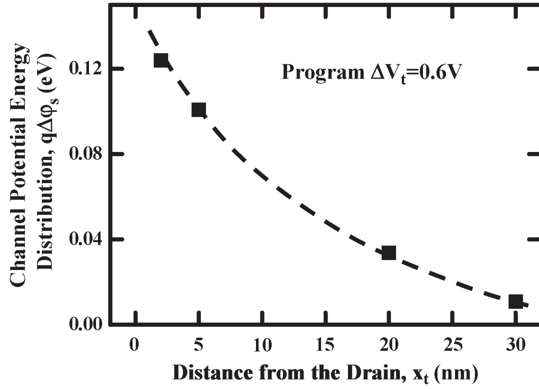

Fig. 8. Channel potential energy distribution extracted from RTS. The CHE program window is $\Delta V_t = 0.6$ V. The width of the potential energy barrier is about 20 nm.

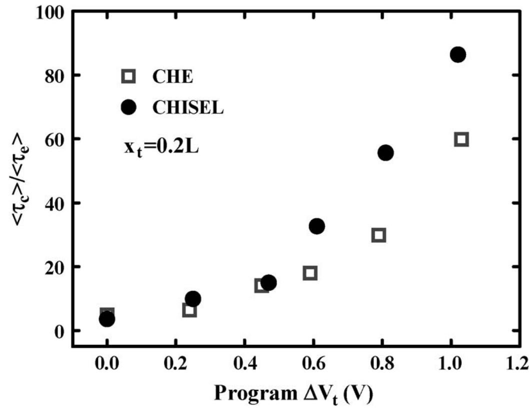

Fig. 9. Comparison of $\langle\tau_c\rangle/\langle\tau_e\rangle$ evolutions with program ΔV_t in CHE and CHISEL program. A substrate bias of -2 V is applied in CHISEL program.

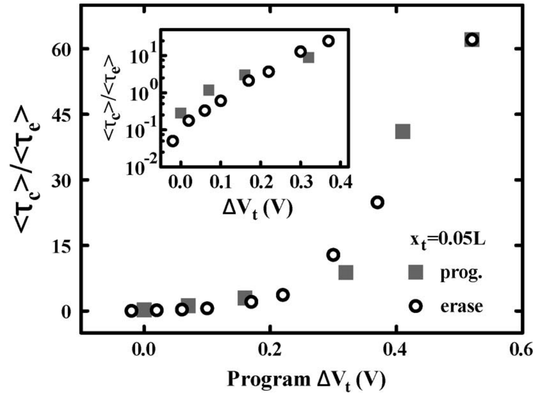

Fig. 10. $\langle\tau_c\rangle/\langle\tau_e\rangle$ versus program ΔV_t during CHE program and BTBT hot hole erase. The device has a trap at 0.05 L from the drain. The inset shows the $\langle\tau_c\rangle/\langle\tau_e\rangle$ in a log scale.

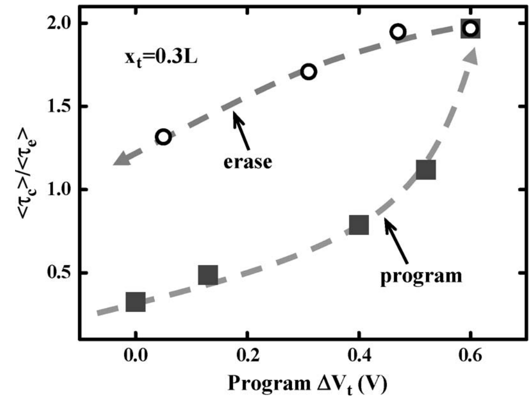

Fig. 11. $\langle\tau_c\rangle/\langle\tau_e\rangle$ versus program ΔV_t during CHE program and BTBT hot hole erase. The device has a trap at 0.3 L from the drain.

B. CHE Versus CHISEL Programming

To compare the width of injected charge by CHE and CHISEL program [23], a SONOS cell having a trap at $x_t = 0.2L$ is used. The device is programmed by CHE first. The ratio of τ_c/τ_e versus a program ΔV_t is recorded. Then, the device is erased and reprogrammed by CHISEL. In CHISEL program, a substrate bias of -2 V is applied. Fig. 9 shows the evolution of τ_c/τ_e with ΔV_t by CHE and CHISEL. The τ_c/τ_e ratio increases more quickly by CHISEL than by CHE. This means that the local channel potential at $x_t = 0.2L$ is affected by injected charge earlier in CHISEL program as ΔV_t increases. In other words, the program charge has a broader distribution in CHISEL than in CHE program at the same program ΔV_t. Our findings here are consistent with the result in [24].

C. CHE Program/BTBT Erase Charge Mismatch

In this section, we discuss the lateral misalignment between CHE program electrons and BTBT erase holes. To this purpose, we choose two devices with a trap located at the position of 0.05 and 0.3 L, respectively, from the drain junction. The two devices are programmed by CHE and then erased by BTBT hot holes. Figs. 10 and 11 show the evolution of the τ_c/τ_e during program and erase in the two devices. The τ_c/τ_e increases with a program ΔV_t and then decreases during erase. In Fig. 10, our monitor point is at $x_t = 0.05L$ in the channel. The τ_c/τ_e curves during program and erase match reasonably well, suggesting that program electrons at 0.05 L can be totally neutralized by erase holes. To examine the charge polarity in erase state, the τ_c/τ_e near $\Delta V_t = 0$ V is redrawn in a log scale in the inset of Fig. 10. The erase state τ_c/τ_e is actually lower than its value in a fresh state. This result provides evidence of hole accumulation near the drain junction in erase state. This phenomenon becomes more pronounced in an over-erased cell, i.e., $\Delta V_t < 0$ V. On the contrary, in Fig. 11, where the monitor point is at $x_t = 0.3L$, the τ_c/τ_e ratio is significantly above its original value after a program/erase (P/E) cycle. The larger τ_c/τ_e value after one P/E cycle implies the existence of some residual program electrons at $x_t = 0.3L$ although the cell has been erased to its original V_t. Combining the results in Figs. 10 and 11, the charge distributions in program and in erase are depicted in Fig. 12. A misalignment of injected erase holes and program electrons [13], [25] is concluded.

D. Program Charge Retention Loss

Two types of models have been published to explain the observed program-state V_t retention loss in a SONOS cell. The first one is nitride charge vertical loss through P/E cycling-induced oxide traps [26]–[30]. The second type of the models explains the V_t retention loss by lateral redistribution of nitride

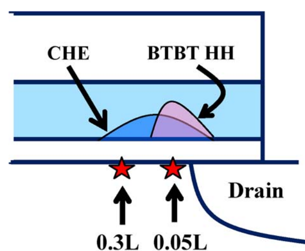

Fig. 12. Program/erase charge distributions in the channel. The stars represent oxide traps. The program electrons at $x_t = 0.05L$ are completely compensated, but some far electron at $x_t = 0.3L$ are not compensated by erase holes.

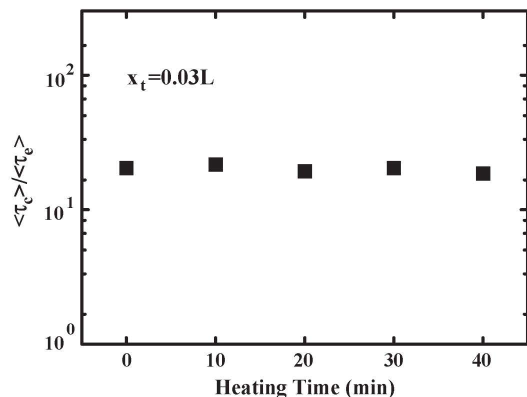

Fig. 13. $\langle\tau_c\rangle/\langle\tau_e\rangle$ in a program-only cell versus bake time. The x_t is 0.03 L. The bake temperature is 120 °C. The program ΔV_t is 1 V.

charges in program state [31]–[34]. The possibility of program electron lateral movement [34] is explored by the RTS method in Fig. 13. The cell has only one-time program and is then subject to high-temperature bake. The trap position is at $0.03L$ from the drain. The result shows that the τ_c/τ_e remains the same during the bake, indicating that the program electron concentration is unchanged. Another explanation for a program-state V_t loss is nitride trapped hole lateral migration. A three-pole electron–hole–electron distribution in program state has to be assumed in the hole lateral migration models [31]–[33]. We use the RTS method to examine the charge polarity along the channel in program state. The trap position (monitor point) in measured devices spreads from the drain junction to 0.4 L into the channel. We measured program-state and erase-state RTS at different P/E cycles. Fig. 14 shows the program state and erase state τ_c/τ_e versus P/E cycles in an $x_t = 0.05L$ device. At other x_t, the τ_c/τ_e dependence on P/E cycle has a similar feature, and the result is not shown here. The maximum cycle number in Fig. 14 is 16. The reason is that the RTS pattern becomes complex at more P/E cycles due to new oxide trap creation. In our monitored range of P/E cycles, program state τ_c/τ_e is always above its original value, showing a negative charge polarity in all the measured cells. We do not find any evidence of positive charge (hole) accumulation in program state at least within 10–20 P/E cycles. However, we would like to point out that a program-state charge profile may vary with operation biases, device doping profile, and P/E cycling conditions [33]. Although there is no sign of hole accumulation within 10–20 P/E cycles in the present operation conditions, we still observe an apparent charge retention loss in these cells

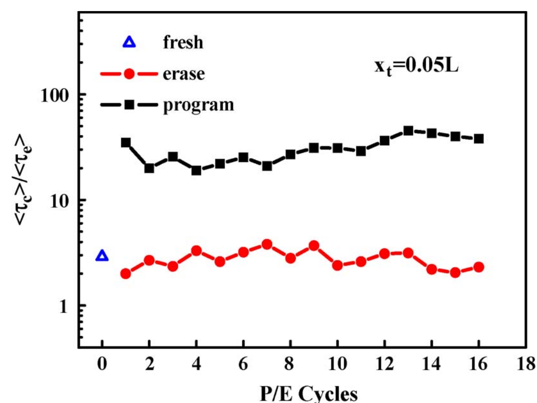

Fig. 14. Program state and erase state $\langle\tau_c\rangle/\langle\tau_e\rangle$ at different P/E cycles. The x_t is 0.05 L. The $\langle\tau_c\rangle/\langle\tau_e\rangle$ in fresh state is also shown in the figure. The program ΔV_t is 1 V.

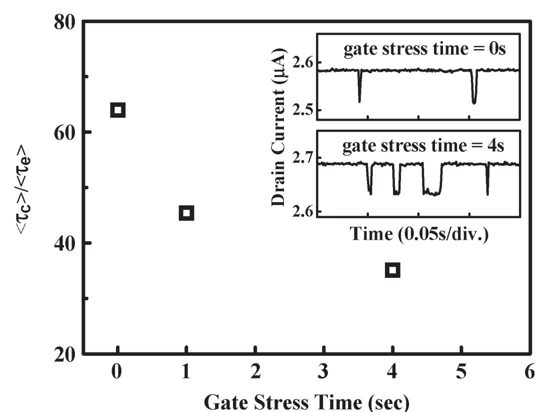

Fig. 15. Program state $\langle\tau_c\rangle/\langle\tau_e\rangle$ is plotted against gate stress time. The program ΔV_t is 1 V. The P/E cycle number is 18. The gate stress voltage is $V_g = -5$ V. The trap position x_t is 0.05 L. RTS waveforms immediately after program and after 4-s gate stress are shown in the inset of the figure.

under a gate stress condition ($V_g = -5$ V) in Fig. 15. The τ_c/τ_e ratio decreases with gate stress time. RTS traces immediately after program and after 4-s gate stress are presented in the inset of Fig. 15. The observed decrease in τ_c/τ_e is attributed to charge vertical loss, i.e., stored electron emission through the bottom oxide. Fig. 16(a) shows the read current variation versus gate stress time in a 33-P/E-cycled cell. The setup for this measurement is shown in Fig. 16(b) [16]. An electronic switch is used to accurately record gate stress time. The sampling rate is 10 kHz, which enables the observation of read current switching with a time resolution up to 0.1 ms. Both RTS and long-term nitride charge escape are observed. Individual nitride charge loss is manifested by a long-term abrupt increase in a read current. During two consecutive nitride charge escapes, RTS is observed. It should be stressed that the "average" read current level remains constant between two consecutive nitride charge emissions. This stepwise evolution characteristic provides an evidence of the vertical charge loss. One major argument in [32] against the vertical loss model is that "the bottleneck of the carrier loss is either the tunneling or the Frenkel–Poole (FP) detrapping." This argument is misleading since they did not consider the recapture of nitride conduction band electrons into nitride traps before tunneling out through the bottom oxide. By taking into account the recapture process,

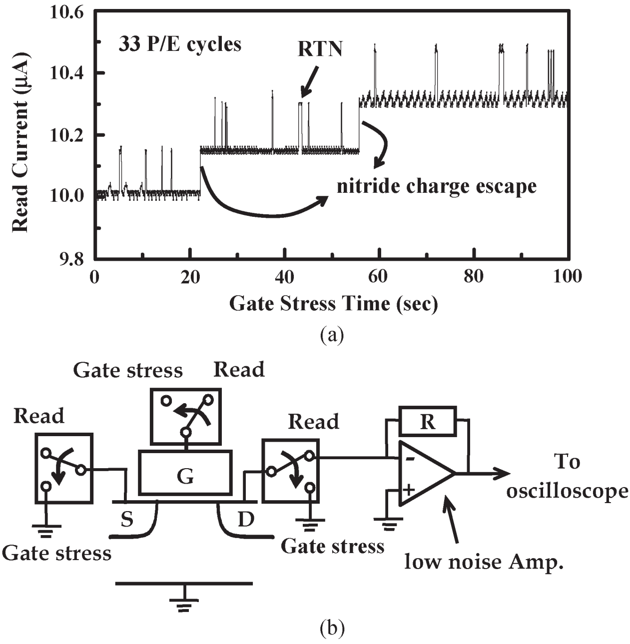

Fig. 16. (a) Read current variation with cumulative gate stress time in program state. The P/E cycle number is 33. (b) Experimental setup for read current measurement. The measurement consists of two alternating phases, i.e., a gate stress phase and a read phase. In gate stress, a negative gate voltage (-3.5 V) is applied to accelerate nitride charge loss. The sampling rate is 10 kHz. The program ΔV_t is 2 V.

we showed [35] that, even in the FP emission-limited condition (i.e., FP emission time longer than oxide tunneling time), the nitride charge retention time can be approximated by

$$\tau(retention) = \frac{\tau_e(FP) + \tau_c(FP)}{\tau_c(FP)}\tau_{\text{ox}} \sim \exp\left(\frac{E_T - q(qF/\pi\varepsilon)^{1/2}}{kT}\right)\tau_{\text{ox}} \quad (4)$$

where $\tau_e(\text{FP})$ and $\tau_c(\text{FP})$ are the FP emission and capture times, respectively. τ_{ox} is an oxide tunneling time or, more specifically, positive oxide trapped charge (hole) assisted tunneling time. F is an electric field in nitride. Other variables have their usual definitions. The preceding equation can well explain many salient features of the observed program-state V_t retention loss, e.g., log dependence on retention time [26], [30], [39] and P/E cycle number [37], [39], negative dependence on gate stress voltage polarity [27], [30], [38], and positive dependence on retention temperature [26], [30], [31]. The comparison of the model predictions from (4) and experimental results is summarized in Table I. It should be mentioned that trap anneal effect during high-temperature bake is not considered in (4). Thus, a deviation between the model and measurement results in the temperature dependence is expected. Although the charge vertical loss model can explain the preceding measurement results well, other V_t retention loss mechanisms may coexist in different operation bias or device process conditions.

Finally, we would like to remark that the aforementioned RTS measurement is limited to a low P/E number because of cycling-induced new oxide trap creation. The program-state hole accumulation is not seen at the present program window,

TABLE I
DEPENDENCE OF PROGRAM-STATE V_t RETENTION LOSS ON RETENTION TIME, P/E CYCLES, GATE STRESS POLARITY, AND TEMPERATURE FROM THE VERTICAL CHARGE LOSS MODEL (IN AN FP EMISSION-LIMITED CONDITION) AND FROM EXPERIMENTAL RESULTS

program-state retention loss (ΔV_t)	retention time (t)	P/E cycle number (N)	gate stress (V_g)	bake temp. (T)
vertical charge loss model (FP emission limited, Eq.(4))	$\Delta V_t \sim \log(t)$	$\Delta V_t \sim \log(\tau_{ox}^{-1})$ $\sim \log(N_{ox})$ $\because N_{ox} \sim t_{stress}^{n} \sim N^{n}$ [36] $\therefore \Delta V_t \sim \log(N)$	negative V_g polarity dep.	$\Delta V_t \sim T$
experimental result	log dep. [26,30,39]	log dep. [37(Fig.9),39]	negative V_g polarity dep. [27,29,38]	positive temp. dep. [26,30,31]

1 V. The RTS measurement result in Fig. 14 does not exclude the possibility of hole accumulation and, thus, a dipole formation in other cycling and device process conditions [33].

IV. CONCLUSION

We have demonstrated a novel RTS method to characterize program and erase charge lateral spread in a SONOS Flash memory without the need to know a doping profile. In the RTS method, the τ_c/τ_e is very sensitive to program/erase/retention charges. It exhibits an exponential dependence on a local potential, compared with a linear dependence of the CP method. The RTS method can provide a better resolution than a CP method or an inverse I–V modeling approach. A mismatch between program electrons and erase holes has been shown by this method. Read current instability due to nitride charge vertical loss and random telegraph noise has been directly observed.

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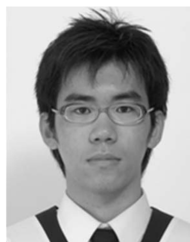

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