Integrated Batteryless Electron Timer

Hiroshi Watanabe, Tomomi Ushijima, Norio Hagiwara, Chiomi Okada, and Takeshi Tanabe

***Abstract*—From the viewpoint of information security, the semiconductor timing devices are reviewed, and a promising cell with floating gate (FG) is proposed as an integrated batteryless electron timer. The first issue is the difficulty in the timing precision, which is related to the trap-detrapping phenomena in the tunnel oxide between the FG and the silicon surface. The basic idea to resolve this issue is to monitor the trap-free cells among a plurality of prepared cells. The integrated batteryless electron timer is composed of a plurality of single-polysilicon-type solid-state aging devices that are connected in parallel. The first sample is fabricated in a standard complementary metal–oxide–semiconductor process, and the measurements clearly exhibit the first evidence that we succeeded to remove the trap-detrapping-related fluctuation in the ticking operation. The resultant secondary issues on the precision, i.e., the manufacturing fluctuation (subjecting to the central-limit theorem) and the temperature dependence, are also briefly discussed.**

***Index Terms*—Batteryless, communication network, encryption, local trap, solid-state aging device (SSAD), timing device.**

I. Introduction

FROM THE ancient Roman times, encryption has been used for exchanging secret diplomatic documents and charging military commands. Cipher breaking is accordingly a weapon to get around the enemy and has been therefore improved with the long history of encryption [1]. Here, we can list three indispensable factors for ensuring secured communication: 1) to deliver encryption keys as securely as possible; 2) to use as strong encryption algorithm as possible; and 3) to replace encryption keys at fixed intervals. The Diffie–Hellman protocol (composed of a pair of public and private keys) was invented in 1976 [2], and then, the Rivest–Shamir–Adelman algorithm [3] showed the method for fixing the first factor (factor 1). The users can deliver their public keys via the Internet and can thereby receive the letters ciphered by their public keys. As long as the algorithm is strong enough (factor 2), they can securely read the messages that they decipher using their private keys. As the Internet spreads all over the world, the encryption technology has grown to a global infrastructure for the communication network. On the other hand, according to Shannon [4], no technology can eternally secure the worldwide network as long as encryption keys are shorter than transinformation contents. It is however difficult to use the key having the same length with the transferred information in the commercial network. The cipher strength is therefore determined by the key length instead of the algorithm toughness. On the other hand, since the computational speed is annually upgraded and the cipher-breaking technique progresses, we should replace worn encryption keys at fixed intervals (factor 3). Recently, it is shown that the existing global-system-for-mobile-communications security is inadequate [5], which is in the news [6]. Here, we consider, to reinforce the security system, an integrated electron device ticking without a power supply. However, such batteryless electron timers have never been realized, although there are many patent publications in the literature [7]–[14].

The first batteryless timing device was proposed by Koehler and Grissom in 1969 [7] and individually by Shannon in 1976 [8]. Their idea is to control the data retention of nonvolatile memories with a charge-storage layer incorporating a radioactive isotope. As the β-particle escapes, the charge state of the charge-storage layer varies. The threshold voltage V_t accordingly varies progressively with time, and the elapsed time is estimated by reading the threshold-voltage shift (V_t shift). It appears that such an isotope timer precisely ticks [9], but the isotope is not preferable in semiconductor manufacturing. A few decades later, a silicon nitride layer was expected as the charge-storage layer of the batteryless timer by Lancaster and Hirose [10] and individually by Aozasa [11]. Here, the beta decay is replaced by the leakage current from the silicon nitride layer. Palm *et al.* proposed the idea of estimating the elapsed time from the time-dependent variation in the spatial distribution of charges in the silicon nitride layer [12]. It is unfortunately difficult to control the location of local traps in the level of the mass product. Berstis *et al.* [13] and Suzuki [14] considered the floating-gate (FG) polysilicon as the charge-storage layer of the batteryless timer. Electrons are stored in the polysilicon film surrounded by the oxide. The negatively charged polysilicon changes the electric field across the oxide. This breaks the detailed balance condition in which the current fluxes emitting from and injecting to the polysilicon are the same. The number of stored electrons is thereby decreased progressively with time without power supply (so-called batteryless), similar to the number of sand particles of the sandglass. However, the oxide film surrounding the polysilicon involves uncontrollable traps (some breakings of an atomistic bonding network) that expand the wavefunction of electrons into the oxide. Electrons are thus relayed deeper into the oxide [15], [16], which significantly increases the speed of change in the polysilicon charge state. This effect is sensitive to the trap level, the trap number, and the trap location, which are all dispersive.

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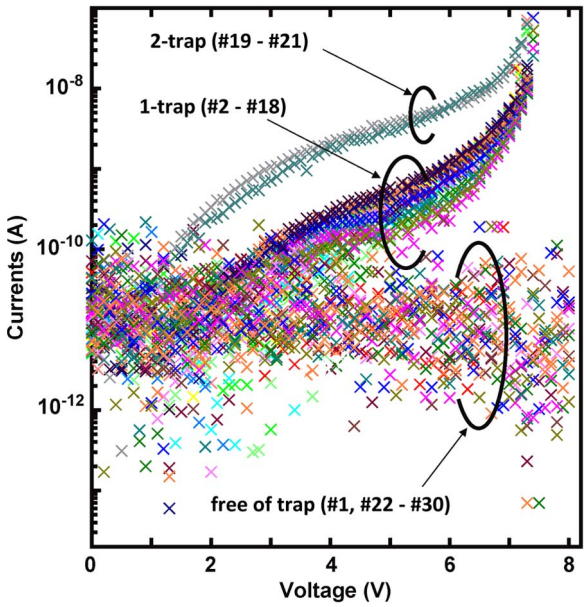

Fig. 1. Impact of the trap on the leakage current.

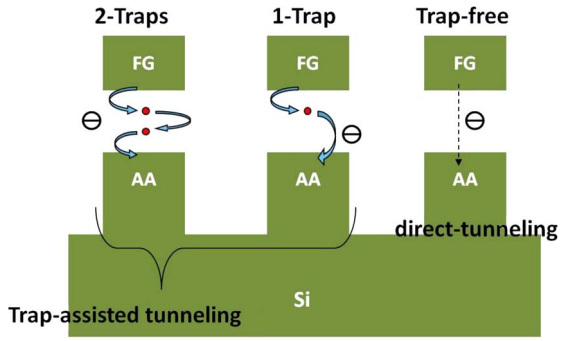

Fig. 2. Scheme of single- and double-trap processes in the leakage.

In Fig. 1, we plot the measured leakage currents through the oxide between the gate polysilicon and the silicon substrate. Here, note that the experiment consists of 30 sequential measurements on one and the same memory cell, in which the number depicts the (number)th IV measurement among 30 sequential measurements. We have three classifications, i.e., the noise, lower, and higher levels, corresponding to numbers 1 and 22–30; 2–18; and 19–21, respectively. In order to recognize the discrepancy between lower and higher levels, let us assume a trap-assisted tunneling, as illustrated in Fig. 2. If we have no trap, the leakage mechanism is regarded as direct tunneling (the trap-free process illustrated in the right of Fig. 2). Since the direct-tunneling current is very small, the leakage current is regarded as in the noise level. If we have a trap, the current is increased, and the mechanism is regarded as the one-trap process illustrated in the center of Fig. 2. If a second trap is involved (the two-trap process illustrated in the left of Fig. 2), the leakage current is further increased. If we assume that the lower level belongs to the one-trap process group, it can be regarded that the higher level belongs to the two-trap process group. Thereby, we find that the probability of the one-trap process is about 57% $(= 17/30)$ in this measurement. The probability of the two-trap process is 10% $(= 3/30)$ in this measurement. It sounds

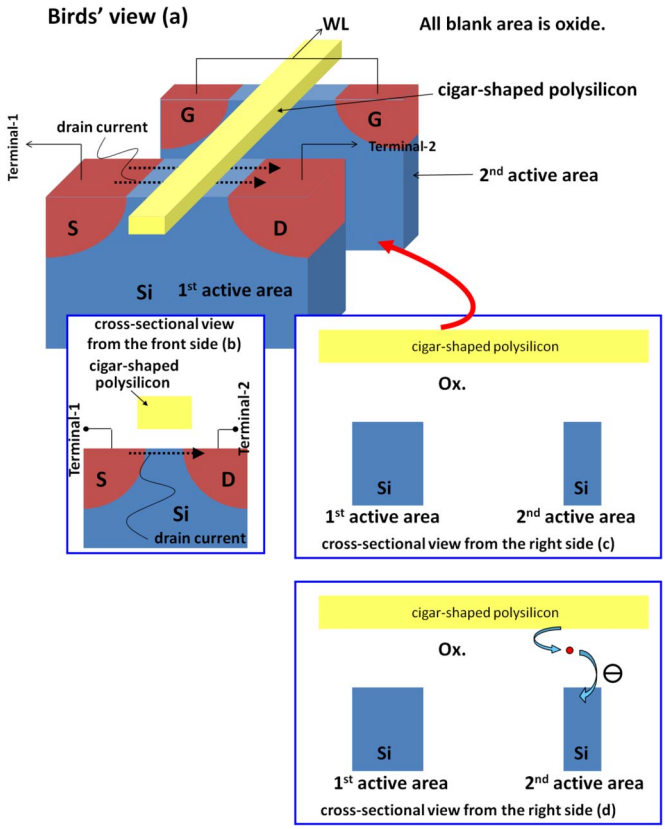

Fig. 3. Basic structure of the sample device.

that the first trap appeared at the second measurement (number 2) and survived during 17 sequential measurements, and the second trap appeared at the 19th measurement (number 19) and survived during three sequential measurements. Finally, they disappear after the 22nd measurement (number 22) and results in the noise level. Since such a change is not reproducible, some traps accidentally transit between the activated and inactivated states during the recursive measurements. From the discrepancy in the currents between the one- and two-trap processes, it is considered that the leakage current increases tenfold, which is consistent to the data-retention degradation (from ten years to several months) of the FG nonvolatile memory cell with a single trap [16], that is, a trap degrades the timing precision by 90%. Therefore, it appears that the speed of the V_t shift is hard to control.

In this paper, we will produce a method to suppress the error in timing owing to the trap. In Section II, we will briefly explain the basic idea. In Sections III and IV, we explain the experiments and the analysis, respectively. Sections V and VI are devoted to the discussion and the summary, respectively.

II. Method for Monitoring the Trap-Free Cell

The basic idea to suppress the error in timing is to monitor trap-free cells among a plurality of cells composing the circuit particularly designed for the solid-state aging device (SSAD) [17], [18]. In Fig. 3(a), the cell device structure of the SSAD is schemed on bird's view. The cross-sectional view from the front, as illustrated in Fig. 3(b), is equivalent to the

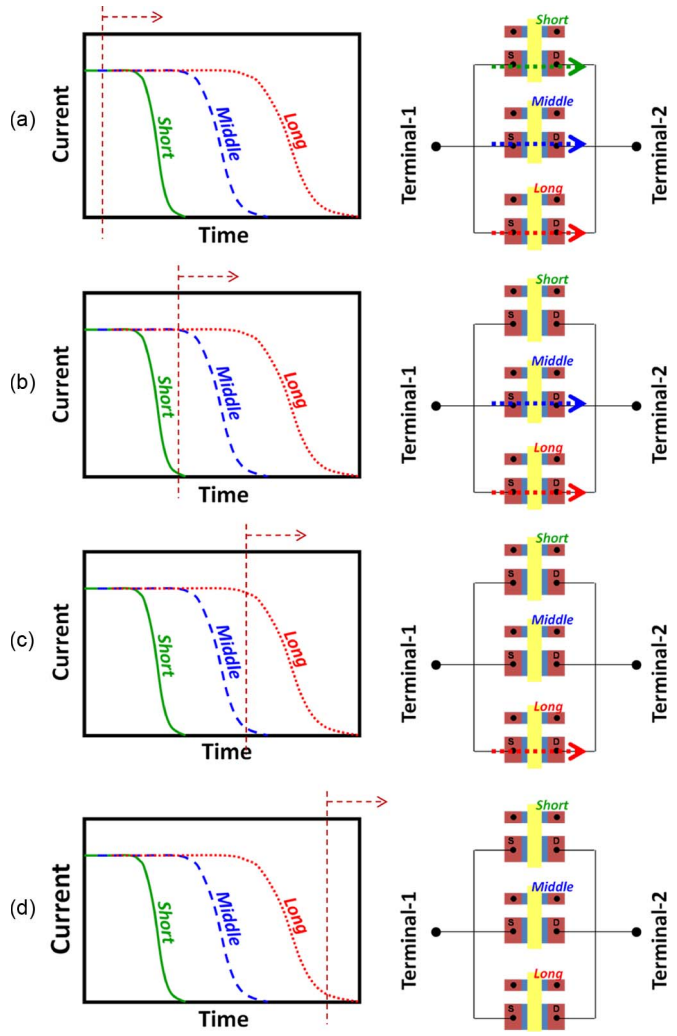

Fig. 4. Schematic of the basic idea for monitoring the trap-free cell.

cross-sectional view of a typical metal–oxide–semiconductor (MOS) field-effect transistor. In the cross-sectional views from the right, as illustrated in Fig. 3(c) and (d), there are the first and second trapeziums of silicon, i.e., the active areas. The oxide is sandwiched between the cigar-shaped polysilicon and the active areas. There is no trap in Fig. 3(c), whereas there is a trap in Fig. 3(d). Terminals 1 and 2 are connected to the source (S) and the drain (D) on the surface of the first active area, respectively. The drain current flows between these terminals, as shown in Fig. 3(a) and (b). On the surface of the second active area, we have the control gate (G) connected to the word line (WL). Here, note that the control gate is fabricated as the diffusion layer in the SSAD cell.

Let us assume that all diffusion layers are n-type and the virgin V_t is positive. In the preprocess, we erase the cell using a positive gate bias, and then decrease V_t. After that, as V_t is progressively increased with time owing to the injection of electrons to the polysilicon, the drain current will vanish at the lifetime of the cell. Let us consider three cells, lifetimes of which are short, middle, and long, respectively, as illustrated in Fig. 4. They are all connected in parallel between two terminals (terminals 1 and 2). The currents through these cells vanish in the sequence of lifetimes. At the initial state (a), the currents flow through all the cells. After the short lifetime (b), the current through the short-lifetime cell vanishes. After the middle lifetime (c), the currents through the middle-lifetime cell vanish. After the long lifetime (d), the connection between these terminals is terminated. This means that the longest-lifetime cell determines the lifetime of the parallel-connected cells between terminals. Since a trap degrades the lifetime, the resultant lifetime is determined by a trap-free cell, as long as the number of parallel-connected cells is large enough.

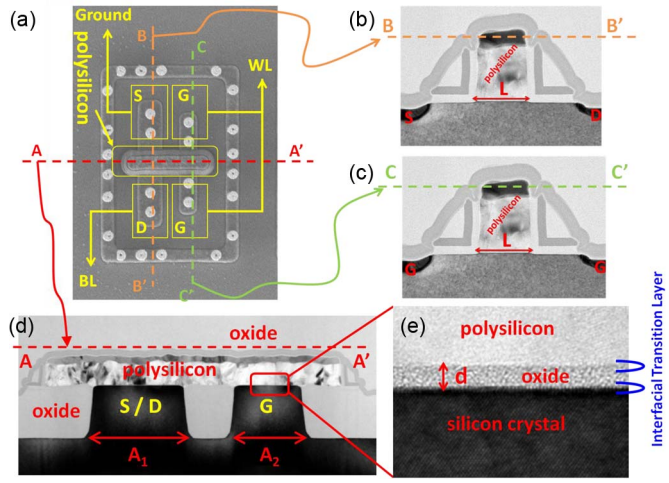

Fig. 5. SEM and TEM images of the measured sample.

III. Experiment

Fig. 5(a)–(e) shows the SSAD cell prepared using a 130-nm standard complementary MOS (CMOS) process for the measurements in this paper. The top view of the scanning electron microscope (SEM) is shown in Fig. 5(a), and the cross-sectional views of the transmission electron microscopes (TEM) along the lines of B−B′, C−C′, and A−A′ are shown in Fig. 5(b)–(d), respectively. In Fig. 5(a), the layout pattern having the contacts of the source (S), the drain (D), and the gates (G) is shown. A small and short sensing pulse is applied on the drain contact connected to a bitline (BL) for the READ operation with as less impact on the V_t shift as possible. The gate contacts are connected to the word line (WL). In Fig. 5(b), there are diffusion layers (n-type) connected to S and D. The width of cigar-shaped polysilicon is depicted by L. In Fig. 5(c), there are diffusion layers (n-type) connected to G in the same cross-sectional view with Fig. 5(b). In Fig. 5(d), there are the first and second active areas (labeled S/D and G, respectively), widths of which are A_1 and A_2, respectively. In Fig. 5(e), the thickness of the oxide, which is sandwiched between the polysilicon and the active areas in the vertical direction, is depicted by d. L and d are determined according to the requirement for the 130-nm CMOS process of the International Technology Roadmap for Semiconductors (ITRS) [19]. In this sample, the gate areas above the first and second active areas are $L \times A_1$ ($\cong 5.5 \times 10^{-10}$ cm^{-2}) and $L \times A_2$ ($\cong 4.1 \times 10^{-10}$ cm^{-2}), respectively.

To initialize the cell, the control-gate voltage V_{CG} is applied to the gate. The electrons tunnel from the polysilicon to the

second active area (G), where the gate capacitance is smaller and the electric field is higher. By this way, the polysilicon is charged positive at the initialized state, which results in a negative V_t.

If V_{CG} is kept zero during standby (after the initialization), electrons are injected to the polysilicon through the oxide to recover the charge neutrality of the polysilicon, which results in the increase in V_t progressively with time. When V_t reaches zero, the channel is closed. This is the lifetime of the SSAD cell. If the drain bias is applied before the lifetime, the drain current flows. If the drain bias is applied after the lifetime, the drain current does not flow. Even during standby (no gate bias), we can sense the V_t shift using a small and short drain bias. Since V_t varies with respect to the number of electrons that have tunneled ΔN, we obtain

$$\Delta N(t) = \frac{1}{q}\frac{\varepsilon_{\mathrm{OX}}}{d} L \frac{A_1 A_2}{A_1 + A_2} \Delta V_t(t) \tag{1}$$

where $\Delta V_t(t)$ is the V_t shift at a given time, t is the elapsed time after the initialization, $\varepsilon_{\mathrm{OX}}$ is the permittivity of the oxide, and q is the elementary charge. Here, in the derivation of (1), we have used the fact that the structure is, in principle, a series connection of two capacitors like in an ordinary FG memory. Let us note that L, d, A_1, and A_2 are the design parameters in manufacturing, while ΔV_t is observable in the electrical measurement, q is a fundamental physical constant, and $\varepsilon_{\mathrm{OX}}$ is a material constant. Since the fabrication process of the thin oxide on crystal silicon has been improved in the recent decades, the fabrication error in d mainly comes from the interfacial transition layer where the permittivity gradually changes [20], [21]. This means that the fabrication error in $\varepsilon_{\mathrm{OX}}$ is equivalent to the error in d, which removes the second factor $\varepsilon_{\mathrm{OX}}/d$ from the error estimation. $\varepsilon_{\mathrm{Litho}}$, which is the error in L, A_1, and A_2, comes from the lithography and the etching process and is then regarded small (i.e., controllable) according to the ITRS [19]. $\varepsilon_{\mathrm{Sens}}$, which is the error in ΔV_t, is from the sensing of the drain current at a given time. Taking into account (1) and $\varepsilon_{\mathrm{trap}}$, which is the influence of the traps on ΔV_t, the error in the number of electrons that have tunneled through the oxide is given by

$$\varepsilon_N(t) = \varepsilon_{\mathrm{Litho}} + \varepsilon_{\mathrm{Sens}}(t) + \varepsilon_{\mathrm{trap}}(t). \tag{2}$$

In Fig. 6, the cells shown in Fig. 5 are connected in parallel. The sources of these cells are connected to terminal 1 via a common source line. The drains of these cells are connected to terminal 2 via a common bitline. The control gates of these cells are connected to the gate (G) via a common word line. We measured these blocks, each composed of 20 parallel-connected cells, as shown in Fig. 6. We separately initialize them after ten cycles of program–erase. After that, we connect some blocks using the probe and then measure 20, 40, 60, ... cells connected in parallel (one, two, three blocks, etc., respectively).

IV. Analysis

In Fig. 7, we plot the data of the V_t shift measured at room temperature for the system composed of 20, 40, ..., and 320 parallel-connected cells with respect to time. As the number of parallel-connected cells is increased, the plotted data merge to a straight line (the guide for the eyes). It can be attributed to the components of the longest-lifetime cell, where the leakage is due to the direct tunneling. In Fig. 8, it is shown that the V_t shifts at 1/2 and 1 month lead to constants, while the number of cells is nearly 300. Thereby, we find

$$\lim_{N\to\infty} \varepsilon_N(t) = \varepsilon_{\mathrm{Litho}} + \varepsilon_{\mathrm{Sens}}(t). \tag{3}$$

In Fig. 9, we plot the number of electrons that have tunneled through the oxide per cell, which is obtained by substituting ΔV_t measured at room temperature into (1). There is a clear relationship between the V_t shift and time, which means that

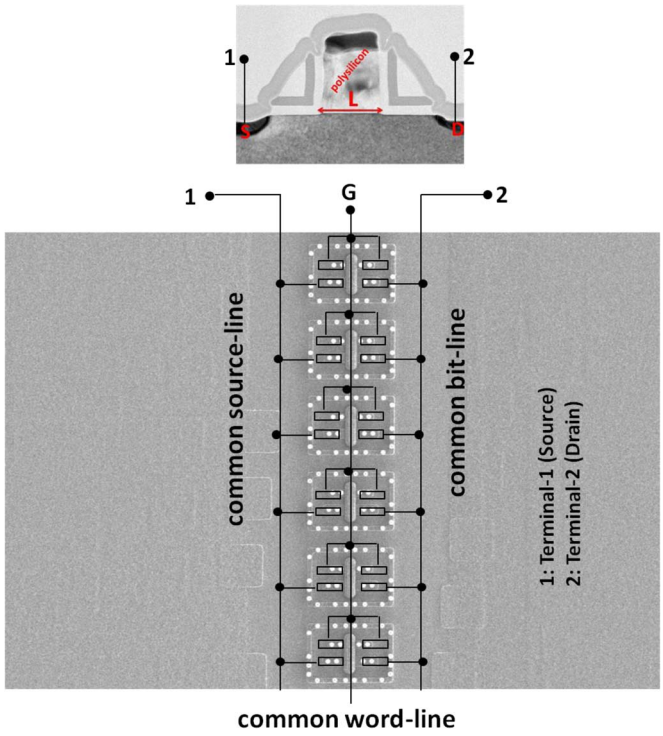

Fig. 6. SEM image of the parallel-connected cells.

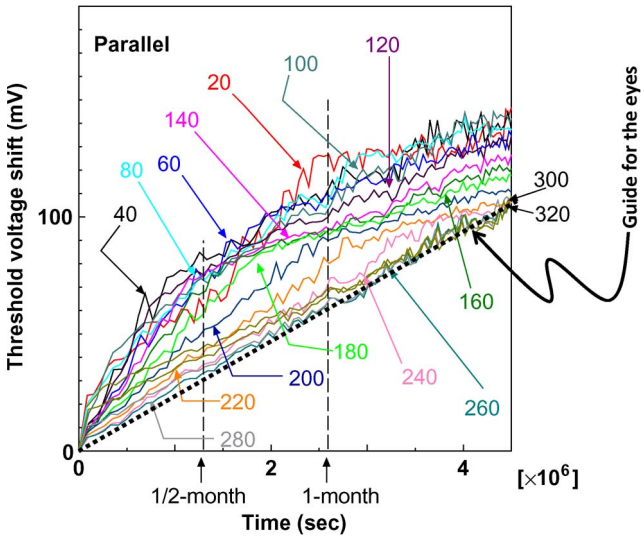

Fig. 7. Effect of the cell number on the speed of the V_t shift.

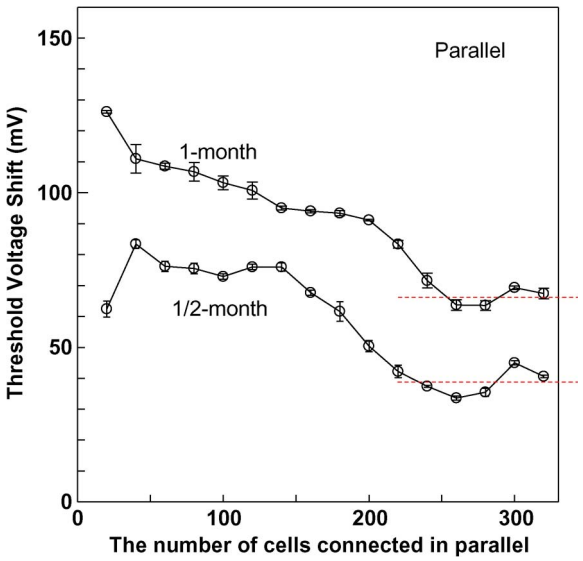

Fig. 8. Effect of the cell number on the speed of the V_t shift.

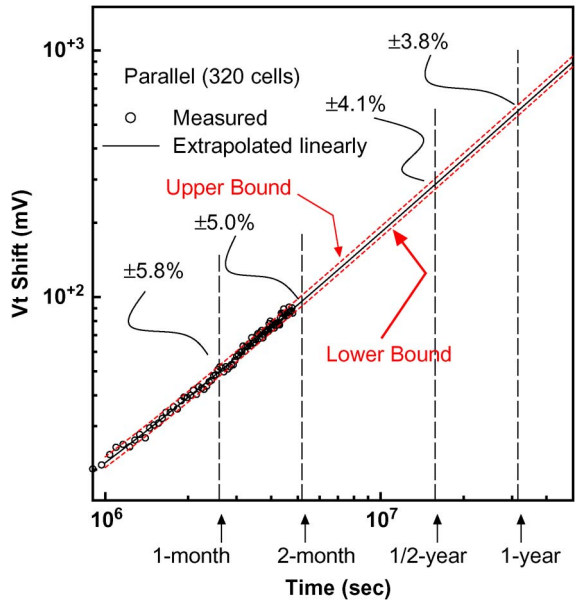

Fig. 9. Experimental evidence for monitoring the trap-free cell.

we have succeeded in removing the influence of the trap. The bulk line is the result of the linear fitting of 94 data of 320 parallel-connected cells (16 blocks connected in parallel) with the variance being 4.5. The red dashed lines of the upper and lower bounds are defined by 14 data points having the negative and positive largest discrepancies from the bulk line with the variances being 1.81 and 0.76, respectively. If the relative error is defined as the difference between the lines fitted with the upper and lower bounds, it is progressively decreased with time from $\pm 5.8\%$ (one month), $\pm 5.0\%$ (two months), $\pm 4.1\%$ (1/2 year), and $\pm 3.8\%$ (one year) at room temperature. This means that the larger V_t shift is preferable for suppressing $\varepsilon_{\mathrm{Sens}}$.

V. Discussion

It is noteworthy that the longer-lifetime cells have a lower discharging speed and that the discharged cells cannot contribute to the signal of the parallel-connected cells. We may thus regard the slowest cell (with the lowest discharge speed) as the cell monitored in the proposed method. Let us consider that there are at least two trap-free cells (first and second slowest cells) in the parallel-connected cells. If a trap is activated in the first slowest cell during the measurements, the second slowest cell will replace the first slowest. Next, if the trap in the first slowest cell is inactivated again, the second slowest cell will be replaced by the first slowest cell. The exchange of the trap-free cells thus causes the fluctuation on the V_t time slope shown in Fig. 9. The lifetime discrepancy between the trap-free cells comes from the fluctuation in the manufacturing controllability of cell devices. Since the oxide-thickness fluctuation exponentially affects the direct tunneling, it might appear that the slope fluctuation must be much larger than that shown in Fig. 9. However, as discussed in Section III, the fluctuations of the oxide thickness and the interface permittivity cancel out each other within the first-order approximation. Therefore, the fluctuation on the slope would be composed of higher-order terms in the tunneling and $LA_1A_2/(A_1 + A_2)$ in (1). Provided that the number of parallel-connected cells is large enough, the fluctuation in manufacturing can be suppressed according to the central-limit theorem in the manufacturing control. In other words, we have successfully removed the trap-induced leakage fluctuation (shown in Fig. 1) that is not subject to the central-limit theorem.

Next, let us discuss the possibility that the fluctuation on the V_t time slope is dependent of temperature. First, note that the tunneling probability itself is independent of temperature in the direct tunneling. However, if the number of tunneling electrons is dependent of temperature, the direct-tunneling "current"(tunneling probability $\times$ electron number) is temperature dependent. According to Fermi–Dirac statistics, at higher temperatures, the Fermi level is higher, and the unclearness around the Fermi level is enhanced. This encourages more electrons to tunnel at higher temperatures. The temperature dependence on the lifetime also comes from the sensing of the signal at terminal 2, i.e., $\varepsilon_{\mathrm{Sens}}$ of (3). To suppress the issue related to temperature dependence, we need to demonstrate another invention that we will report elsewhere.

In addition, it is preferable to use a larger mean value of V_t in sensing the lifetime because the V_t fluctuation becomes comparatively small. In other words, we need to increase the average slope of the V_t time, which is determined by the electric field across the oxide. To control the electric field, we may adjust the doping profile and not the oxide thickness because the target oxide thickness is not adjustable in the commercial manufacturing line. We must also take care of the READ-disturb issue, which may be involved by the drain voltage during the sensing of V_t. In the measurements, we applied a 0.1-V drain bias to suppress the READ disturb as possible as we can. A more detailed investigation is, of course, needed in future work.

VI. Summary

We have proposed the SSAD as a new cell structure for the batteryless timer and a method for removing the influence of traps on the ticking precision (monitoring a trap-free cell).

We have fabricated the first trial sample of the SSAD using a 0.13-μm standard CMOS process. We have carefully investigated this sample and have obtained a clear relation between the number of parallel-connected cells and the speed of the V_t shift. The obtained data have been studied using the error analysis, and then, we have regarded the leakage current from the polysilicon as subject to the direct tunneling that is independent of traps. We have estimated the number of electrons that have tunneled during standby at room temperature. This result can be regarded as hopeful to the future development of the integrated batteryless electron timer. The data shown in Fig. 1 have been obtained by measuring the samples shown in Fig. 5.

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Dr. Watanabe is a member of the Japan Society of Applied Physics. He is also a member of Memory Subcommittee of IEEE International Reliability Physics Symposium (IRPS 2011).

Tomomi Ushijima, photograph and biography not available at the time of publication.

Norio Hagiwara, photograph and biography not available at the time of publication.

Chiomi Okada, photograph and biography not available at the time of publication.

Takeshi Tanabe, photograph and biography not available at the time of publication.