FinFET SRAM Cell Optimization Considering Temporal Variability Due to NBTI/PBTI, Surface Orientation and Various Gate Dielectrics

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***Abstract*—This paper analyzes the impacts of intrinsic process variations and negative bias temperature instability (NBTI)/positive BTI (PBTI)-induced time-dependent variations on the stability/variability of 6T FinFET static random access memory (SRAM) cells with various surface orientations and gate dielectrics. Due to quantum confinement, (110)-oriented pull–down n-channel FETs with fin line-edge roughness (LER) show larger Vread,0 and Vtrip variations, thus degrading READ static noise margin (RSNM) and its variability. Pull-up p-channel FETs with fin LER that are (100)-oriented show larger Vwrite,0 and Vtrip variations, hence degrade the variability of WRITE SNM. The combined effects of intrinsic process variations and NBTI/PBTI-induced statistical variations have been examined to optimize the FinFET SRAM cells. Worst-case stress scenario for SNM stability/variability is analyzed. With the presence of both NBTI and PBTI in high-k metal-gate FinFET SRAM, the RSNM suffers significant degradation as Vread,0 increases, whereas Vtrip simultaneously decreases. Variability comparisons for FinFET SRAM cells with different gate stacks (SiO_2 and SiO_2/HfO_2) are also examined. Our paper indicates that the consideration of NBTI/PBTI-induced temporal variation changes the optimal choice of FinFET SRAM cell surface orientations in terms of the μ/σ ratio in RSNM.**

***Index Terms*—FinFET, negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), static random access memory (SRAM), surface orientation, variability.**

I. INTRODUCTION

MULTIGATE FinFETs are promising device candidates for post-22-nm complementary metal–oxide–semiconductor (MOS) technology generations due to their superior short channel effects, better subthreshold slope, and reduced random dopant fluctuation. The sidewall surface (conducting channel) orientation of FinFET devices can be easily changed by rotating the layout of the devices to improve the carrier mobility, and thus circuit performance [1]–[3]. The fluctuation of the fin width due to line-edge roughness (fin LER) is widely recognized as a major source of variability for FinFET devices [4]. As the fin width scales down, the quantum–mechanical effect becomes more significant. However, the different surface orientation, with different quantization effective mass and quantum confinement, may result in distinctly different variability [22], [25].

In addition to time-zero intrinsic process variability, negative bias temperature instabilities [NBTI; for p-channel FET (PFET)] and positive BTI [PBTI; for n-channel FET (NFET)] have become major long-term reliability concerns as they weaken MOSFETs over time, thus resulting in temporal degradation in the stability and variability of the static random access memory (SRAM) cells [5]–[9]. The (110)-oriented Si surface has more dangling bonds before passivation and is therefore expected to have more bonded hydrogen at the interface in comparison with (100)-oriented Si surface. As such, the NBTI/PBTI degradation is more significant in (110)-oriented device than in (100)-oriented one [10], [11]. FinFET devices with different surface orientations exhibit distinct threshold voltage variations resulting from the intrinsic process variations and NBTI/PBTI-induced temporal variations. Fig. 1(a)–(c) illustrate the layouts of 6T FinFET SRAM cells with various combination of (110) and (100) surface (conducting channel) orientations by rotating the FinFET devices. The layouts are based on scaled ground rules from 32-nm node according to the International Technology Roadmap for Semiconductors projection.

In this paper, for the first time, the combined effects of time-zero intrinsic process variability and long-term temporal variability (due to NBTI/PBTI) are considered for optimizing the FinFET device orientation combinations to improve the stability/variability of 6T FinFET SRAM cells with oxide and high-k gate dielectrics, respectively. For NBTI/PBTI, the temporal degradation in SRAM stability/variability under worst case stress pattern/condition is considered. This paper is organized as follows. Section II describes the device design and simulation methodology used in this paper. Section III investigates the stability and variability of the 6T FinFET SRAM cells with various surface orientation combinations and gate dielectrics. In the first part of Section III, the fin LER is considered to optimize the 6T FinFET SRAM cells in terms of μRSNM$/\sigma$RSNM, where μRSNM is the mean of READ static noise margin (RSNM), and σRSNM is the standard deviation of the RSNM. In the second part, the combined effects of fin

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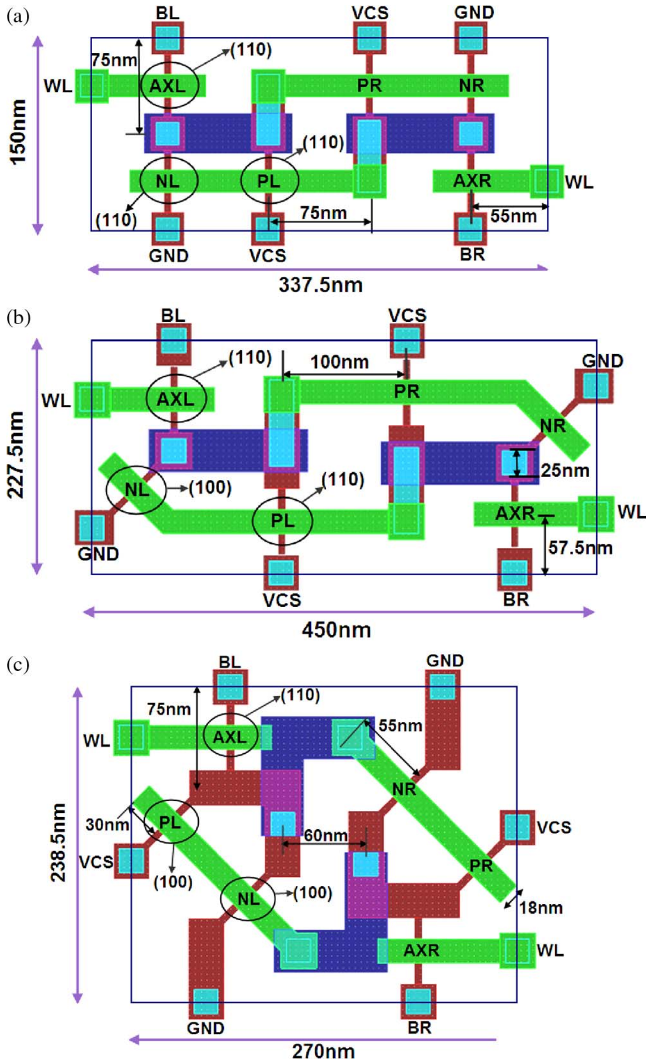


Fig. 1. (a) PU (PL/PR), PD (NL/NR), and PG transistors (AXL/AXR), all with (110) orientation. (b) (110) PU, (100) PD, and (110) PG transistors. (c) (100) PU, (100) PD, and (110) PG transistors.

LER and the NBTI/PBTI-induced temporal variability are then considered to optimize the 6T FinFET SRAM cells with oxide and high-k dielectrics, respectively. Section IV concludes this paper.

II. Device Design and Simulation Methodology

In this paper, the 6T FinFET SRAM cells designed with 18-nm L_g FinFET devices [$W_{\text{fin}} = 5$ nm, $H_{\text{fin}} = 15$ nm, channel doping = 1e17 cm^{-3}, $V_{\text{dd}} = 1$ V, gate stacks: $\text{SiO}_2(0.6\ \text{nm})/\text{HfO}_2(2.5\ \text{nm})$ or $\text{SiO}_2(1\ \text{nm})$] are analyzed using 3-D atomistic technology computer-aided design mixed-mode simulations [12]. The quantum-confinement effect is calibrated with the exact solution of Schrödinger's equation [13] to accurately account for the threshold voltage sensitivity to process variations for (100)/(110) N/PFETs. Reaction–diffusion model [14] is used to calibrate the threshold voltage drift due to NBTI/PBTI [10], [15]. To assess the dominant process variation source, i.e., fin LER [4], [16], the rough line edge patterns are generated using Fourier synthesis approach [17] with correlation length = 20 nm and

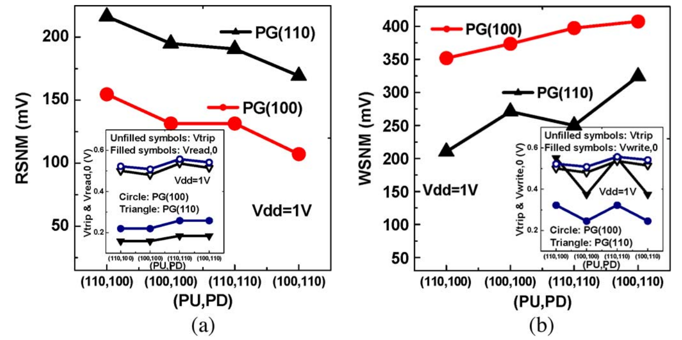


Fig. 2. (a) RSNM comparisons for eight types of 6T FinFET SRAM cells. (b) WSNM comparisons for eight types of 6T FinFET SRAM cells.

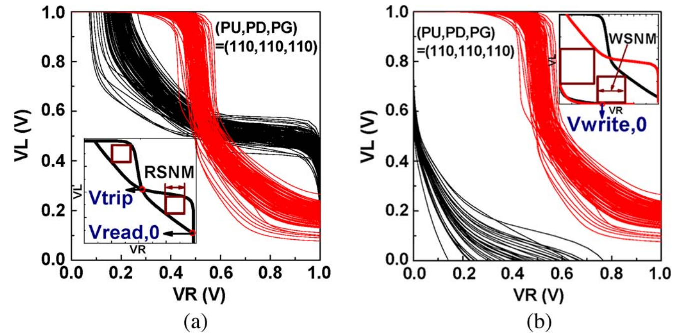


Fig. 3. (a) RSNM variation and (b) WSNM variation due to fin LER. (Correlation length = 20 nm and rms amplitude = 1.5 nm [4]).

root mean square amplitude = 1.5 nm [4]. Atomic-level 3-D mixed-mode Monte Carlo simulations with 200 samples are then performed for each case.

III. 6T FinFET SRAM Cells With (100)/(110) Surface Orientations

Pull-up (PU), pull-down (PD) and pass-gate (PG) transistors with (110) and (100) orientations can be combined for eight types of 6T FinFET SRAM cells. Fig. 2(a) shows the RSNM and Vread,0/Vtrip (defined in Fig. 3(a) inset) comparisons among the eight types of cells. The RSNM is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. Vread,0 is the READ disturb voltage determined by the voltage divider effect between the PG and PD transistors. Vtrip is the voltage needed to flip the cell inverter. Increase in Vread,0 or decrease in Vtrip will degrade the RSNM. FinFET SRAM cells with (110) PG devices show lower Vread,0 and higher RSNM than that with (100) PG devices. Due to stronger (100) PD device, (PU, PD, PG) = (110, 100, 110) and (100, 100, 110) show lower Vread,0 and higher RSNM than the standard SRAM cell with all (110) devices. Fig. 2(b) shows the WRITE static noise margin (WSNM) and Vwrite,0/Vtrip (defined in Fig. 3(b) inset) comparisons. The WSNM is determined by the smaller of the two squares that can fit between the cell-static voltage transfer characteristics during a WRITE operation (see Fig. 3(b) inset). Vwrite,0 is determined by the voltage divider effect between the PU PFET and PG transistors. Lower Vwrite,0 will benefit the WSNM. As can be seen, (100) PG device with stronger strength (higher mobility) shows lower Vwrite,0 and larger WSNM.

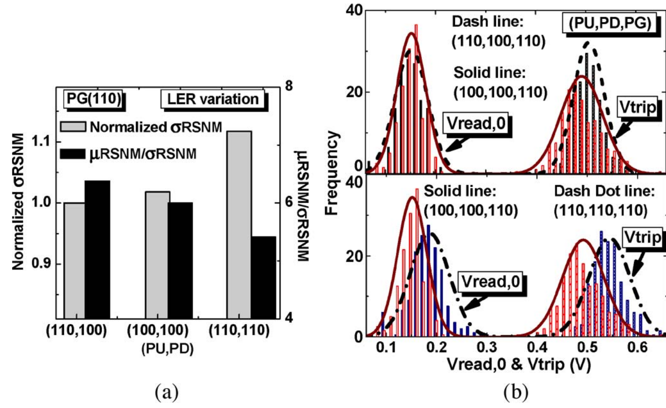


Fig. 4. (a) Normalized σRSNM and μRSNM$/\sigma$RSNM comparison considering fin LER. (110,100,110) SRAM cell shows largest μRSNM$/\sigma$RSNM. (b) Vread,0 and Vtrip variation comparisons considering fin LER.

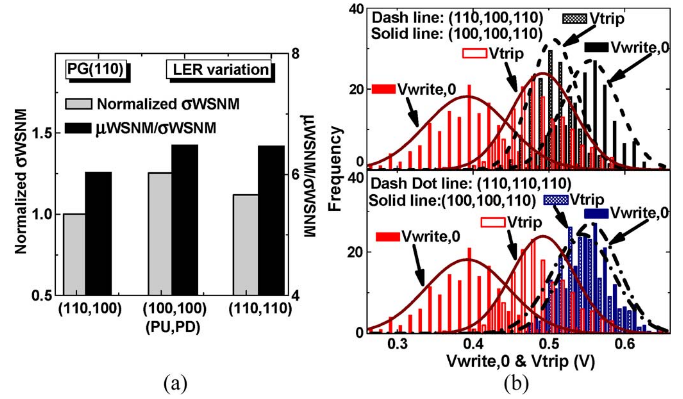


Fig. 5. (a) (100,100,110) SRAM cell shows largest μWSNM$/\sigma$WSNM. (b) Vwritet,0 and Vtrip variation comparisons considering fin LER.

A. Time-Zero Stability/Variability Due to Process Variation

In this section, the impacts of local random variations on device variability and optimization of the 6T FinFET SRAM cells are analyzed. Due to the difference in quantization effective mass [18]–[20], the effect of quantum confinement varies for different orientations. FinFETs with smaller quantization effective mass and stronger quantum confinement are more susceptible to fin LER than that with larger quantization effective mass. Fig. 3 illustrates the degradation READ/WRITE stability of 6T FinFET SRAM cell due to fin LER. Fig. 4(a) shows the normalized σRSNM and μRSNM$/\sigma$RSNM comparisons among the three types of FinFET SRAM cells with higher RSNM. The SRAM cell with (PU,PD,PG) = (100,100,110) shows larger σRSNM than the (110,100,110) case. Because (100) PU device with stronger quantum confinement exhibits larger threshold voltage variation due to fin LER than the (110) PU device, the (100,100,110) SRAM cell shows larger Vtrip variation [see Fig. 4(b)] and σRSNM than the (110,100,110) cell. The voltage margin between Vread,0 and Vtrip is larger in the (110,100,110) cell than the (100,100,110) one, which indicates that the μRSNM is larger in the (110,100,110) SRAM cell. Therefore, the (110,100,110) SRAM cell shows larger μRSNM$/\sigma$RSNM than the (100,100,110) one. The (PU,PD,PG) = (110,110,110) SRAM cell shows higher σRSNM than the (100,100,110) cell. The (110) NFET with stronger quantum confinement shows larger threshold voltage variation, due to fin LER, than the (100) NFET. Therefore, the (110,110,110) SRAM cell with (110) PD device shows larger Vread,0 variation than the (100,100,110) cell with (100) PD device [see bottom of Fig. 4(b)]. Vtrip is determined by the strength ratio between PU PFET and PD NFET devices. The (110,110,110) cell with (110) PD NFET and the (100,100,110) cell with (100) PU PFET show comparable Vtrip variation due to stronger quantum confinement in (110) PD NFET and (100) PU PFET, respectively, [see bottom of Fig. 4(b)]. Therefore, the (110,110,110) cell with larger Vread,0 variation and comparable Vtrip variation shows larger σRSNM than the (100,100,110) cell.

Fig. 5(a) compares the normalized σWSNM and μWSNM$/\sigma$WSNM. Vwrite,0 is determined by the voltage divider effect between PU PFET and PG NFET devices. The (100,100,110) cell with (100) PU PFET shows larger Vwrite,0 variation and σWSNM than the (110,100,110) and (110,110,110) cells with (110) PU devices [see Fig. 5(b)]. Due to its larger voltage margin between Vtrip and Vwrite,0, the (100,100,110) cell shows larger μWSNM than the (110,100,110) and (110,110,110) cells. Even though the (100,100,110) cell has larger σWSNM than the (110,100,110) and (110,110,110) cells, it still shows larger μWSNM$/\sigma$WSNM due to its larger μWSNM.

B. Long-Term Stability/Variability Due to NBTI/PBTI

Another factor of variability is the degradation of transistor parameters over time that also lowers the operating margin of SRAM cells. The NBTI (for PFET) and PBTI (for NFET) increase the transistor threshold voltages and reduce the drive currents with time. The NBTI/PBTI-induced random discrete charge trapping results in additional statistical variation. Fig. 6(a) and (b) show the time-dependent threshold voltage increase ($|\Delta V_{\rm th}|$) due to NBTI and PBTI for SiO_2/HfO_2/TiN and SiO_2 FETs, respectively, and the insets demonstrate the good calibration results with published data [7], [8]. For SiO_2/HfO_2/TiN FETs, PBTI- and NBTI-induced $V_{\rm th}$ shifts are comparable. For SiO_2 FETs, NBTI-induced $|\Delta V_{\rm th}|$ is larger than PBTI by approximately one order of magnitude for the poly-gate FinFETs studied. The generated interface traps account for the increase in device threshold voltage as follows:

$$|\Delta V_{\rm th}(t)| = qN_{\rm it}(t)/C_g$$

where $N_{\rm it}$ is the density of interfacial traps and C_g is the gate capacitance. Based on this equation, the trap density for each case can be obtained (as shown in Table I). With the average number of traps determined for specific surface orientation, the actual number of traps in each device is randomly generated based on Poisson distribution [21]. Then, each trap is assigned to a random location in the channel/gate dielectric interface [23].

In this paper, the degradation in SRAM stability with time under worst case stress pattern/condition (extreme asymmetry condition, only PR with NBTI and NL with PBTI) is considered, as shown in Fig. 7(a). Fig. 7(b) shows that FinFET SRAM cells with SiO_2 gate dielectric suffer from NBTI and show 9.5%

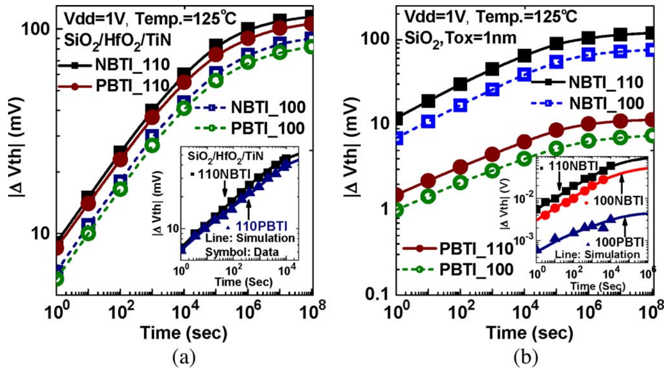


Fig. 6. (a) NBTI/PBTI-induced V_{th} shift for $SiO_2/HfO_2/TiN$ FET. (Inset) The model-data calibration. (b) BTI-induced V_{th} shift for the SiO_2 gate dielectric FET.

TABLE I
TRAP DENSITY FOR HIGH-k AND OXIDE GATE DIELECTRICS WITH (100) AND (110) SURFACE ORIENTATIONS. THE STRESS TIME IS 1×10^8 s, TEMPERATURE = 125 °C, AND Vdd = 1 V

Nit (cm^{-2})	Surface Orientation	HfO_2	SiO_2
NBTI	(110)	2.48×10^{12}	2.58×10^{12}
	(100)	1.94×10^{12}	1.52×10^{12}
PBTI	(110)	2.32×10^{12}	2.48×10^{11}
	(100)	1.65×10^{12}	1.62×10^{11}

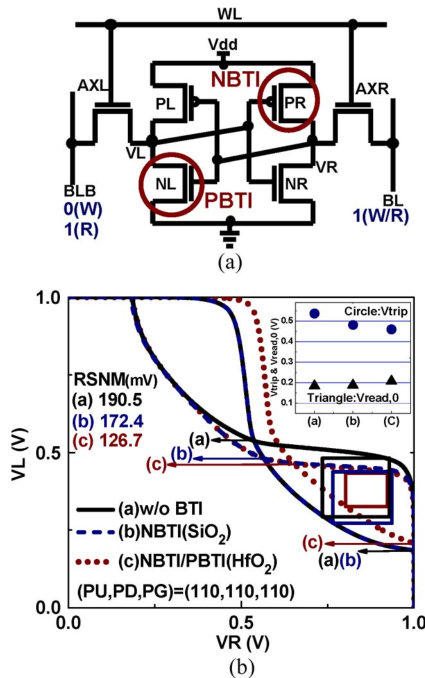


Fig. 7. (a) Worst case stress scenario for READ (R) and WRITE (W) stability. (b) RSNM comparison among curves (a) without BTI, (b) considering NBTI only, and (c) considering NBTI/PBTI. The stress time is 1×10^8 s at 125 °C.

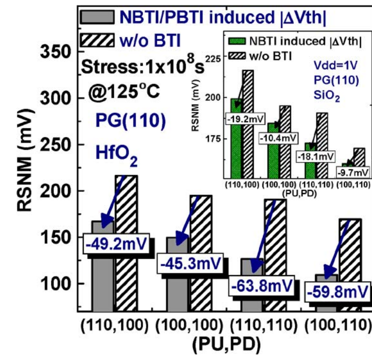


Fig. 8. RSNM degradation due to NBTI/PBTI. (Inset) The RSNM degradation due to NBTI only.

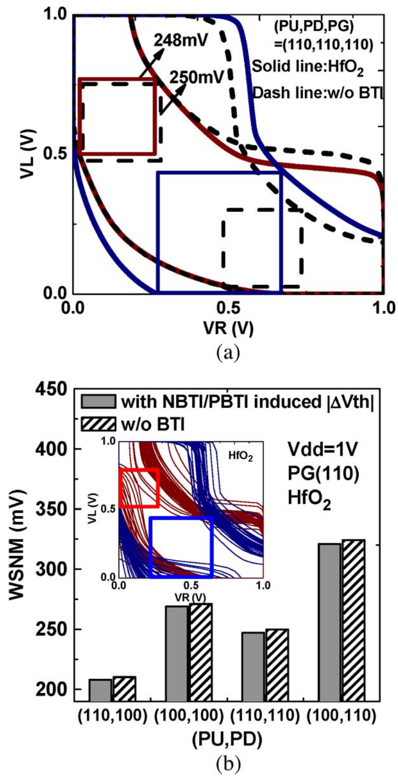


Fig. 9. (a) WSNM comparison between SRAM cells without BTI and considering NBTI/PBTI. The WRITE curves of solid and dashed lines overlap with each other. (b) Slight degradation in WSNM due to NBTI/PBTI under worst case stress condition. NBTI/PBTI stress time is 1×10^8 s at 125 °C.

degradation (stress time is 1×10^8 s at 125 °C) in RSNM due to its decreased Vtrip. FinFET SRAM cells with high-k gate dielectric under the same stress time and temperature suffer from NBTI/PBTI and show 33.5% degradation in RSNM due to its increased Vread,0 and decreased Vtrip (see Fig. 7(b) inset). As shown, the sensitivity of PBTI on RSNM is larger than NBTI. Fig. 8 shows the impact of NBTI/PBTI-induced $|\Delta V_{\mathrm{th}}|$ on the RSNM. The FinFET SRAM cells with (110)-oriented PU(PD) devices suffer larger NBTI(PBTI) degradation due to higher number of interface traps, resulting in larger degradation in RSNM. In contrast with the significant RSNM degradation due to NBTI/PBTI, Fig. 9(a) and (b) show that the WSNM only slightly degrades. In Fig. 7(a), NBTI weakens PR and makes VR easier to write than VL; therefore, WSNM is mainly determined by writing VL. The long-term WSNM variability slightly degrades, as compared with the time-zero WSNM variability. Fig. 10 shows the long-term RSNM variability considering LER and NBTI/PBTI-induced V_{th} variation for high-k and oxide gate dielectric FETs. PBTI dominates the RSNM variation for high-k metal gate SRAM cells; thus, SRAM cells with (110) PD devices show larger σRSNM, Vread,0 variation [see bottom of Fig. 11(a)] and Vtrip variation [see bottom of Fig. 11(b)]. However, for SiO_2 FETs, NBTI dominates its RSNM

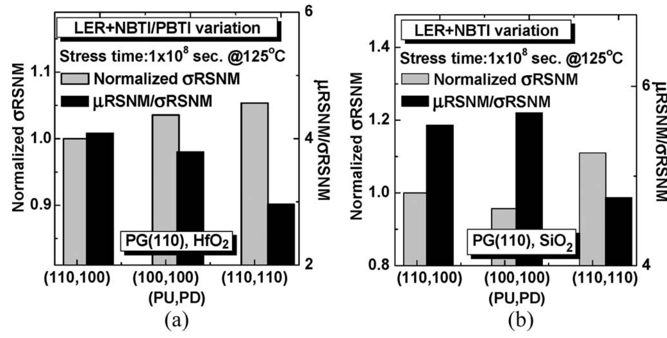


Fig. 10. (a) Normalized σRSNM and μRSNM/σRSNM comparison considering fin LER and NBTI/PBTI-induced variation. The (110,100,110) SRAM cell (HfO_2) shows the largest μRSNM/σRSNM. (b) The (100,100,110) SRAM cell (SiO_2) shows the largest μRSNM/σRSNM.

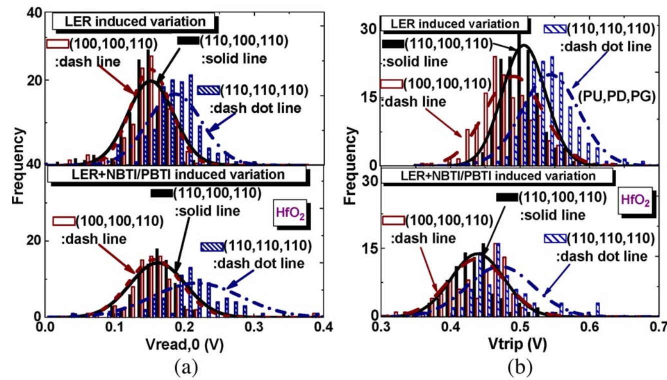


Fig. 11. (a) (110) PD devices show larger time-dependent Vread,0 variability degradation and Vread,0 increase. (b) (110) PD devices show larger time-dependent Vread,0 variability degradation and Vread,0 increase. BTI stress time is 1×10^8 s at 125 °C.

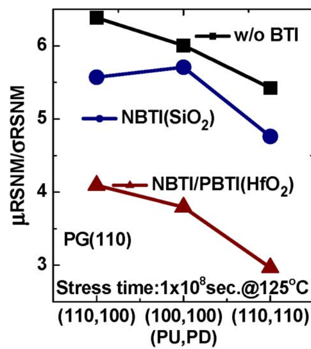
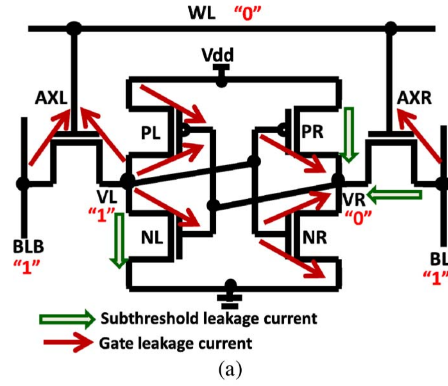


Fig. 12. μRSNM/σRSNM comparison considering short-term (fin LER) and long-term (fin LER + NBTI/PBTI) variations.

variation; thus, SRAM cells with (110) PU devices show larger decrease in μRSNM (see Fig. 8 inset) and larger σRSNM [see Fig. 10(b)]. Therefore, SRAM cells (SiO_2 dielectric) with (110) PU devices show larger decrease in μRSNM/σRSNM than SRAM cells with (100) PU devices. Fig. 12 demonstrates that NBTI/PBTI-induced temporal variability in SRAM will change the optimal choice of FinFET SRAM cells with different gate stacks in terms of μRSNM/σRSNM.

The fin LER-induced time-zero variability of FinFET SRAM cell is related to the fin width. FinFET SRAM cells with smaller fin width and larger quantum confinement will show larger difference in the time-zero variability among cells with different surface orientation combinations. On the other hand, FinFET SRAM cells with different surface orientations may show comparable time-zero variability if wider fin devices with less quantum confinement are used. However, the NBTI/PBTI-induced temporal variability still impacts the optimal choice of FinFET SRAM cells with different surface orientation combinations.



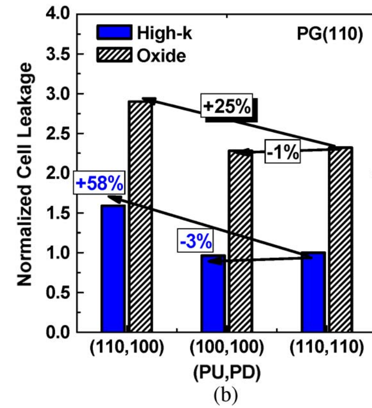


Fig. 13. (a) Cell leakage components of a 6T SRAM cell. (b) Normalized cell leakage comparisons of FinFET SRAM cells with high-k and oxide gate dielectrics. The cell leakages of high-k FinFET SRAM cells show larger orientation dependence than that of oxide FinFET SRAM cells.

Fig. 13(a) shows the leakage components of the 6T SRAM cell. The standby leakage current of the 6T SRAM cell can be estimated by the sum of all the subthreshold and gate leakage currents. Fig. 13(b) shows the normalized cell leakage comparisons of FinFET SRAM cells with oxide and high-k gate dielectrics. The subthreshold leakage current exponentially increases with decreasing threshold voltage. Therefore, the (110) NFET [(100) PFET] with stronger quantum confinement and larger threshold voltage shows lower subthreshold leakage current than the (100) NFET [(110) PFET]. Yang *et al.* [24] showed that the gate leakage currents are comparable between the (110) and (100) devices. In other words, the difference in cell leakages among these FinFET SRAM cells [see Fig. 13(b)] is mainly due to the difference in the subthreshold leakage currents. FinFET SRAM cells with high-k gate dielectric show two orders of magnitude lower gate leakage than that with oxide gate dielectric. Therefore, the cell leakage currents of high-k FinFET SRAM cells are mainly from the subthreshold leakage currents, thus exhibiting larger orientation dependence than that of oxide FinFET SRAMs. Compared with the (110,110,110) cell, the (110,100,110) cell with high-k gate dielectric shows

58% higher cell leakage, whereas the (110,100,110) cell with oxide gate dielectric shows 25% higher cell leakage.

IV. Conclusion

We have investigated the impacts of fin LER and NBTI/PBTI on the stability and variability of the 6T FinFET SRAM cells with high-k and oxide gate dielectrics, respectively. The 3-D mixed-mode simulations together with atomistic Monte Carlo simulations were used to investigate the variability due to fin LER and NBTI/PBTI-induced random discrete traps. The time-dependent $V_{\rm th}$ drift and variation due to NBTI/PBTI degraded the stability and variability of RSNM (significantly) and WSNM (slightly). Our paper has indicated that the optimum FinFET SRAM design had to consider the combined effects of the intrinsic process variability, surface orientation, the specific gate dielectric used, and the temporal variability introduced by NBTI/PBTI.

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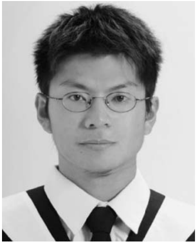

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