Heterogeneous Chip Integration Process for Flexible Wireless Microsystem Application

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***Abstract*—This paper presents a low-cost heterogeneous integration technology combining the previously developed bumpless radio-frequency (RF) system-on-a-package scheme with a special surface cleaning process to assemble a complementary metal–oxide–semiconductor chip with an organic substrate (SU-8/polydimethylsiloxane) by low-temperature Au–Au thermocompressive bonds ($< 200\ ^\circ$C) for flexible wireless microsystem fabrication. The RF performance of -15 dB return loss and -0.25 dB insertion loss at 40 GHz and above 6 MPa bonding strength of a microstrip-to-coplanar-waveguide interconnect transition between the chip and the substrate make the technology practical for flexible wireless microsystem integration.**

***Index Terms*—Au–Au thermocompressive (TC) bonding, bumpless interconnecting, flexible electronics, flip-chip, heterogeneous chip integration, surface cleaning.**

I. Introduction

FLEXIBLE electronics has recently become a critical research topic owing to great demand for personal portable devices [1], [2]. To keep the whole process temperature below the glass transition temperature ($< 200\ ^\circ$C) of flexible substrates, several technologies such as polydimethylsiloxane (PDMS) transfer printing [1], silicon-on-insulator active layer transfer [2], amorphous silicon transistor fabrication [3], organic transistor fabrication [4], and wafer transfer [5] have been developed for the realization of the flexible electronics. The fabrication processes included device substrate thinning, transferring, and backend metal rerouting. The active devices can be fabricated either directly on the flexible substrate or on the device substrate before thinning and transferring onto a flexible substrate. However, poor active device performance, low process flexibility to heterogeneous chip integration, or high manufacturing cost and complexity have resulted in the difficulty in technology implementation in commercial flexible microsystem manufacture. On the other hand, heterogeneous chip assembly schemes have been utilized for multichip module integration on an organic substrate for flexible electronics applications [6]–[9]. Chips fabricated by different process technologies such as complementary metal–oxide–semiconductor (CMOS), microelectromechanical systems (MEMS), and III–V can be individually optimized and fully integrated onto a flexible substrate to form a microsystem using conventional packaging technology. Although the process temperature of Cu lateral interconnects [6] and the bonding temperature of flip-chip process using solder bump or anisotropic conductive adhesive [7], [8] can be lower than 200 °C, large structure discontinuity between chips and substrates and high contact resistance will cause a drastic increase in return and insertion loss, respectively, in the interconnecting transition, which is not suitable for high-frequency applications.

Previously, we developed a bumpless interconnecting technology using Au–Au thermocompressive (TC) bonds to achieve good RF characteristics up to 50 GHz [10]. Via a self-interlocking design and flip-chip bonding technique to electrically and mechanically integrate a CMOS chip with a silicon carrier substrate, the interconnect transition can have diminutive parasitic effects to make the transmission of a high-frequency signal with the lowest power loss. Although the technology has shown its great potential in RF system-on-a-package integration, high-temperature TC bonding process ($> 300\ ^\circ$C) would make the technology impractical for the chip integration on a flexible substrate. Prior investigation has shown that the cleanness of bonding surface is a key process parameter to lower the bonding temperature [11]. Although Saito *et al.* has demonstrated a room-temperature surface-activated Cu–Cu bonding (SAB) [9] for chip assembly, the SAB has the characteristics of low process uniformity tolerance, long activation time (~30 min), and special customized tool requirement difficult for the implementation of mass production.

Therefore, in this paper, we will present a bumpless CMOS chip assembly scheme using a low-temperature Au–Au TC bond for flexible wireless microsystem fabrication. A low-cost surface-cleaning process is developed for contaminant removal in bonding interfaces for achieving a low-temperature Au–Au bond. Not only CMOS chips but also the other heterogeneous chips such as MEMS and III–V chips can be fully integrated with a flexible organic substrate using the proposed scheme to form a high-performance wireless microsystem.

II. Integration Process

RF CMOS chips are generally designed with microstrips as electrical interconnects for the sake of small form factor. Therefore, a flip-chip transition structure from a coplanar waveguide (CPW) to a microstrip has been extensively utilized for the investigation and design verification of RF packages [12]. The

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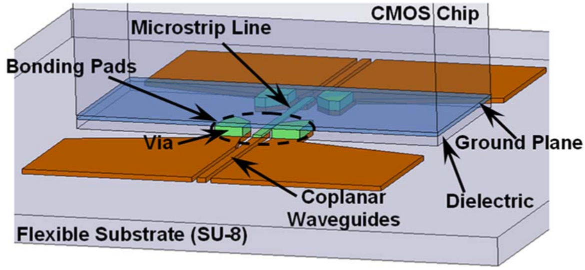

Fig. 1. Scheme of the designed interconnection structure includes two CPWs on flexible substrate and microstrip line on CMOS chip for characterization of the proposed integration technology.

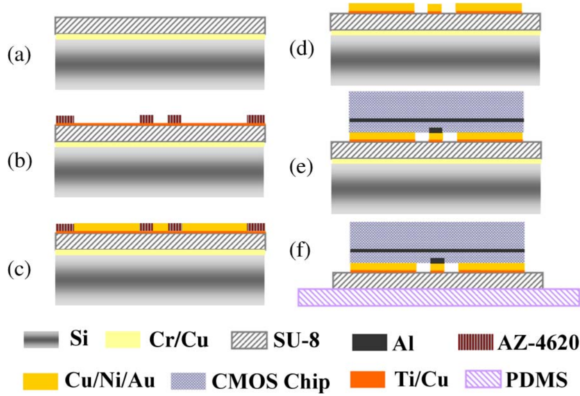

Fig. 2. Scheme of the integration process. (a) Deposition of a Cr/Cu sacrificial layer covered with a fully cured SU-8. (b) Ti/Cu seed layer deposition with PR patterning on the top. (c) Cu plating for the fabrication of CPW structure, followed by electroless Ni/Au plating for bonding. (d) PR and seed layer removal. (e) CMOS chip to SU-8 substrate bonding. (f) Si handle wafer detachment by sacrificial layer release in Cu etchant and then SU-8 film attachment on PDMS.

proposed integration process is demonstrated by a flip-chip transition structure, as shown in Fig. 1, including a microstrip and CPWs, which are designed with a 50-Ω characteristic impedance and 10.5-μm-wide signal line, and fabricated on a TSMC 0.18-μm RF CMOS chip and an SU-8 flexible substrate, respectively. The integration process, as shown in Fig. 2, begins with the flexible substrate fabrication given here.

Fig. 2(a) shows a silicon substrate that is first sputtered with 10/300-nm-thick Cr/Cu as a sacrificial layer, followed by SU-8 spin-coating. The thickness of the SU-8 layer is about 26 μm. After photopatterning the SU-8, the substrate is hard-baked at 200 °C for 2 h in order to make a fully cross-linked SU-8 for having a higher glass transition temperature Tg [13]. The baking process can enhance TC bonding reliability by preventing the sudden changes in terms of the coefficient of thermal expansion increase and the stiffness decrease in the SU-8 once the bonding temperature is larger than the Tg of SU-8. In addition, it can also increase the SU-8's chemical stability in the surface-cleaning process for bonding. After substrate baking, a 10/90-nm Ti/Cu seeding layer is deposited on the SU-8, followed by a photolithograph process using a 10-μm-thick AZ 4620 photoresist to define the region for the CPW fabrication, as shown in Fig. 2(b). After electroplating an 8-μm-thick copper CPW on that region, a serial process of 1-μm electroless Ni and 0.4-μm electroless Au is performed to metallize the Cu surface for the bonding, as shown in Fig. 2(c). Fig. 2(d) shows that the AZ 4620 and Ti/Cu seed layers are

TABLE I
SURFACE ELEMENT CONTENT ANALYSIS BY XPS BEFORE AND AFTER ACIDIC SURFACE CLEANING

Cleaning time (seconds)	Surface Contents (at.%)		
	C	O	Au
0	1.71	56.38	41.91
180	1.45	33.95	64.4

TABLE II
SPECIFIC CONTACT RESISTANCE VERSUS BONDING TEMPERATURE

Temperature(°C)	160	200	240
SCR(10^{-7} $\Omega\cdot$cm^2)	5.65±1.86	4.74±1.69	2.84±1.03

then sequentially removed using ACE, CR-7 T, and then BOE. On the other hand, the contact surfaces of TSMC 0.18-μm CMOS chip will be metallized using a maskless double-zincating process, followed by 0.2-μm electroless Ni deposition and 0.4-μm electroless Au. Detail CMOS chip preparation for the bumpless integration has been detailed in [10].

Piranha clean has been used as a standard cleaning procedure in CMOS front-end processes [14]. In fact, the piranha clean process can also be utilized in the proposed integration technique for bonding surface cleaning since the Au pads and passivation layer on the CMOS chips in the proposed integration scheme are all chemical inert to the cleaning chemical. Meanwhile, SU-8 is a photopatternable polymer with several superior material properties including good chemical stability, high flexibility, good electromagnetic properties, and wafer-level process capability that make it fascinating as a flexible substrate material. Thus, in the integration scheme, the acidic mixture solution of H_2SO_4 and H_2O_2 with the volume ratio of 3:1 is then employed as a cleanser for realizing low-temperature Au–Au TC bonds. Once both surfaces of the CMOS chip and SU-8 substrate are cleaned at about 50 °C, the CMOS chip is flip-chip bonded to the SU-8 substrate at the conditions of 180 °C and 100-MPa applied pressure for 3 min, as shown in Fig. 2(e). At final, the sacrificial Cr/Cu layer is chemically etched away in Cu etchant $(100{:}5{:}5\ H_2O : CH_3COOH{:}H_2O_2)$ to release the SU-8 substrate, which can be directly attached to a PDMS (Sylgard 184) supporting substrate to form a flexible microsystem, as shown in Fig. 2(f).

III. RESULTS AND DISCUSSION

The surface-cleaning process for low-temperature Au–Au TC bonding is characterized using a daisy chain structure with ten bumps formed within two Si chips. Table I lists X-ray photoelectron spectrometer measurements regarding the surface contents of Au bonding pads before and after the surface-cleaning treatment using the aforementioned cleaning process. The increase in Au content from 41.9% to 64.6% and the reduction in carbon and oxygen contents indicate that organic contamination has been effectively removed from the pad surface. Table II lists the measured specific contact resistance (SCR) versus the bonding temperature of Au–Au bonds under the conditions of 100-MPa applied pressure for 3 min. For a 4-min cleaning treatment, the bonding temperature can be lowered down to 160 °C with a $(5.65 \pm 1.86) \times 10^{-7}\ \Omega \bullet \text{cm}^2$ SCR.

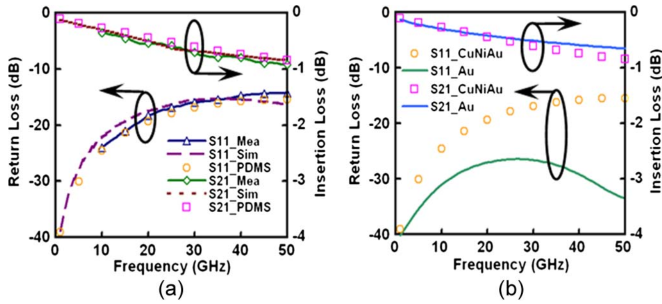

Fig. 3. (a) Comparison of the RF measurements and HFSS simulations on SU-8/Si and on SU-8/PDMS, respectively, of the designed transition structure. (b) Comparison of the simulation results of the transition on SU-8/PDMS with CPW made by either Cu/Ni/Au or pure Au, respectively.

Two-port S-parameters of the transition structure are measured using Agilent E8364B PNA and Cascade Infinity GSG probe in the frequency range of 10–50 GHz. In order to maintain measurement and calibration accuracy, the designed interconnect measurement is performed before handling wafer detachment rather than directly probing on the released SU-8. The measured S-parameters have excluded parasitic effects from measurement pads and moved reference planes near the edge of bonding pads using thru-reflect-line calibration. Fig. 3 shows the RF performance of the CPW–microstrip–CPW flip-chip transition, i.e., including two interconnect transitions and a microstrip. Better than -15 dB return loss and lower than -0.8 dB insertion loss up to 40 GHz have been achieved and closely matched with HFSS simulation results, as shown in Fig. 3(a). The measured return loss is as good as that of the microstrip-to-CPW flip-chip compensated interconnects with pure Au line structures on an Al_2O_3 substrate demonstrated by Wu *et al.* [12]. In fact, the return loss can be further improved with a better impedance match between the CPW and the microstrip by process optimization in terms of the CPW dimensions and metal thickness control. In addition, according to the simulation results, there is no obvious RF performance difference between the transition on the SU-8 substrate with a Si handle wafer and that with a PDMS substrate, as shown in Fig. 3(a). It can be attributed to the SU-8 layer, which is thick enough to prevent the possible influence of the sacrificial Cu layers on the performance.

After deducting the loss of microstrip (-0.31 dB at 40 GHz) from the measured insertion loss (-0.8 dB at 40 GHz), the loss of a bumpless interconnect transition can be calculated about -0.25 dB at 40 GHz. Owing to process limitation, electroless Ni simultaneously acting as the diffusion barrier layer between Au and Cu and the seeding layer of electroless Au is used in the fabrication of the interconnect transition and CPW in our case. Since the electroless Ni has a larger resistivity ($\sim$100 $\mu\Omega \bullet$ cm), which will result in a larger ohmic loss in comparison with that of Cu (1.7 $\mu\Omega \bullet$ cm) and Au (2.2 $\mu\Omega \bullet$ cm), the insertion loss performance is, therefore, worse than Wu's result (-0.065 dB at 40 GHz). Fig. 3(b) shows the comparison results of the transition on the SU-8/PDMS substrate with the CPW made by either Cu (8 μm)/Ni (1 μm)/Au (0.4 μm) or pure Au (9.4 μm), respectively. The insertion loss of one transition can be reduced down to -0.14 dB due to lower metal loss

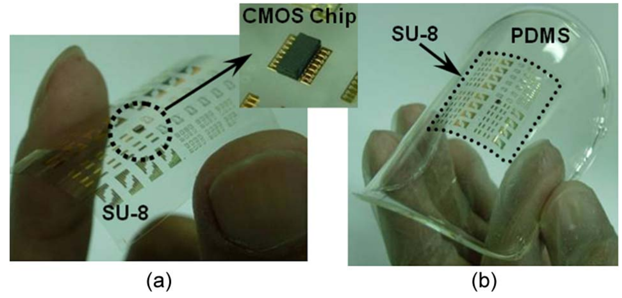

Fig. 4. Optical photographs of (a) detached SU-8 film. The enlarged inset photograph shows CMOS chip successfully bonded on SU-8, and (b) SU-8 attaches to and bends along with thick PDMS substrate.

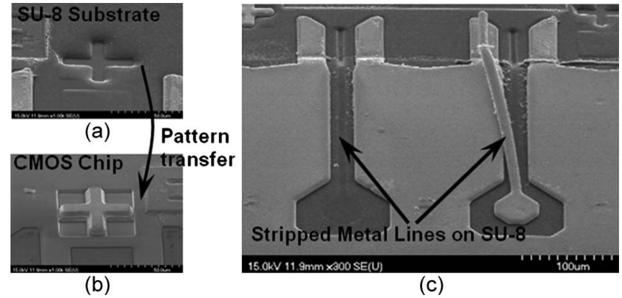

Fig. 5. Enlarged scanning electron micrographs of two bonded substrates, i.e., CMOS and SU-8, respectively, after forcefully separating the compressive bond. (a) Alignment mark torn away from the SU-8 substrate. (b) Alignment mark transferred onto the CMOS chip. (c) Fully stripped metal lines on the SU-8 substrate.

once the material of CPW is changed from Cu/Ni/Au to pure Au. Although there is still -0.075 dB loss difference between our technology and Wu's work, the first demonstration of the integration of CMOS chip to a flexible substrate with the characteristics of small bonding pad (minimum 10.5 μm in width) and simple structure design has revealed the potential of this technology for the integration of high-performance flexible wireless microsystems.

Fig. 4 shows optical photographs of a CMOS chip bonded with the SU-8 film released from a handling silicon wafer and the bonded sample attached to a PDMS film, respectively. The bonding strength is qualitatively characterized by forcefully separating the bonded substrates, as shown in Fig. 5. Either the Au pad is stripped away from the SU-8 and bonded to the CMOS chip or the Au pad is delaminated directly from the SU-8 after breaking the bonded interface, indicating that the bonding strength can be larger than 6 MPa [15]. Nevertheless, the detail process optimization and characterization of the surface cleaning and flip-chip bonding, and the investigation of the process correlation to the bonding strength and contact resistance are still underway.

IV. Conclusion

In summary, a low-cost heterogeneous chip integration technology using low-temperature Au–Au TC bonding has been successfully demonstrated with a good broadband electrical interconnect performance between a TSMC 0.18-μm RF CMOS chip and SU-8 polymer substrate. Not only CMOS chips but also the other heterogeneous chips such as MEMS and III–V chips can be fully integrated with a flexible organic substrate

using the proposed scheme to form a high-performance wireless microsystem.

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