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高性能混合訊號式介面積體電路
High-Performance Mixed-Signal Interface ICs

計畫編號 ： NSC-92-2215-E-009-032
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一、摘要

本計畫以整合資源方式，配合政府政策，因應產業需求，研發類比數位混合訊號式積體電路之設計技術。本計畫共分成六個子計畫。分別是(1)矽射頻元件模型與技術；(2)射頻電路之靜電放電防護技術與高速高低壓界面電路之研發；(3) 5 GHz 高性能無線通訊系統中主要積體電路的設計與整合；(4) 高性能類比數位介面積體電路；(5) 低電壓差動信號傳輸接收器之設計與量測；(6) 光纖傳輸之類比前端積體電路。子計畫一將建立主動與被動元件之射頻模型供電路設計與模擬。子計畫二則在設計晶片與電路板之間的可靠介面。計畫三將研究射頻無線電波與類比訊號之介面電路。計畫四將研究類比與數位訊號之介面電路。計畫五將研究數位與數位訊號之晶片介面電路。計畫六將研究光纖傳輸中光與數位訊號之介面電路。本計畫所研發的成果將會是積體電路設計之核心技術，有助於國內積體電路產業升級，尤其是無線及光纖通訊方面。而所訓練的設計人才也是國內目前迫切需求的。

關鍵詞：混合訊號式積體電路、介面、CMOS。

Abstract

This project combines the resources of several researchers to investigate the mixed-signal integrated circuit design techniques, so as to promote the government policy and satisfy the industry's need. There are 6 projects in this combined effort: (1) Si RF Device Modeling and Technology; (2) Development of On-Chip ESD Protection Technique for GHz RF Circuits and High-Speed Mixed-Voltage Interface Circuits; (3) The Design and Integration of Key Component ICs for 5 GHz High Performance Wireless Communication System; (4) High-Performance Analog-Digital Interface Integrated Circuits; (5) The Design and Testing of High Performance LVDS Transceiver; and (6) Analog Front-End Integrated Circuits for Optical-Fiber Transmission. Project 1 will build the high-frequency models for active and passive components suitable for circuit design and simulation. Project 2 investigates the reliable interfaces between chips and circuit boards. Project 3 investigates the interface circuits between wireless electro-magnetic waves and the analog domain. Project 4 investigates the interface circuits between the analog and the digital domains. Project 5 investigates the chip-to-chip digital interfaces. Project 6 investigates the interfaces between the optical-fiber light signals and the digital domain. The topics are all fundamental technologies for the design of high-performance integrated circuits, especially for wireless and optical fiber communications. In addition, the participated personnel will be trained to satisfy the need of the IC design industry.

Key Words: Mixed-Signal Integrated Circuits, Interfaces, CMOS.

二、緣由與目的

本整合型研究計畫係依據工程處微電子學門 VLSI/CAD 推動小組提出的「類比、混合訊號及 RF 模組設計」規畫書中的「子系統設計研究」項目規畫而成。計畫的主題為高性能之混合訊號介面積體電路。此處所謂的介面包括通訊傳輸媒介（如無線、光纖等）與積體電路之間的介面，類比與數位積體電路之間的介面，數位與數位積體電路之

間的介面，以及積體電路與周遭環境之間的介面。這些介面電路都需要使用混合訊號式積體電路設計技術。而本計畫就是研究其中的基本卻又先進的設計技術。而其成果將是支援無線通訊與光纖通訊之核心技術。

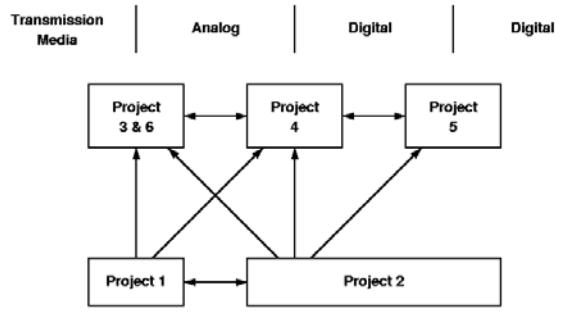

Fig. 1. 子計畫關係圖。

本計畫分成六個子計畫。分別是(1) 矽射頻元件模型與技術；(2) 射頻電路之靜電放電防護技術與高速高低壓界面電路之研發；(3) 5 GHz 高性能無線通訊系統中主要積體電路的設計與整合；(4)高性能類比數位介面積體電路；(5)低電壓差動信號傳輸接收器之設計與量測；(6)光纖傳輸之類比前端積體電路。圖 12.1 顯示了子計畫之間的相互關係。子計畫一將建立 MOSFET 之射頻模型供子計畫三與六使用。子計畫二則在設計晶片與電路板之間的介面供子計畫三至六使用。計畫三將研究射頻無線電波與類比訊號之介面電路。計畫四將研究類比與數位訊號之介面電路。計畫五將研究數位與數位訊號之晶片介面電路。計畫六將研究光纖傳輸中光與數位訊號之介面電路。計畫整合的最主要目的是設備與人力資源之整合。

本計畫其中之四位主持人所共同組成之研究群共用一間實驗室，所有學生之座位及實驗設備（如工作站和量測儀器）均共同使用。即使是個別計畫申請到的儀器設備也是如此，真正做到資源共享避免機器閒置之浪費。本計畫之子計畫所使用的設備都有共通性。如子計畫 1, 2, 3, 6 可使用相同的射頻量測儀器。而子計畫 2, 4, 5 則會使用相同的訊號源、示波器、與邏輯分析儀。

本計畫研究群學生的座位都在相鄰地方，學術研究會因為在一起而容易相互交流。子計畫雖各有不同的主題，但基本技能卻是共通的。例如子計畫 1, 2, 3, 6 對於射頻元件都必須深入了解，而且也都會使用到同樣的射頻量測技術。子計畫 2, 3, 4, 6 都須考慮到低雜訊電路的設計方法。而子計畫 4, 5 會特別重視時序訊號的抖動。也因為這些共通性，更增加了彼此交流與經驗傳承的誘因。

三、執行成果

A. 子計畫一：矽射頻元件模型與技術

The RF MOSFETs using 0.18 and 0.13 μm technology nodes are studied in this work. In additional to the low resistance silicide gate technology, the multi-fingered gate layout can further reduce the gate resistance by connecting in parallel. The finger width is 5 μm and the finger number is ranged from 20 to 70 at an increment of 10. The devices are characterized by DC I-V and 2-port S-parameters using HP8510C network analyzer from 300 MHz to 30 GHz. Then regular de-embedding procedure is followed to eliminate the parasitic effect of probe pad. The NFmin and associate gain are measured using standard ATN-NP5B Noise Parameter Extraction System up to 7.2 GHz that covers the most important frequency range for wireless communication. The extraction of dominate RF noise sources were performed by using an equivalent circuit model of intrinsic MOSFET with additional terminal resistance and shunt pass to ground at both input and output ports. To avoid non-physically based data in the equivalent circuit model, DC and low frequency data are measured and referred in circuit model.

The measured NFmin shows a general trend of decreasing RF noise with increasing the gate finger for MOSFETs in both technology nodes. A small NFmin of 0.93 dB is measured at 5.8 GHz using 50 gate fingers in 0.18 μm case, which shows the excellent noise performance at such high frequency and can be used for wireless LAN application. However, the NFmin increases by ~0.2 dB as scaling down from 0.18 to 0.13 μm technology node, which is opposite to the scaling trend. In addition, an abnormal increase of NFmin is observed as gate fingers increasing >50 in 0.18μm case.

A decreasing trend of associated gain with

increasing gate finger is measured for both MOSFETs using 0.18 and 0.13 μm technology nodes. Although the decreasing RF noise is achieved by decreasing Rg-nqs using parallel gate fingers, the increasing finger number also increases the undesired Cgd that decreases the associated gain.

The scaling from 0.18 to 0.13 μm technology improves the f_T to ~100 GHz that shows the good device performance. It is noticed that the f_T decreases as increasing the number of gate fingers. The increasing finger number improves the RF noise but also increases the parallel Cgd that decreases the f_T.

To further analyze the RF noise, we have developed a self-consistent model for both S-parameter and NF_{min}. Good matching between measured and modeled S-parameters and DC I-V (not shown) are obtained for RF MOSFETs in 0.13 μm nodes with the smallest 20 and largest 70 gate fingers. The good agreement between measured and modeled data is also obtained in other gate fingers of MOSFETs using both 0.13 and 0.18 μm technologies. Using the same model, we have further simulated the NF_{min} self-consistently with S-parameter and DC I-V. The Rg-nqs generates the dominate thermal noise in RF MOSFETs, which decreases as increasing parallel finger numbers. The Rg-nqs also increases with decreasing gate length from 0.18 to 0.13 μm nodes, which explains the abnormal increasing NF_{min} and opposites to the scaling trend. The next important noise source is from the shunt pass of Zg-sub. The increasing Zg-sub with increasing parallel gate fingers in 0.18 μm case fits well the abnormal increasing NF_{min} when gate finger > 50. The Zg-sub represents the RF signal loss to shunt pass to ground, which has been identified as the primary RF technology challenge for circuits on current VLSI technology using low resistivity Si substrates.

B. 子計畫二：射頻電路之靜電放電防護技術與高速高低壓界面電路之研發

本計畫第二年度的研究成果已經整理且發表了五篇 IEEE Conference 論文以及四篇 IEEE 國際期刊論文。研究的內容有應用於射頻電路的 ESD 保護電路、一般輸入/輸出端所使用的 ESD 保護電路和新型的高速高低壓界面電路。

在射頻電路的 ESD 保護電路研究中，我們首先提出新型阻抗隔絕技術(impedance-isolation technique)：LC-tank 結構，作為射頻低雜訊放大器(low noise amplifier, LNA)的靜電放電防護架構，並實際在 0.25-μm 互補式金氧半(CMOS)製程中實際製造驗證晶片，利用操作在射頻區段的雙端 GSG 量測方式來探討此架構的的高頻特性。在操作頻率為 2.7 GHz 的射頻電路中，這組帶有 LC-tank 的 ESD 保護電路不僅可以通過一般 ESD 測試規格的要求，而且只會對射頻電路造成-0.69 dB 的功率增益損耗和只增加 0.63 dB 的雜訊指數(noise figure)。另外，我們也成功地設計了一組可供 CMOS 寬頻段射頻電路(broadband RF circuit) 所使用的 ESD 保護電路。在高頻特性下其 S11, S21 有較佳的特性，並且其靜電放電防護能力大為提升，在人體靜電放電模式(HBM)下均超過 8 kV，均較傳統的架構更適用於寬頻段射頻電路。

我們也提出了幾種一般輸入/輸出端所使用的 ESD 保護電路，其中包含了利用互補式基體觸發矽控整流器(complementary substrate-trigger SCR)、雙重基體觸發矽控整流器(double-triggered substrate-trigger SCR)架構、Native-NMOS Triggered SCR (NANSCR)防護架構和靜電放電離子佈植的閘極接地 N 型金氧半電晶體(ESD-implantation ggNMOS)做為 ESD 保護元件的保護電路。

在高速高低壓界面電路領域，我們提出基體觸發技術(substrate-triggered technique)來加速高低壓介面的靜電放電保護元件的導通速度。而此項設計已在 0.25-μm CMOS 製程下製作驗證晶片，此設計不僅克服高低壓介面電路可靠度的問題，更進一步的提昇此靜電放電防護電路之 ESD 耐受能力達 60%。此外，我們提出一組新穎型的司密斯觸發高低壓界面電路，不需要使用厚的閘氧化層就可以避免薄閘極氧化層在高低壓界面電路所面臨的可靠度問題。在 0.13 微米 1 V/2.5 V CMOS 的製程中實際驗證，此高低壓介面電路，可以有效的操作在 3.3 V 的高壓輸出入訊號下，並且無閘極氧化層可靠度問題(gate-oxide reliability issue)，並能阻滯輸入

雜訊。

C. 子計畫三： 5 GHz 高性能無線通訊系統中主要積體電路的設計與整合

此計劃主要是以 0.18 ~ 0.13μm 場效金氧半電晶體的製程來實現 IEEE 802.11a 的 5-GHz 高頻段無線射頻金氧半電晶體收發機元件。預計完成的電路元件包括低雜訊放大器、混波器、多相位中頻濾波器、自動增益控制器、類比至數位資料轉換器、電壓控制振盪器、功率放大器。

本計畫接收器採用了雙正交接的架構。此架構由 Jan Crols 及 Michael Steyaert 於 1995 年提出，藉由將輸入及 LO 訊號都轉為正交形式，可以對 Multi-Path 電路製程上無法完全匹配的缺點有較大的容忍力，並降低了鏡像訊號的干擾。在提高整合度以及降低電路複雜性，發射機的架構選擇了 Direct Conversion 架構。

我們已設計了正交混波器及正交電壓控制震盪器電路。I-Channel 正交相位調變器和 Q-Channel 為相同的電路，但輸入的射頻訊號接線不同，並與 I-Channel 共用相同的電壓控制震盪器。因為此架構中需要四個降頻混波器，所以功率消耗將成為重要考量，在此電路中我們採用了疊加 (cascode) 的概念，使降頻混波器與正交電壓控制震盪器使用相同的電流，此方法將可明顯的減少功率消耗。

I-Q 訊號可視為一個複數訊號 I+jQ，所以一個 Polyphase Filter 即是一個複數的濾波器。因為所需要的訊號與鏡像訊號位於相同頻率的正負兩端，作為一個具備鏡像壓縮功能的 Polyphase Filter 便必須對正負頻率有足夠的選擇性。複數濾波器的轉移函數可以以四個實數濾波器組合而成。適當的選擇實數濾波器的轉移函數即可以完成對正負頻率作篩選的功能。此多相為濾波器的研究成果已撰寫成論文並發表。

本計畫所設計的功率放大器為兩級 Cascade 的架構，利用 Cascode MOS 的方式來提高兩級間 Isolation，以提高此功率放大器的穩定度；利用 Cascode MOS 的方式，可同時降低輸出端的大訊號振幅對 Gate-Drain Oxide 的電壓降，進而減輕 Oxide Breakdown 的問題。在 IEEE802.11a 的系統定義中，諸如 M-QAM 等的調變方式，需要較大的線性操作；然而考慮到功率效益 (power efficiency)，所以需要在線性度與功率效益間取得平衡，故將此功率放大器的兩級都操作於 Class-AB 的形式。在所選取的操作的頻帶 5.15~5.25GHz 下，能夠提供最大 200mW 的輸出功率。

本計畫所設計的正交相位電壓控制振盪器電路 (QVCO) 可調頻率可從 5GHz 至 5.4GHz，其 phase nose 在 1MHz offset 處為 -120dBc/Hz，功率消耗為 2.76mW。以上是模擬結果。

本計畫之整個 ADC 中包含了管線化的每一級、暫存器及數位錯誤修正等電路。此種架構中的每一級所處理的解析度為 log2 (2n-1) 位元，其中 n 為每一級所產生的數位輸出。在此次設計中 n 為 3，故其每一級所能處理的解析度為 2.8 位元，而最後一級為 2 位元。總共需要四級來完成全部八位元的解析度。在經過每一級的訊號處理之後所有的數位輸出將同時送往暫存器及之後的數位錯誤修正電路中，最後八位元的數位輸出將平行地被送出。其中每一級包含了一組取樣保持電路(sample-and-hold)、六組電壓轉電流電路(VIC)、一顆電流汲取式數位類比轉換器 (current steering DAC)、六組電流比較器及一組 thermometer-to-binary 編碼器，最後同時產生三位元 Binary 碼及六位元的 Thermometer 碼。然而最後一級只需要產生 2 位元 Binary 碼，所以只需要三組 VICs 及電流比較器即可。模擬結果顯示，輸入頻率為 20MHz，經過 FFT 分析後，其 SNDR 為 44dB，約為 7.01 位元的解析度。此開放式架構 ADC 亦已撰寫成論文發表。

D. 子計畫四：高性能類比數位介面積體電路

A time-interleaved analog-to-digital converter (ADC) has been studied for high-speed high-resolution applications. The ADC uses M identical N-bit ADCs operating in parallel at f_s/M clock rate to achieve an equivalent f_s sampling rate and N-bit resolution. For this project, N will be larger than 14, and f_s will be more than 100 MHz. A single input sample-and-hold amplifier (SHA) is preferred to avoid the potential sampling phase offset if M distributed SHAs are used instead. The design of the input SHA is crucial, since it

operates at sampling rate and needs to have N-bit resolution. The effects of the gain and offset mismatches among the sub-ADCs can be eliminated through calibration.

A high-speed high-resolution SHA is designed for time-interleaved ADC applications. Using the techniques of precharging and output capacitor coupling can mitigate the stringent performance requirements for the opamp, resulting in low power dissipation. Implemented in a standard 0.25 μm CMOS technology, the SHA achieves 80 dB spurious-free dynamic range (SFDR) for a 1.8 Vpp output at 100 MHz Nyquist sampling rate. The SHA occupies a die area of 0.44 mm^2 and dissipates 33 mW from a single 2.5 V supply.

A pipelined ADC has been designed. It consists of a front-end sample-and-hold amplifier (SHA), 17 radix-2 1.5-bit switched-capacitor (SC) pipeline stages, and a final 2-bit flash stage. It is known that gain errors caused by capacitor mismatches and opamp's finite gain in the pipeline stages can results in nonlinear A/D conversion for the entire pipeline. Calibration is required to achieve A/D resolution of more than 10 bits. A new background calibration scheme has been developed which can to measure and quantize the gain error of pipeline stages without interrupting the normal A/D operation. A pseudo random signal is injected into the pipeline stage. The exact value of its voltage gain can then be obtained by extracting the random signal from the ADC's output code. Using this scheme, the procedures for calibration and A/D conversion can be performed simultaneously without interrupting each other. An experimental ADC prototype was fabricated in a 0.25 μm 1P5M CMOS technology with MIM capacitors. Chip area is 3.8x3.6 mm^2. Operating at 40 MS/s sampling rate under a single 2.5 V supply, the analog block consumes a total of 350 mW of power, while the digital block consumes only 20 mW. Operating at 40 MS/s sampling rate, the ADC achieves a signal-to-noise-plus-distortion ratio (SNDR) of 73.5 dB and a spurious-free-dynamic-range (SFDR) of 93.3 dB with an 8-MHz sinusoidal input.

E. 子計畫五：低電壓差動信號傳輸接收器之設計與量測

The primary components of a data link are the transmitter, receiver, and cable. In the first year of this research project had designed a CMOS serial link transmitter and receiver at a data rate of 480 Mb/s using LVDS (low voltage differential signal). In the second year, we had tried to increase the data rate to 1~1.2 Gb/s using TSMC 0.35um 2P4M process with 3.3V supply. Three transmitters were designed, fabricated and measured. Three receivers were designed; two were fabricated and measured.

The transmitter with pre-emphasis is consisted of a PLL, an 8 to 1 data multiplexer, an 8 to 1 emphasis multiplexer and an emphasis data driver. With a 31.25 MHz reference frequency, the PLL can form a 125MHz output with eight uniformly distributed phases as clock signals for the multiplexer. Therefore we can achieve bit rates of 1 Gb/s. The multiplexer consists of two stages: a differential input multiplexer and a source coupled pre-driver. The pre-driver is composed of a source coupled pair with active inductive peaking load. The active inductive peaking load can substantially enhance the bandwidth of gain stages.

Oversampling receivers in this report uses 3 samples per bit. Each sample is compared with neighboring samples to indicate whether a data transition occurs or not. With this information, the bit value and boundary can be determined. The receiver consists of demultiplexing samplers, shift registers, a control logic circuit, a synchronizer, a phase shifter, phase selectors, a PLL and two interface circuits. In order to recover 1.2 Gb/s data input, the PLL output is 600 MHz with 12 phases outputs, i.e., equivalent to 7.2 GHz resolution. Six phase selectors are used to select 6 phases out of the 12-phase clocks. The Sampler produces 6 samples at 600 MHz rate, i.e, 2 data bits were sampled each time. Another receiver only samples 1 bit at 600 MHz rate. Therefore, its PLL is working at 1.2 GHz, but only has 6 phase outputs. Only 3 phase selctors are needed. Both circuits are operating at equivalent frequency of 7.2 GHz, but the die size of the second one is smaller. Yet another receiver is designed. It uses

half-rate clock and data recovery circuit. With input data at 1 Gb/s, the half-rate CDR is operating at 500 MHz.

Two kinds of LVDS transmitter circuit with pre-emphasis has been designed and fabricated in 0.35um 2p4M CMOS process. The pseudo differential transmitter is verified to perform at 1.2 Gb/s with 3.3V supply. The true differential data driver also worked at 1.2 Gb/s, but the transmitter has serious jitter. It may be from the PLL and the MUX circuit. Two oversampling receivers were fabricated. The bit error rate of the 2-bit over-sampling receiver is quite high. The 1-bit over-sampling receiver's PLL does not work properly. A new round the receiver will be design in next year.

四、發表論文（部分）

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