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光纖傳輸之類比前端積體電路
Analog Front-End ICs for Optical-Fiber Transmission

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一、摘要

本計畫將研發用於寬頻傳輸系統之高速類比前端積體電路。所考慮的光纖系統至少有 10 Gb/s 的傳輸速率。為了便於用數位訊號處理的技術來提升傳輸效能，前端電路須有足夠的動態範圍，並能將輸入訊號轉成多位元之數位訊號。規劃的電路規格有訊號頻寬超過 6 GHz，解析度超過 4 Bits，而等效取樣頻率超過 10 GSamples/s。其中的電路包括 Transimpedance Amplifier、可變增益放大器、取樣並保存電路、類比數位轉換器、以及時序產生器等。所設計之電路將以先進之 CMOS 製程，如 0.18 µm，製作成晶片來加以驗證。由於取樣並保存電路與類比數位轉換器將採用平行架構來提升等效取樣頻率，本計畫也會發展所需的校正技巧來修正增益不匹配、Offset 不匹配、以及取樣相位不匹配等各種誤差。所製作的晶片將用 Silicon-on-Package (SoP) 的技術加以封裝，以利於高頻量測。

關鍵詞：混合訊號式積體電路、類比前端電路、光纖傳輸、CMOS。

Abstract

This project is to design and realize analog front-end integrated circuits for high-speed optical fiber communication systems. In addition to having more than 10 Gb/s data transmission rate, the front-end, with sufficient dynamic range, will convert the received optical signals into multi-bit digital data, so that digital signal processing techniques can be used to improve transmission efficiency. The specifications for the circuits are at least 6-GHz signal bandwidth, at least 4-bit resolution, and at least 10-GSamples/s effective sampling rate. Circuits under studied include transimpedance amplifiers, programmable-gain amplifiers, sample-and-hold circuits, analog-to-digital converters, and clock generators. All circuits will be realized using advanced fabrication technologies, e.g., 0.18 µm CMOS. Since the parallel architecture will be applied in the sample-and-hold and analog-to-digital functions, the required calibration techniques will also be developed to correct errors such as gain mismatches, offset mismatch, and sampling phase mismatch. In addition, silicon-on-package (SoP) technology will be used for packaging the fabricated chip, so as to facilitate high-frequency characterization.

Key Words: Mixed-Signal Integrated Circuits, Analog Front-End Circuits, Optical Fiber Transmission, CMOS.

二、緣由與目的

光纖是目前具有最高傳輸量的通訊傳輸介質。其特性是寬頻，低損耗訊號傳輸，以及不易受外界雜訊之干擾。然而當傳輸速率大於 10 Gb/s 且傳輸距離長達數十以至數百公里時，光纖的信號傳輸便已不能再被視為是理想的完美傳輸。光纖傳輸的不完美特性主要包括傳輸損耗 (Attenuation) 、群延遲波形分散 (Differential Group Delay) 及色相分離 (Chromatic Dispersion) 等現象。雖然可利用不同型式的光纖互相做初步的補償，若在接收機電路使用等化器 (Equalizer) 對信號做進一步等化，則可得到更準確穩定的信號傳輸效能。另外，使用多位階傳輸訊號 (Multi-level Signaling) 可更有效地利用有限的頻寬，也是克服電路頻寬限制及光通道不完美特性的一種方法。而在長距離超高速傳輸時，利用 Forward Error Correction 的通道編碼方式來修正傳輸錯誤，以增進傳輸效益

的架構也必然會成為一種趨勢。以上所敘述的種種發展方向都會影響接收機的設計考量。如 Fig. 1 之所示，先進的接收機將會引進數位訊號處理 (Digital Signal Processing, DSP) 的技術。接收端所接收到的訊號不能視為只有 0 和 1 兩階，電路設計除了須符合頻寬和雜訊的要求之外，還要顧及線性度和足夠的動態範圍。至於時序及資訊的還原，則會使用多階的類比數位轉換器 (ADC) 配合 DSP 技巧以求得最佳功能。

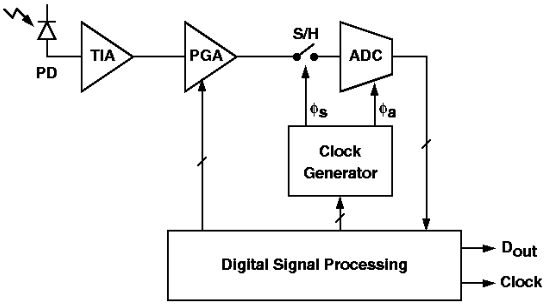

Fig. 1: 先進接收機架構。

本計畫不以 Over-Sampling Delta-Sigma Modulation 的技巧來提升系統的解析度。而是研究嚴謹的電路設計技巧，用來發展寬頻且低雜訊的類比電路，再配合數位校正（Digital Calibration）技術來提高電路本身的解析度。同時在設計時，還需考量深次微米 CMOS 製程元件特性及低電壓操作環境。由於現有的量測儀器不容易測試到預期的電路規格，本計畫會依需要發展量測技術。

基於以上的發展趨勢，本計畫將研究光纖系統接收機所需的 CMOS 類比電路設計技術。其中電路包括 TIA、可調變增益放大器 （Programmable-Gain Amplifier, PGA）、取樣並保持電路（Sample and Hold, S/H）、類比數位轉換器（Analog-to-Digital Converter, ADC）、以及時脈產生器（Clock Generator）。目標是 6 GHz 以上的訊號頻寬，4 Bit 以上的解析度，而等效取樣頻率則大於 10 GSamples/s。本計畫將會檢視放大器、取樣並保持電路、類比數位轉換器、以及時序產生器在高速應用中的基本限制。對於深次微米的元件特性，包含頻寬限制、線性度、和雜訊，也都會有深入的研究。所設計之電路都將以最先進之 CMOS 製程，如 0.18 um，製作成晶片。

在設計高速電路的過程中，所使用被動元件及其所造成的各類寄生效應均面臨極嚴苛的考驗，而其中最重要的技術瓶頸在於 IC 封裝的技術。傳統 IC 封裝中接腳是以細金線作 Bond Wire 連接晶片與外部接腳或外部元件，其寄生電感及晶片上 Bond Pad 的寄生電容在高速電路應用中，會使頻率響應變得極為不理想。在設計極限下，其 LC 等效電路之截止頻率（Cut-off Frequency）約只有 10~20 GHz。

為此，本計畫將引用覆晶接合技術以取代 Bond Wire 的使用，以另一個矽基座當作基板，將數個不同用途的晶片倒覆接合在此基板上作連接。覆晶接合技術不需要 Bond Wire 因此幾乎沒有寄生電感，且其 Bond Pad 可以做得更小，大幅降低其所產生的寄生電容。覆晶接合技術除了可應用在高速信號的需求外，亦可讓不同性質的晶片有適當的隔離，避免因矽基座耦合而造成串音雜訊干擾。在系統應用上，覆晶接合技術則是系統整合封裝 (System-in-a-Package, SIP) 的關鍵技術。

三、執行成果

A. Time-Interleaved ADC

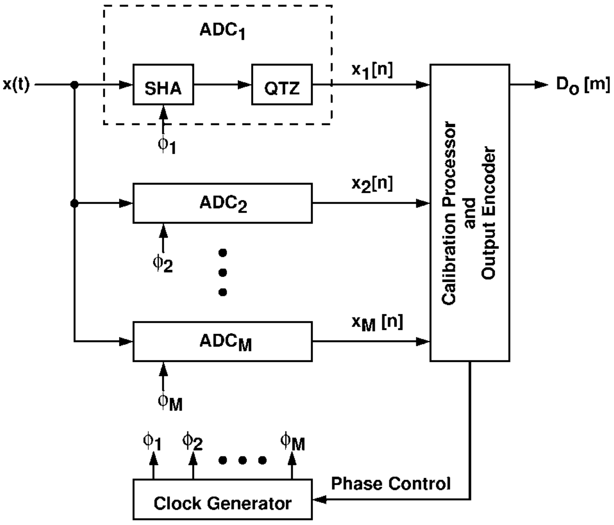

Fig. 1: Time-interleaved ADC.

The time-interleaved configuration shown in Fig. 1 has been studied for very high-speed analog-to-digital converters (ADCs). The entire A/D system consists of M identical N-bit sub-ADCs, $ADC_1 \cdots ADC_M$. Each sub-ADC, including a sample-and-hold amplifier (SHA) and a quantizer (QTZ), is driven by an f_c clock with different phase. The M clock phases, $\phi_1 \cdots \phi_M$, are equally spaced and constitute an entire clock period. The entire system achieves an equivalent $f_s = f_c \times M$ sampling rate and N-bit resolution. For this project, we want $N \geq 6$ $f_c \geq 1\,\text{GHz}$ and $M \geq 10$, to yield a 6-bit 10-GSamples/s ADC system.

Although the parallel architecture shown in Fig. 1 can achieve very high sampling rate, mismatches among the sub-ADCs introduce additional errors in normal A/D conversion. These mismatches, including sampling phase mismatch, gain mismatch, and offset mismatch, must be removed or calibrated in order to attain high resolution.

B. Background Calibration for Flash ADC

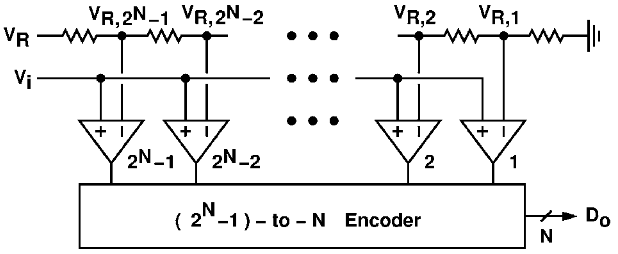

Fig. 2: Flash A/D architecture.

In this project, the sub-ADC employs the flash A/D architecture shown in Fig. 2. The N-bit ADC uses 2^N-1 comparators to simultaneously compare input, V_i, with 2^N-1 references, $V_{R,j}$, where j=1,2, ⋯, 2^N-1. The overall digital output D_o is obtained by encoding the binary output from the comparators. The flash architecture has the highest A/D conversion speed at a given N for a given technology.

For high-speed CMOS flash ADCs, it is the random input-referred offset voltages of the comparators that determine the ADC's linearity. The offset of a comparator with symmetric circuit configuration is caused by device's mismatches. Devices with larger size have better matching properties but also result in circuits of less power efficiency. Due to this design consideration for matching, there exists a fundamental trade-off among the speed, power, and accuracy of a CMOS flash ADC [1].

To overcome this speed-power-accuracy limitation, we have developed a new background calibration technique that can automatically trim the comparator's input offset voltage according to the statistical characteristic of input signals [2].

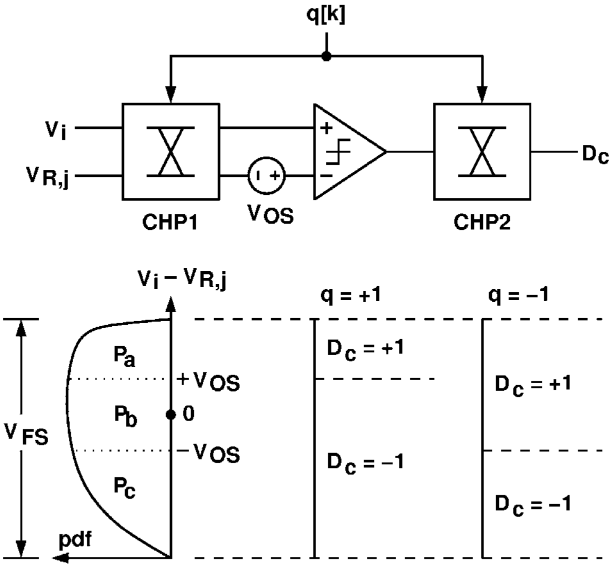

Fig. 3: A comparator with random choppers.

The proposed calibration scheme is based on the random chopping comparator shown in Fig. 3. This chopping comparator can replace the j-th comparator shown in Fig. 2. The comparator compares input, V_i, with a reference voltage, $V_{R,j}$, and then generates a corresponding binary output, $D_c[k] \in \{1,0\}$. The internal comparator has an input offset voltage of V_{OS}. The two choppers, CHP1 and CHP2, are controlled by a binary-valued random sequence, $q[k] \in \{+1,-1\}$. The CHP1 is an analog chopper, which passes the inputs unchanged when $q = +1$ and interchanges the inputs when $q = -1$. In CMOS technologies, CHP1 can be realized using 4 analog switches. The CHP2 is a digital chopper, which inverts its input when $q = -1$. Also shown in Fig. 3 is the probability density function (PDF) of $V_i - V_{R,j}$. One can detect the polarity of V_{OS} from the polarity of P_b, and then trim the V_{OS} accordingly. It is necessary for the

Fig. 4 shows the block diagram of the proposed background-calibrated comparator (BCC), which is composed of a random chopping comparator and a calibration processor (CP). The entire CP is realized in the digital domain. The CHP2 chopper in Fig.

3 becomes an XNOR gate with corresponding random sequence $q'[k]\in\{1,0\}$. The ACC1 accumulator records the difference between the number of $D_c[k]=1$ occurrences for $q[k]=+1$ and $q[k]=-1$\$. Thus, its output, R[k] is proportional to the probability P_b of Fig. 3. The bilateral peak detector (BPD) monitors the value of R[k] and generates a corresponding triple-valued output, $S[k]\in\{+1,-1,0\}$. The BPD has two thresholds, $+N_C$ and $-N_C$. When $R[k]\geq +N_C$, $S[k]=+1$. When $R[k]\leq -N_C$, $S[k]=-1$. Otherwise, $S[k]=0$. In addition, the ACC1 accumulator is reset to zero whenever $S[k]=+1$ or $S[k]=-1$. The S[k] sequence is integrated by the ACC2 accumulator. Its output, T[k], controls the comparator's input offset voltage, which can be expressed as: $V_{OS}[k]=V_{OS}[0]+\Delta V\times T[k]$, where $V_{OS}[0]$ is the initial offset and ΔV is the offset quantization step of the comparator.

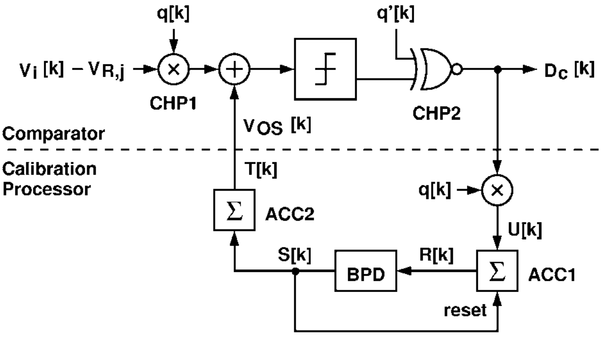

Fig. 4: A background-calibrated comparator (BCC).

There are two design parameters in this calibration scheme, i.e., ΔV and N_C, both of which affect the converging speed as well as the variation of offset. Large ΔV and small N_C result in fast converging speed but large fluctuation in V_{OS}. On the other hand, small ΔV and large N_C results in small V_{OS} fluctuation but also slow converging speed.

四、結論

本計畫 92 年度的執行重點在於高速 Time-Interleaved ADC 之設計。而此架構的主要問題包括取樣時間誤差以及子系統 ADC 之 Gain/Offset 不匹配等。我們將以 Flash A/D 的架構來設計子系統 ADC。如此可以避開 Gain/Offset 不匹配之問題。而我們也正在發展偵測取樣時間誤差的方法，並用來控制多相位時脈產生器。希望能就此消除取樣時間誤差。同時，我們在設計一個可數位控制之多相位時脈產生器電路。它可同時輸出 16 組不同之相位之時脈，而頻率可超過 1 GHz。此時脈產生器將會自動調整輸出相位來消除 A/D 取樣時間之誤差。

在單一子系統 Flash ADC 設計方面，我們發明了一種自動調整 ADC 內部比較器 Offset 之方法。如此可以設計出面積更小又更省電之 ADC。此自動調整方法是全數位式，而且不會影響 ADC 之正常運作。本新技術將申請專利，並用來設計一個 6-bit 1-GSamples/s 之 ADC。

對於未來之工作，我們將整合一個有 16 支子系統 Flash ADC 之 Time-Interleaved ADC 系統。此系統會包含所需的多相位時脈產生器並自動調整取樣時間誤差。最後目標是實現一個 6-bit 16-GSamples/s 之 ADC 晶片。

本計畫所發表的論文皆可放在主持人的網頁上：http://www.cc.nctu.edu.tw/~jtwu。

五、參考文獻

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