VI. Conclusion

This paper has detailed our experience in developing an energy-efficient MPEG-2 audio/video decoder, which we have since publicly distributed in source form [1]. Aware that FPGAs are inherently energy-*inefficient*, in this paper we have stressed that the efficiency gains we have made are at the architectural level, providing benefits regardless of the choice of implementation technology.

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A Digitally Testable $\Sigma - \Delta$ Modulator Using the Decorrelating Design-for-Digital-Testability

Sheng-Chuan Liang and Hao-Chiao Hong

***Abstract*—This paper demonstrates a digitally testable second-order $\Sigma - \Delta$ modulator. The modulator under test (MUT) employs the decorrelating design-for-digital-testability ($\mathrm{D^3T}$) scheme to provide two operation modes: the normal mode and the digital test mode. In the digital test mode, the input switched-capacitor network of the $\mathrm{D^3T}$ modulator is reconfigured as two sub-digital-to-charge converters (sub-DCCs). Each of the sub-DCCs accepts a $\Sigma - \Delta$ modulated bit-stream as its test stimulus. By repetitively inputting the DCCs with the same $\Sigma - \Delta$ modulated bit-stream but with different delays, the DCCs incorporates with the integrator to generate the analog stimulus in the digital test mode. The analog stimulus is analogous to the result of filtering the bit-stream with a two-nonzero-term FIR decorrelating term. Consequently, the $\mathrm{D^3T}$ MUT suffers less from the undesired shaped noise of the digital stimuli, and achieves better digital test accuracy. Measurement results show that the digital tests present a peak signal-to-noise-and-distortion ratio (SNDR) of 80.1 dB at an oversampling ratio of 128. The SNDR results of the digital tests differ from their conventional analog counterparts by no more than 2 dB except for the −3.2 dBFS test. The analog hardware overhead of the $\mathrm{D^3T}$ MUT only consists of 13 switches.**

***Index Terms*—Analog-to-digital conversion (ADC), built-in self-test (BIST), design-for-testability (DfT), integrated circuit testing, mixed-mode circuit, Sigma-Delta modulation.**

I. Introduction

Testing $\Sigma - \Delta$ modulators is very costly by conventional functional tests because of expensive automatic test equipment (ATE), a long test time, and a low-noise testing environment [1]. To reduce the test cost of the analog-to-digital converter (ADC), many design-for-testability (DfT), and built-in-self-test (BIST) techniques for ADCs have been proposed [2]–[11]. Most of the state-of-the-art works are functional-test based to provide must-have results for industry such as signal-to-noise ratio (SNR) and signal-to-noise-and-distortion ratio (SNDR) [12]. They also have purely digital input/output (I/O) during testing since digital signals have large noise margins against environmental noise and interference. To digitize the I/O, the compulsory analog stimulus generator (ASG) for conducting functional tests can not but be embedded. As a result, the test accuracy of the DfT/BIST heavily relies on the performance of the embedded ASG. Xing *et al.* proposes a histogram-based BIST strategy that can use a low-resolution ASG to characterize the transition levels of the ADC under test [13].

A robust approach to realize the embedded ASG is applying a $\Sigma - \Delta$ modulated bit-stream to a one-bit DAC followed by an analog anti-aliasing filter (AAF) [2], [3]. The single-bit characteristic of the $\Sigma - \Delta$ modulated bit-stream ensures that the generated analog stimulus is purely linear as far as the AAF is linear.

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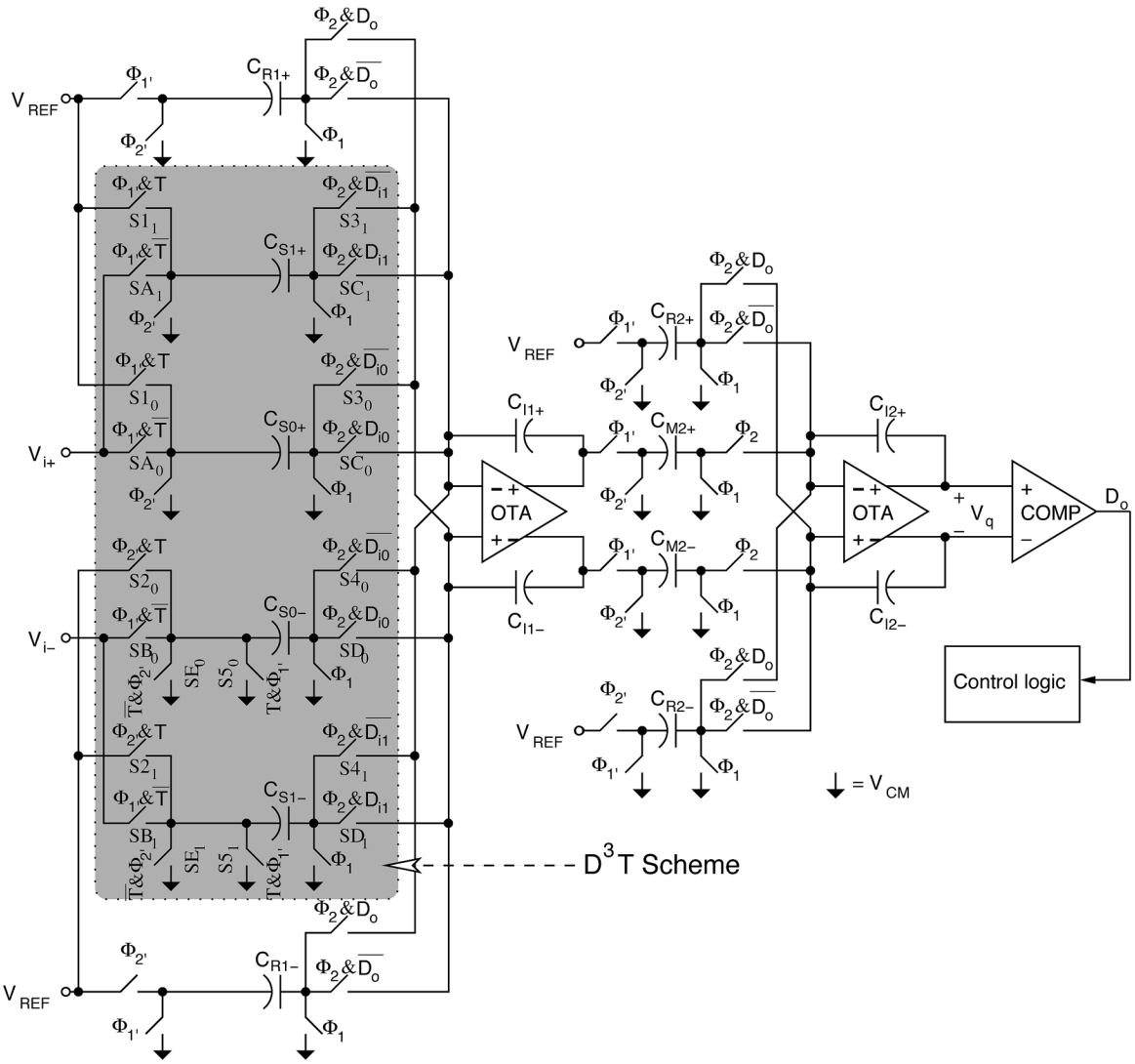

Fig. 1. Schematic of the proposed $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator.

Based on the similar idea of testing the ADC with a $\Sigma-\Delta$ modulated bit-stream, we proposed a design-for-digital-testability (DfDT) $\Sigma-\Delta$ modulator design in [14]. The DfDT $\Sigma-\Delta$ modulator is digitally testable with a $\Sigma-\Delta$ modulated bit-stream and needs no AAF. Experimental results show that the DfDT design has low area overhead, high fault observability, good test accuracy, and is at-speed testable. However, the SNDR result of the digital test degrades if the stimulus tone level exceeds -6 dBFS. The digital and the corresponding analog test results can have an SNDR difference as high as 12 dB at an oversampling ratio (OSR) of 128 [14]. The major issue of the DfDT tests in [14] is that the digital stimuli are $\Sigma-\Delta$ modulated bit-streams. They contain significant out-of-band shaped quantization noise which is absent in their analog counterparts. The digital stimulus' shaped noise correlates to the shaped noise generated by the modulator under test (MUT) and raises the inband noise power. As a result, DfDT tests always report lower SNDR results than their analog counterparts do. The digital stimulus' shaped noise also overloads the MUT at a higher stimulus tone level. Thus, the DfDT tests present a lower peak SNDR than analog tests do.

Reference [15] proposed a decorrelating design-for-digital-testability ($\mathrm{D^3T}$) scheme for $\Sigma-\Delta$ modulators to improve the test accuracy of digital tests. The $\mathrm{D^3T}$ design realizes an intrinsic finite-impulse-response (FIR) low-pass filter (LPF) to filter the digital stimulus. This additional LPF mitigates the undesired shaped noise of the digital stimulus and thus enhances the test accuracy. Behavioral and circuit simulation results verify that the $\mathrm{D^3T}$ tests are superior to the DfDT ones.

To more solidly validate the $\mathrm{D^3T}$ scheme and to evaluate its practical performance, we demonstrate experimental results of a second-order modulator with the $\mathrm{D^3T}$ scheme in this brief. Section II describes the design of the proposed $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator. Measurement results are shown in Section III. Finally, Section IV concludes this work.

II. Design of the $\mathrm{D^3T}$ Second-Order $\Sigma-\Delta$ Modulator

Fig. 1 shows the schematic of the proposed $\mathrm{D^3T}$ second-order $\Sigma-\Delta$ modulator. It is derived from the schematic of the DfDT modulator in [14] by splitting the original DfDT structure into two copies as shown by the shaded area of Fig. 1. In this way, the proposed $\mathrm{D^3T}$ design has a decomposition number of two so as not to increase too much additional KT/C noise to the digital test results [15]. Note that the proposed implementation requires only one reference (V_{REF}), while the design in the [15] requires two reference voltage sources (including $V_{\mathrm{REF}+}$ and $V_{\mathrm{REF}-}$). It saves the area and the power of an additional reference generator. The $\mathrm{D^3T}$ MUT has two operation modes.

1) Normal Mode: When the test mode control pin T is set to zero and the stimulus input pins $D_{ij}(z)$, $j \in \{0,1\}$ are fixed at one, the MUT operates in the normal mode. This setup turns off the switches $S1_j$ to $S5_j$, where $j \in \{0,1\}$. The configured MUT accepts the test stimulus from the primary analog inputs V_{i+} and V_{i-}. The $\mathrm{D^3T}$ MUT operates as a normal second-order $\Sigma - \Delta$ modulator does.

Let $Y_o \equiv 2D_O - 1$ be the normalized output of the MUT and $V_i(z) = V_{\mathrm{REF}} X_{\mathrm{ASG}}(z)$. The normalized I/O relationship of the MUT in the normal mode can be shown to be

$$Y_o(z) = \mathrm{STF}_{\mathrm{MUT}}(z) X_{\mathrm{ASG}}(z) + \mathrm{NTF}_{\mathrm{MUT}}(z) E_{\mathrm{MUT}}(z) \quad (1)$$

where $\mathrm{STF}_{\mathrm{MUT}}(z)$, $X_{\mathrm{ASG}}(z)$, $\mathrm{NTF}_{\mathrm{MUT}}(z)$ and $E_{\mathrm{MUT}}(z)$, stand for the signal transfer function (STF), the normalized test stimulus, the noise transfer function (NTF), and the quantization noise of MUT, respectively.

2) Digital Test Mode: By setting the digital test mode control pin T to one, the MUT operates in the digital test mode. In this mode, the switches SA_j, SB_j, and SE_j for $j \in \{0,1\}$ are off. The $\mathrm{D^3T}$ switched-capacitor network, indicated by the shaded area in Fig. 1, is reconfigured as two differential digital-to-charge converters (DCCs). Each of the DCCs accepts the corresponding single-bit digital stimulus D_{ij} as its input. The two DCCs convert the digital stimuli into two charge signals and the following integrator sums up the charge signals as the analog test stimulus in the digital test mode. The rest of the MUT convert the analog test stimulus into a $\Sigma - \Delta$ modulated output D_O as if they were in the normal mode. Because both the DCCs are single-bit, the generated analog test stimulus is nonlinearity-free. Hence, the $\mathrm{D^3T}$ MUT can achieve high test accuracy.

The required two digital stimuli D_{ij} are the same $\Sigma - \Delta$ modulated bit-streams except for a relative delay n [15]. We adopted the feed-forward, single-bit, third-order $\Sigma - \Delta$ modulator in [16] as our bit-stream generator (BSG) which modulates the normalized test stimulus $X_{\mathrm{ASG}}(z)$ to generate D_{ij}. Note that this BSG inherently can not accept a stimulus tone level higher than -3 dBFS; otherwise, the BSG will not be stable. The limited input level is a common restriction of high-order, single-bit $\Sigma - \Delta$ modulator designs [16].

Let $\mathrm{STF}_{\mathrm{BSG}}(z)$, $\mathrm{NTF}_{\mathrm{BSG}}(z)$, and $E_{\mathrm{BSG}}(z)$ represent the STF, the NTF, and the quantization error of the software BSG, respectively. Without loss of generality, the normalized digital stimuli $Y_{ij} \equiv 2D_{ij} - 1$, $j \in \{0,1\}$ can be shown to be

$$\begin{aligned} Y_{i0}(z) &= \mathrm{STF}_{\mathrm{BSG}}(z) X_{\mathrm{ASG}}(z) + \mathrm{NTF}_{\mathrm{BSG}}(z) E_{\mathrm{BSG}}(z) \\ Y_{i1}(z) &= z^{-n} Y_{i0}(z). \end{aligned} \quad (2)$$

We choose $C_{S0+} = C_{S1+} = C_{S0-} = C_{S1-}$ in this design so as to achieve the best shaped noise attenuation [15]. The normalized I/O relationship of the $\mathrm{D^3T}$ MUT in the digital test mode thus becomes

$$\begin{aligned} Y_o(z) = {} & H_{\mathrm{DCR}}(z) \mathrm{STF}_{\mathrm{MUT}}(z) \mathrm{STF}_{\mathrm{BSG}}(z) X_{\mathrm{ASG}}(z) \\ & + H_{\mathrm{DCR}}(z) \mathrm{STF}_{\mathrm{MUT}}(z) \mathrm{NTF}_{\mathrm{BSG}}(z) E_{\mathrm{BSG}}(z) \\ & + \mathrm{NTF}_{\mathrm{MUT}}(z) E_{\mathrm{MUT}}(z) \end{aligned} \quad (3)$$

where the decorrelating term is defined as

$$H_{\mathrm{DCR}}(z) \equiv \frac{(1 + z^{-n})}{2}. \quad (4)$$

Equation (3) indicates that the $\mathrm{D^3T}$ test can attenuate the digital stimulus' shaped noise as our desire since $H_{\mathrm{DCR}}(z)$ is actually an FIR LPF.

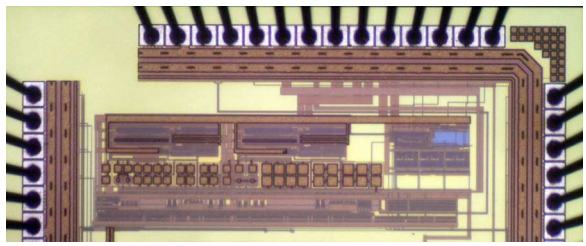

Fig. 2. Micrograph of the decorrelating DfDT second-order $\Sigma - \Delta$ modulator.

This decorrelating term puts real zeros on the frequencies of m/nf_{clk}, $m \leq n$ and these zeros attenate the shaped noise around them. We can tune the relative input delay n in (4) to achieve the best test accuracy. On the contrary, $H_{\mathrm{DCR}}(z)$ usually has negligible impacts on the stimulus term of (3). It is because the MUT operates at a large oversampling ratio (OSR) and thus the zeros of $H_{\mathrm{DCR}}(z)$ are far from the passband for a moderate n.

The $\mathrm{D^3T}$ MUT only consists of three active components: two operational transconductance amplifiers (OTAs) and a comparator. The OTAs of this design are similar to the folded-cascode OTA used in [14]. Circuit simulation results show that our OTA achieves an open-loop gain of 87.7 dB, a phase-margin of 68 degrees, and a unit-gain bandwidth of 100 MHz.

On the other hand, the design of the comparator is not as critical because the noise and the distortion generated by the comparator will be attenuated by the $\Sigma - \Delta$ modulation loop. This work uses a simple latch-type comparator.

III. Experimental Results

The $\mathrm{D^3T}$ MUT has been fabricated in a 0.18-μm 1.8/3.3 V mixed-mode CMOS process through the service of the Chip Implementation Center (CIC), Taiwan. The analog parts are realized by 3.3 V devices, while the digital circuits are realized using 1.8 V devices. Fig. 2 shows the micrograph of the $\mathrm{D^3T}$ $\Sigma - \Delta$ modulator. The active area of the $\mathrm{D^3T}$ MUT is 310 378 $\mu\mathrm{m}^2$. The total area of the additional analog switches and the control-signal generator for the $\mathrm{D^3T}$ scheme is less than 1200 $\mu\mathrm{m}^2$. All the additional circuits are placed on the free space of the layout, resulting in no area overhead.

The following measurements are all single-tone tests. The stimulus tone has a level of -4 dBFS and a frequency of 23/128 k times the sampling frequency unless otherwise noted. Each of the digital stimuli is a 128 k-sample bit-stream which is cyclicly applied to the MUT. The sampling frequency and the OSR are set to 6.144 and 128 MHz, respectively, corresponding to a passband of 24 kHz. The minimum four-term window is applied to derive all spectra.

A. Choice of the Relative Input Delay

Fig. 3 shows the measured SNDR results with various n. We also added the measurement result of the corresponding analog test as a reference. The digital-test-mode-enabled $\mathrm{D^3T}$ MUT has the lowest SNDR, 75.9 dB, when $n = 0$. In fact, setting n to zero turns the decorrelating term of the $\mathrm{D^3T}$ MUT to one and thus disables the LPF capability of the decorrelating term. In other words, the $\mathrm{D^3T}$ MUT degenerates into a DfDT one. Consequently, the shaped correlation between the MUT and the digital stimulus becomes higher and degrades the measured SNDR.

The SNDR result closest to that of the analog test is 80.1 dB when n equals 4. This value is 4.2 dB higher than the DfDT case ($n = 0$). Further increasing n does not improve the test accuracy because a larger n narrows the attenuation bands of the zeros of the decorrelating term. Consequently, some significant high-frequency spurs of the digital stimuli may not be effectively suppressed. Fig. 3 also shows

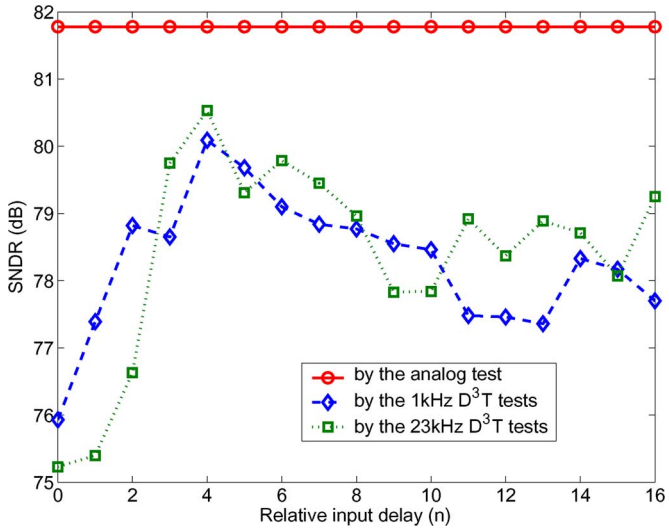

Fig. 3. Measured SNDR results of the $\mathrm{D^3T}$ tests with various relative input delays. The stimulus tone level is -4 dBFS.

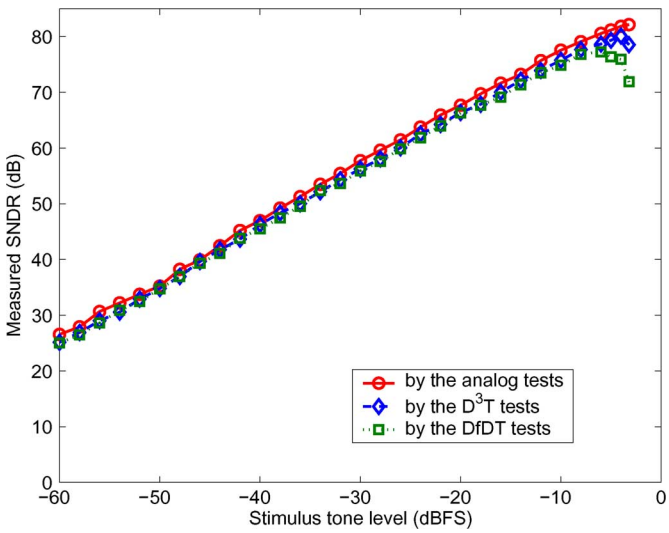

Fig. 4. Measured SNDR versus stimulus tone level.

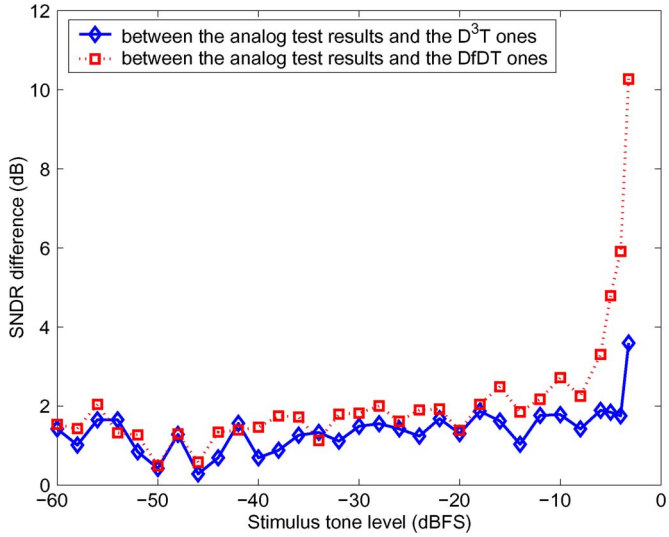

Fig. 5. SNDR difference versus stimulus tone level.

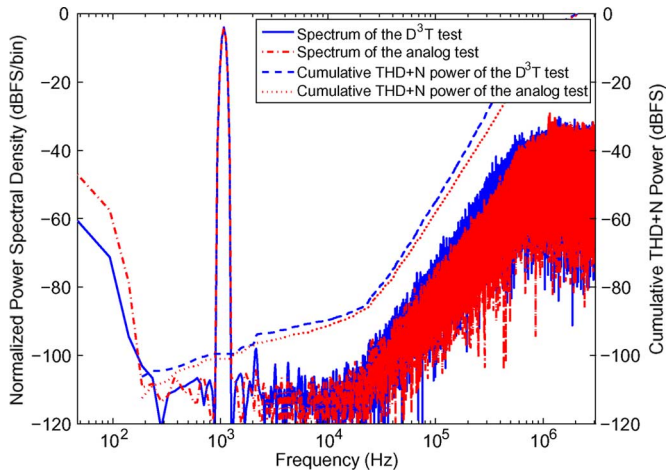

Fig. 6. Measured output spectra of the -4 dBFS analog test and the -4 dBFS $\mathrm{D^3T}$ test.

the measurement results of 23 kHz tests. The highest SNDR occurs at $n = 4$ as well. It shows that the best n seems to be stimulus frequency independent.

We measured all the five samples we had. Four of them achieve their highest SNDRs when $n = 4$. Only one sample achieves its peak SNDR at $n = 6$. Yet the $n = 4$ test gives the second highest SNDR for this exclusive sample. The SNDR difference between the two tests is only 0.2 dB.

B. Dynamic Range Tests

Fig. 4 shows the measured SNDRs of the MUT at different stimulus tone levels. We sweep the stimulus tone level from -60 to -3.2 dBFS. The $\mathrm{D^3T}$ tests are set with the same relative input delay of 4. In particular, we add the measurement results of the degenerated DfDT MUT (setting $n = 0$) as references to demonstrate the effectiveness of the $\mathrm{D^3T}$ scheme. The measurement results show that the $\mathrm{D^3T}$ test results are very close to their analog counterparts.

The dynamic range (DR) obtained by the $\mathrm{D^3T}$ test is 85.2 dB. This value is very close to the normal mode test result which is 86.6 dB. The peak SNDRs of the $\mathrm{D^3T}$ test and the DfDT test are 80.1 dB and 77.3 dB which occur at -4 dBFS and at -6 dBFS, respectively. The $\mathrm{D^3T}$ test successfully extends the peak stimulus tone level of the digital tests by 2 dB. Fig. 5 plots the measured SNDR differences between the analog tests and the corresponding digital ones to compare both tests with each other. The $\mathrm{D^3T}$ tests outperform their DfDT counterparts in most cases. In the range of -60 to -4 dBFS, the maximal SNDR difference between the $\mathrm{D^3T}$ tests and the corresponding analog ones is less than 1.9 dB.

On the contrary, the DfDT SNDR results diverse from the corresponding analog ones more severely as the stimulus tone level approaches the full scale. Within the same -60 to -4 dBFS range, the peak SNDR difference between the DfDT and the analog tests is as high as 5.9 dB. As has been discussed in Section I, the large shaped noise of the digital stimulus leads to the increased SNDR differences [15].

The -3.2 dBFS $\mathrm{D^3T}$ test reports an SNDR that differs from the corresponding analog test result by 3.6 dB. It is because such a large stimulus severely overloads the MUT, though the decorrelating term alleviates the shaped noise of the digital stimulus. Nevertheless, the $\mathrm{D^3T}$ test still achieves 6.7 dB improvement over the corresponding DfDT test.

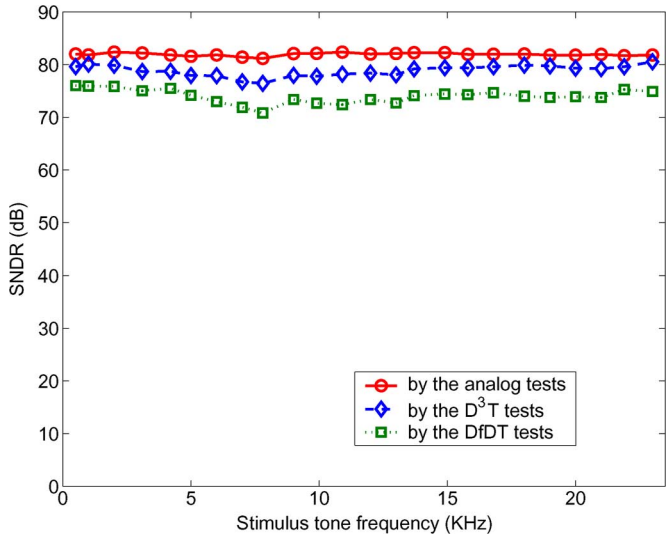

Fig. 7. Measured SNDR versus stimulus frequency. The stimulus tone levels are all −4 dBFS.

TABLE I
PERFORMANCE SUMMARY

Test items	Test method		
	Analog	D^3T	DfDT
Peak SNDR @1 kHz	82.1 dB @−3.2 dBFS	80.1 dB @−4 dBFS	77.3 dB @−6 dBFS
Dynamic range[1]	86.6 dB	85.2 dB	85 dB
SFDR[2]	98.0 dBc	94.9 dBc	88.0dBc
Maximum SNDR difference[3]	—	1.9 dB	5.9 dB
MUT's offset	−43.7 dBFS	−57.3 dBFS	−57.6 dBFS
MUT's gain error	+0.009 dB	−0.009 dB	−0.01 dB

[1] Dynamic range ≡ SNDR @-60 dBFS (in dB) + 60 dB [17].

[2]: Test results of the −4 dBFS, 1 kHz tests.

[3]: For the stimulus tone levels within −4 dBFS.

Fig. 6 compares the output spectrum of the −4 dBFS D^3T test with that of the corresponding analog test. The two spectra are similar to each other, but show different offset values for the same MUT. The offset reported by the digital test is more accurate since the offset is determined by the MUT itself. While the ASG, the analog buffers on the evaluation board, and the MUT contribute the measured offset together in the analog test. The SNDR difference between the two tests in Fig. 6 is less than 1.6 dB. However, the spectrum of the analog test shows no significant harmonic tone within the passband, whereas the D^3T test reports some. This is because the input power of the −4 dBFS D^3T test is higher than that of the analog test owing to the residue shaped noise of the digital stimulus. This higher input power somewhat overloads the digital-test-mode-enabled MUT and results in the harmonics. A solid evidence for our argument is that these harmonics almost disappear in the output spectrum of the −5 dBFS D^3T test.

C. Full Power Bandwidth Tests

Fig. 7 illustrates the measured SNDR values of the MUT vs. stimulus frequency. The D^3T tests show better correlation to the analog tests than the DfDT tests do over the whole passband. When the stimulus frequency is 23 kHz, the measured SNDR results of the analog, the D^3T and the DfDT tests are 81.8, 80.5, and 74.9 dB, respectively. The experimental results reveal that the D^3T digital tests can be used to test the full power bandwidth of the MUT with good test accuracy.

Table I summarizes the performance of the D^3T second-order $\Sigma-\Delta$ modulator. The MUT receives the largest input power in the DfDT test and thus is overloaded the most severely. As a result, the DfDT test presents the worst SFDR. The D^3T test gives a closer SFDR to that of the analog test because its decorrelating term reduces the digital stimulus' shaped noise power.

IV. Conclusion

This paper demonstrates a D^3T second-order $\Sigma-\Delta$ modulator fabricated in 0.18-μm CMOS. Measurement results show that the D^3T digital tests report a peak SNDR of 80.1 dB for the MUT, which is 2.8 dB better than the result obtained by the DfDT tests. At an OSR of 128, the D^3T tests and their analog counterparts have SNDR differences less than 2 dB when the stimulus tone level is not higher than −4 dB. The analog hardware overhead of the D^3T design only consists of 13 switches, which is negligible. The D^3T design also ensures high fault observability because most of the MUT's components are active and have the same functions and loads in both the modes.

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