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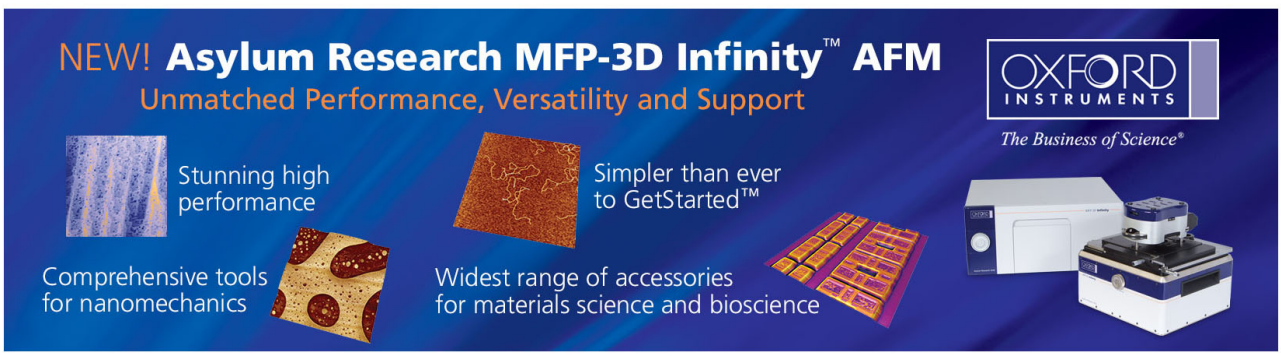

Impact of static and dynamic stress on threshold voltage instability in high-k/metal gate n-channel metal-oxide-semiconductor field-effect transistors

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This letter investigates the impact of static and dynamic stress on threshold voltage (V_{th}) instability in ultrathin n-channel metal-oxide-semiconductor field-effect transistors with hafnium-based gate stacks. Experimental results indicate V_{th} shift under dynamic stress is more serious than that under static stress due to charge trapping within the high-k dielectric. Capacitance-voltage techniques demonstrated that electron trapping under dynamic stress was located in the high-k dielectric near the source/drain overlap region rather than throughout the overall dielectric layer. This implies in real circuit operation, the phenomenon of electrons trapped in high-k near the source/drain overlap is the main issue affecting V_{th} instability. © *2011 American Institute of Physics*.
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With the scaling down of metal-oxide semiconductor field electrical field transistors (MOSFETs), the aggressive shrinking of the conventional SiO_2-based dielectric in recent years has approached its physical limits. To meet the International Technology Roadmap for Semiconductors, Hf-based dielectrics have been heavily investigated as a replacement for SiO_2 gate insulator to reduce both tunneling gate leakage and power consumption in complementary metal-oxide-semiconductor circuits.[1–3] However, charge trapping in high-k gate stacks remains a key reliability issue, since it causes the V_{th} shift and drive current degradation.[3–5] This is believed to happen due to the filling of pre-existing traps in the high-k dielectric layer, rather than trap creation over the device operation time.[6–8] However, these studies mainly focused on charge trapping characteristics under the static bias condition. There are a few studies investigating the impact of dynamic operation on V_{th} instability in Hf-based n-MOSFETs, noteworthy because in real circuits the devices are generally operated in the dynamic condition. Therefore, this work further investigates V_{th} instability of Hf-based n-MOSFETs under the dynamic bias operation. The static condition was also performed on the identical device for a comparison.

The HfO_2/TiN n-MOSFETs used in this study were fabricated using a conventional self-aligned transistor flow through the gate first process. For the gate first process devices, high quality thermal oxide with thickness of 10 Å was grown as an interfacial layer oxide layer. After standard cleaning procedures, 30 Å of HfO_2 films were sequentially deposited by atomic layer deposition. Next, 10 nm of TiN films were deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The source/drain (S/D) and poly-Si gate activation were performed at 1025 °C.

The devices are stressed in the dynamic condition with 50% duty cycle. A pulse train with high-voltage of 0.5 V $+V_{th}$, low-voltage of 0 V, and frequency of 100 kHz was applied to the gate electrode. The static bias stress was also performed at 0.5 V$+V_{th}$ for comparison. The source, drain, and body terminals were all grounded during stress. Variations in the V_{th} were monitored from the drain current-gate voltage (Id-Vg) and capacitance-voltage (C-V) transfer characteristics. In the gate-to-channel capacitance (Cgc) measurement, a capacitance measurement high (CMH) was applied to the gate electrode, and both S/D electrodes were connected to a capacitance measurement low (CML). In the gate-to-body capacitance (Cgb) measurement, the gate and body electrodes were connected to CMH and CML, respectively. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer.

Figure 1(a) shows the Id-Vg transfer characteristic curves with 50 mV drain voltage under initial and after static

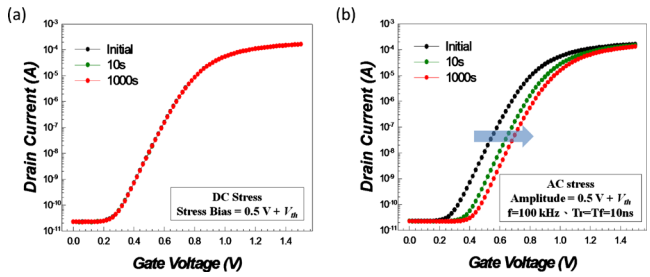

FIG. 1. (Color online) Id-Vg transfer characteristic curves of high-k/metal gate MOSFETs as function of stress time under (a) dc stress and (b) ac stress. The sweep was done at Vd=0.05 V for both curves.

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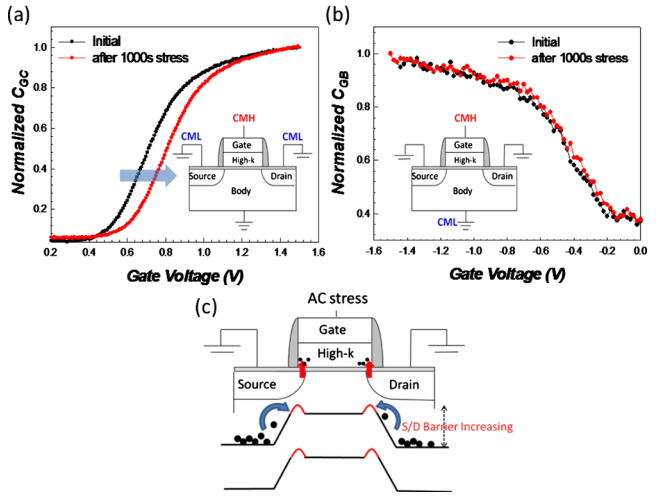

FIG. 2. (Color online) (a) Cgc-Vg and (b) Cgb-Vg transfer characteristics under initial and after dynamic stress. The inset shows their respective measurement method. (c) Schematic diagram of the high-k/metal gate MOSFET and its energy-band diagram after dynamic stress.

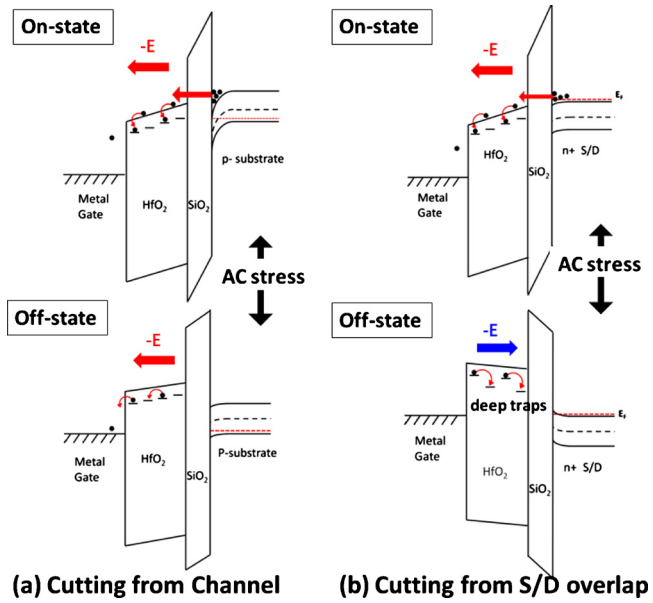

FIG. 3. (Color online) Variation in energy-band diagram cutting from (a) channel region and (b) S/D overlap region during dynamic stress.

stress. Obviously, the device exhibits no degradation under the static positive gate bias of 0.5 $V+V_{th}$ over a period of 1000 s. However, when dynamic stress was applied to the identical device, the V_{th} shifts to the positive direction and on-current is degraded after the stress, as shown in Fig. 1(b). In addition, the transfer curves shift has not been accompanied by subthreshold swing degradation, meaning that there is no creation of extra interface states. Therefore, most of the V_{th} shift can be attributed to the charge trapping within the high-k dielectric layer.

The results above are inconsistent with the general realization that the dynamic bias causes less degradation due to its shorter effective stress time.[9] To further understand this phenomenon, the Cgb-Vg and Cgc-Vg transfer characteristics under initial and after dynamic stress are measured and shown in Figs. 2(a) and 2(b), respectively. It can be observed that the Cgc-Vg curves shift in the positive direction after dynamic stress, which is consistent with the Id-Vg result in Fig. 1(b). However, Fig. 2(b) shows that Cgb measured between the gate and the body terminals has no significant change before and after stresses. No variation in flat band voltage suggests that in the dynamic condition, electrons cannot be really captured in throughout the overall high-k dielectric layer. Therefore, the ΔV_{th} in Figs. 1(b) and 2(a) can be mainly attributed to the electrons trapped near the S/D overlap region. Figure 2(c) illustrates that the captured electrons raise the band energy upward and induce additional energy barriers near the S/D overlap. Both barrier heights resist the electrons supplied from the S/D, leading to the positive shift in the Cgc-Vg measurement. However, the local electrons trapped near the S/D overlap region have no influence on the charge variation during the Cgb-Vg measurement. Therefore, the flat band voltage in the Cgb-Vg curves has no significant change before and after stresses.

The previous proposed charge trapping model[10,11] suggests that in the period of on-state stress, a small portion of electrons can be captured instantly in the shallow traps of the high-k dielectric, as shown in the Fig. 3(a). Then, at off state, the built-in electronic field established by work function difference between metal gate and p-substrate drives these trapped electrons to migrate toward the gate electrode by Poole–Frenkel emission.[4] This same electrical field direction during on-state and off-state continuously drives these elections, captured in shallow traps, toward the gate electrode. Therefore, few electrons can be captured in the deep traps of high-k dielectric above the channel region. This is also the reason why the charge trapping phenomenon cannot be observed under static bias stress. The constant electrical field drives the electrons to migrate toward the gate electrode continuously, leading to few electrons captured in the deep traps. When we consider the S/D overlap region, the on-state bias results in the electrons still being captured in the shallow traps, as shown in Fig. 3(b). In the off-state stress, however, due to the positive value of work function difference between TiN and N^+ S/D, a contrary direction of electrical field exists and prompts the trapped electrons to migrate toward the N^+ S/D. The different electrical field directions between on and off states does not allow these electrons in the shallow traps to have sufficient time to escape from the high-k dielectric. This significantly increases the possibility of electron capture in the deep traps of high-k dielectric.

To further confirm this phenomenon, the dynamic stress condition was imposed upon an identical device, with the exception of a floating source terminal. The gate-to-drain capacitance (Cgd) and gate-to-source capacitance (Cgs) measurements before and after stress are shown in Figs. 4(a) and 4(b), respectively. After the stress, the Cgd-Vg curves have a similar shift to those in Fig. 2(a) due to the energy barrier induced by trapped electrons in the drain overlap region, as shown in the inset of Fig. 4(a). However, Fig. 4(b) shows no significant change in the Cgs-Vg curves under this stress condition. This evidence indicates that there is no additional energy barrier near the source overlap region, due to the fact that the dynamic bias cannot be applied across the overlap region between the gate and floating source terminals. This result further verifies that charge trapping in the overlap region is an effect of variation in electrical field.

In summary, we observed that the V_{th} instability induced by charge trapping under dynamic stress was more serious than under static stress. C-V techniques verified that electron

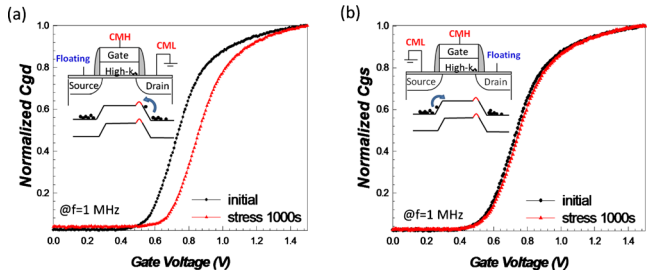

FIG. 4. (Color online) (a) Cgd-Vg and (b) Cgs-Vg transfer characteristics under initial and after dynamic stress. The inset shows their respective measurement method and illustrates the energy-band diagram after dynamic stress for a device with a floating source.

trapping under ac stress is located in the high-k dielectric near the S/D overlap region rather than throughout the overall dielectric. This can be attributed to the influence of different electrical field directions in the S/D overlap region during dynamic stress. These results suggest that the overlap region in high-k/metal gate stacks is the primary charge trapping issue in the real circuit operation.

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