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晶圓製造廠生產控制策略全面性整合之研究

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中文摘要

本計畫主要目的在探討晶圓製造廠現場管理策略之整合性研究；主要包括交期指派、訂單投料、現場派工及、不良品重加工等現場控制策略。計畫中利用類神經網路及線性迴歸等技術分別發展交期指派模式，並進行四項模擬實驗，以驗證晶圓廠現場控制策略間的交互關係，進而提出能有效改善晶圓廠各項績效指標之策略整合建議。

實驗一探討不良品重工需求對晶圓廠現場控制策略的影響。主要納入的現場控制策略以訂單投料及現場派工為主，並以實務上經常應用且具代表性的法則為限。透過模擬驗證在不同程度的不良品重加工需求下，各項績效指標之表現狀況。研究發現重工對系統績效指標之影響十分顯著，訂單投料及現場派工等控制策略的績效，明顯受重工需求的影響。若能正確選用現場控制策略，可有效改善重工對系統績效的衝擊。在不同重工需求下，本計畫提出相關現場控制策略之建議。

實驗二以訂單投料、現場派工、及不良品重加工等現場控制策略間之關係為核心，探討不同策略組合對晶圓廠系統績效的影響。由模擬及統計分析結果發現，多數投料法則若選用適當的現場派工及重工法則搭配可大幅改善其績效；但沒有任何特定法則可兼顧各項績效指標。因此實務上應針對不同系統狀況，選用合適的現場控制策略。各項現場控制策略應整體規劃，包括訂單投料、現場派工、及重工策略等應一併考慮，以合適的策略組合有效提升系統績效。計畫中針對不同績效指標提出適合的策略組合建議。

交期指派是晶圓廠現場管理決策的要務之一，決定合適的訂單交期並將產品準時送交客戶將可有效提升客戶服務水準並強化競爭優勢。實驗三透過類神經網路預測製造前置時間，進而決定交期。本計畫發展一個以類神經網路為基礎，並結合系統模擬及統計分析技術的交期指派模式，同時構建以迴歸技術為基礎的交期指派法則，並納入傳統交期指派法則作為標竿，進行績效評估。從模擬及統計分析的結果發現，以類神經網路為基礎的交期指派法則比其他類型的交期指派法則有較高的敏感度與準確性，訂單延誤的狀況亦可大幅改善。另外，傳統交期預測方法則以 JIQ 表現較佳，以迴歸技術為基礎的交期預測方法則以 SFM_Sep 較佳。

實驗四探討不同投料及派工法則下，各類交期指派法則的績效表現。在特定投料及派工法則下，選用合適的交期指派法則來預估交期，會直接影響系統中交期相關績效指標的表現。從模擬及統計分析的結果可發現，類神經網路為基礎的交期預測模式明顯優於其他方法，尤其在平均延遲時間上的表現最佳。本計畫整理出在不同現場管理策略組合及績效指標要求下適合的交期指派法則建議。

關鍵詞：*晶圓廠、現場管理、交期指派、訂單投料、現場派工、重工、類神經網路*

英文摘要

The purpose of this project is to study the integration of SFC strategies, like as due date assignment, order review and release, dispatching, and rework rules. The artificial neural network and regression techniques will be adopted to develop the ANN_Based and Reg_Based due date assignment rules for a virtual wafer fabrication plants. There are four simulation experiments in the project for testing the interaction of SFC strategies in wafer fabrication.

The first experiment is focused on the effect of rework operations on the shop floor control's strategies, including order review/release and dispatching. It will try to determine the performance of various production control strategies on the system performance indicators under different level of rework rate. Besides, the interaction of order release and dispatching strategies under different rework operations will be investigated. Some representative SFC strategies are considered in this simulation model. This project has found the effect of rework operation on the system performance is significant. The order release and dispatching strategies' performance will be affected by the rework operation. The performance will be improved dramatically if the suitable combination of order release and dispatching strategies are adopted. Under different rework rate and performance indicators the suitable combination of SFC strategy are suggested in this project.

The second experiment is concerned with the interaction among shop floor control (SFC) strategies (order review/release, dispatching, and rework rules) and its impact on the performance of wafer fabrication. It tried to find the better combination of these rules by specific performance indicators. From the results of simulations and statistic analysis, the performance of most ORR rules will be improved when combined with suitable dispatching and rework strategies. But no single strategy can satisfy all performance indicators. In practice, SFC strategies should be chosen carefully based on the system conditions. Furthermore, ORR, dispatching, and rework strategies cannot be separately considered. Instead, they should be combined and integrated for improving the system performance. The suitable combinations of SFC (Shop Floor Control) strategies for different performance indicators are suggested in this project.

Due date assignment (DDA) is the first important task of shop floor control in wafer fabrication. Due date related performance is impacted by the quality of the DDA rules. Assigning order due dates and timely delivering the goods to the customer will enhance customer service and competitive advantage. A new methodology for lead-time prediction, artificial neural network (ANN) prediction is considered in the third experiment. An ANN_Based DDA rule combined with simulation technology and statistical analysis is developed. Besides, Reg_Based DDA rules for wafer fabrication are modeled as benchmarking. Whether neural networks can outperform

conventional and Reg_Based DDA rules taken from the literature is examined. From the simulation and statistical results, ANN_Based DDA rules perform a better job in due date prediction. ANN_Based DDA rules have a smaller tardiness rate than the other rules. ANN_Based DDA rules have better sensitivity and variance than the other rules. Therefore, if the wafer fab information is not difficult to obtain, the ANN_Based DDA rule can perform better due date prediction. The SFM_Sep and JIQ in Reg_Based and conventional rules are better than the others.

Owing to the interactions between the DDA and SFC rules order review/release and dispatching are significant. In the fourth experiment, the ANN_Based DDA rules will be discussed under different SFC rules in the simulation model. It is very important to determine a suitable DDA rule under various ORR combinations and dispatching rules. From the simulation and statistical results, ANN_Based DDA rules perform better in due date prediction. ANN_Based DDA rules have a smaller tardiness rate than the other rules. ANN_Based DDA rules have better sensitivity and variance. This project provides suggestions for DDA rules under various SFC rule combinations. ANN_Sep is suitable for most of these combinations, especially when ORR, WR and TB, rules are adopted.

Keywords: *wafer fabrication plants, shop floor control, due date assignment, order review/release, dispatching, rework, artificial neural network*

目　　錄

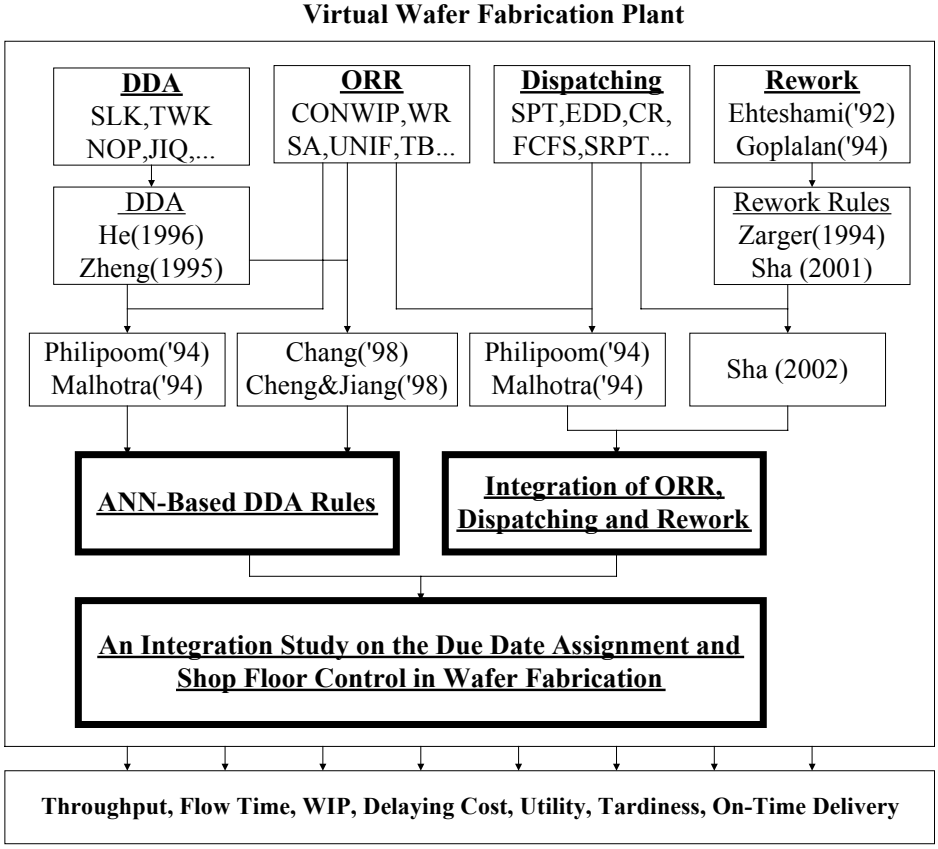
一、前言

半導體產業為台灣的關鍵發展產業之一，晶圓製造更為半導體產業的核心。然而由於晶圓製造的複雜性與其生產流程的再回流性(reentry)，使其生產系統的現場管控十分困難，過去便有許多學者投入心力在晶圓廠現場控制策略的研究上。然而多數的研究多僅侷限在單獨探討投料或派工法則，以發展合適的投料或派工法則為主要目的。然而由於晶圓廠生產系統的高度複雜性與投料、派工法則間明顯存在之交互作用，使得過去許多研究成果多僅達到局部最佳化，當系統環境發生變化或進行其他現場控制策略調整時，系統績效將明顯受到影響。因此現場控制策略實應進行整合性的探討。另外，由於晶圓單價甚高，因此線上即時進行不良品的重工以降低晶圓報廢的成本，便顯得十分迫切。過去生產控制策略的研究卻多忽略不良品重工的需求，因此在本計畫在進行晶圓廠生產控制策略整合性研究時，亦將重工的需求與重工的控制策略納入一併考量。

另外，過去晶圓廠現場控制策略的研究多僅重視系統內相關績效，而忽略交期相關績效。然而由於近來來全球運籌與供應鏈的推動，客戶對訂單準時達交的要求日益殷切，因此如何決定合適的訂單交期，有效提升生產系統交期相關績效便顯得十分重要。因此本計畫除進行投料、派工及重工策略間之整合性研究外，更將嘗試以類神經網路為基礎並結合電腦模擬與統計分析等技術構建「以類神經網路為基礎之交期指派法則」，希望能提高交期指派的品質，並進而探討在各種不統現場控制策略邏輯下，各類交期指派法則之適用性，提出可有效改善交期相關績效指標之生產控制策略整合建議。

二、研究目的

半導體業是台灣重點產業之一，晶圓製造更是半導體業之製程關鍵所在，然而由於晶圓製造製程之繁複與其特殊之再回溯性（reentry），使得其生產系統之控制十分複雜，因此晶圓廠生產系統之現場控制策略，包括:交期指派（DDA, due date assignment）、投料（ORR, order review and release）、派工（dispatching）等均是學者研究之重心所在。然而，相關研究多僅單獨探討上述主題，整合性的研究普遍缺乏（如圖一）。研究重點多在假設其他控制策略固定不變的前提下，發展特定策略之新方法（例如：研究投料的學者多在忽視交期相關績效並固定現場派工的邏輯為簡單的先進先出（FIFO）的環境下，發展新的投料法則。），研究成果多僅能達到局部最適化，當系統環境發生變動，或生產現場其他控制策略（採用其他派工法則）改變時，系統績效便普遍不如預期；另外晶圓廠製程為提高製程良率，針對不良品多需進行重工（rework），此類需求在現場控制策略研究中也多被忽略，當生產系統發生不良需進行重工時，相關研究所建構之生產控制策略可能喪失其適用性。



圖一 研究問題定位

因此本研究將考量現場重工的需求，將可行的重工策略納入，並結合投料、派工等進行生產系統現場控制策略之整合性研究。另外，隨著供應鍊與全球運籌管理觀念的興起，準時交貨逐漸成為客戶要求的重點，交期相關績效指標逐漸受到重視，如何在接單時能決定合適的訂單交期，並有效提高生產系統的達交率已成為現場管理的另一重點。因此本研究亦將交期指派策略納入，除嘗試結合類神經網路、統計分析與電腦模擬技術發展以類神經網路為基礎的交期指派法則(ANN-Based DDA rules)外，並納入許多業界及學者常用的交期指派法則，在各種不同現場控制策略環境下進行模擬驗證，期能進一步探討不同現場控制策略組合對交期相關績效的影響？整體而言，本研究嘗試探討的問題包括：

1. 生產系統之不良品重工需求對系統績效與現場控制策略的影響？
2. 探討現場控制策略（投料、派工及重工策略）之交互影響？及嘗試提出在特定績效指標下之最適策略組合。
3. 構建以類神經網路為基礎之交期指派法則，並探討在不同現場控制策略下各類交期指派法則之績效表現？
4. 如何選用合適的現場控制策略組合已改善交期相關績效？

三、文獻探討

晶圓製造廠的生產規劃與排程作業由於製程的複雜性、產品及生產技術的快速汰換更新、重加工（rework）與良率的隨機性(random yield)等特性而存在許多不易克服的問題（Uzsoy and Martin-Vega, 1992）。因此在生產規劃與排程問題的研究方面，便有很多學者投入進行研究，希望尋找可行的生產策略，在生產成本最小化的前提下，提高產出率、產量、機器利用率，並改善品質與運送效率。此類型的問題包括：交期指派（due-date assignment）、投料法則（ORR）、微影黃光區排程(dispatching)、批量排程(batch scheduling)、重加工（rework）等多是學者熱衷研究的主題。

然而，經本研究小組初步進行之文獻探討發現：就現有之研究成果來看，早期研究多傾向於單獨探討上述問題，以發展或修正相關決策法則來提昇生產績效為主要研究方向，近十年來才陸續有許多學者針對問題進行策略組合與交互作用的研究。以下便分別說明各類問題的相關研究狀況：

（一）投料法則

在投料法則方面，為決定投料生產的時機與數量，除了許多學者致力建構最佳化之數學模式外，由於生產系統之複雜度過高，近來之研究多傾向啟發式解法的發展與建構，包括 Wein(1988)、Glassary & Resende(1988)、Melynk&Ragatz(1989)、Spearmand（1990）、Goldratt(1990)、Yan(1992) 等學者。現有發展的投料法則包括：CONWIP（constant work-in-process）、WR(workload regulating)、SA(starvation avoidance)、UNIF(uniform)、DBR（drum buffer rope）、TB（two-boundary）等，Kim 等(1998)則針對 WR 法則修正後提出 PWR（parametric workload regulating）。相關研究的重心多在利用各種生產效率衡量的指標來評估投料法則之優劣，評估時多將現場排程派工法則予以簡化（多數假設為 FIFO）。

（二）排程派工

晶圓廠的排程方面，由於晶圓加工必須利用微影製程將許多層的電路建立在晶圓上，因此每片晶圓在加工過程中必須一再進入微影黃光區。因此晶圓廠的排程研究方面，有許多學者特別針對微影黃光區之排程方法進行探討，以提高整體生產績效。較傳統的排程方法包括：SPT(shortest process time）、EDD(earliest due date)、CR(critical ratio)、FCFS（first come first service）、SRPT(shortest remaining processing time)等，根據 Glassary & Resende(1988)利用系統模擬研究發現 SRPT 的表現狀況較佳。除此之外，Kim 等(1998)曾提出針對加工循環（loop）之加工負荷水準加以考量的 LWL（loop workload leveling）法則。另外除了微影黃光區外的製程，如氧化、薄膜沈積、蝕刻、擴散、離子植入及清洗等可以進行批量處理的製程，則有許多學者針對批量排程（batch scheduling）進行研究，批量排程通常包括批量決定與排程派工兩個問題。關於批量訂定方面 Uzsoy 等(1994)指出 MBS（minimum batch size）最常被應用，亦即當等候批量累積數大於預設值時便開始生產。在批量處理的排程派工方面，除 FCFS 等通用的派工法則外，Kim(1998)利用 SA 法的精神提出 BFQL（Back and Front queues

leveling）的派工法則，以提昇整體效率。

（三）交期指派

過去晶圓廠生產控制的研究多以產出率、在製品與流程時間等作為生產績效衡量指標，但隨著供應鍊與全球運籌管理觀念的興起，準時交貨逐漸成為客戶要求的重點。因此，生產系統延遲（lateness）或延誤（tardiness）等指標逐漸成為要求重點，亦即必須提高完工時間與交期之一致性，避免因延後完工產生客訴及商譽的損失或因提前完工造成存貨堆積與配送成本的額外負擔等（Cheng&Jiang,1998）。而此類與交期相關的績效指標除將受投料與派工策略的影響外，交期的擬訂更是直接影響其績效表現的關鍵因素，故應將交期指派納入生產控制策略一併考量。

交期指派的研究方面，學者的研究多以考量工件特徵（如總加工時間、作業項目、生產數量等）等靜態資訊與生產系統狀態（系統工件數、工作站等候工件數等）等動態資訊為主，提出的交期指派法則中，僅考量靜態資訊的以 CON、RAN、TWK、NOP、SLK 等為主，考量動態與靜態資訊的法則則包括：JIQ、JIS、OFS、COFS 等(Chang, 1996)，綜觀所有法則其精神多在於依據工件到達時間與工件生產前置時間（包括：等待投料時間與實際加工總工時）以預估完工時間並決定交期。預測與估算的方法則包括：電腦模擬法、迴歸分析法與直接估計法。

關於晶圓廠的交期指派方面，由於晶圓廠的製程較為複雜，交期的決定牽涉甚廣，因此過去的研究多以傳統零工型環境為主，近來則有許多學者嘗試利用迴歸分析與電腦模擬等技巧，透過流程時間的估算來決定交期，何氏（1997）便嘗試利用階段迴歸分析法來預測晶圓製造廠的流程時間以決定交期，但迴歸分析法的績效常受限於納入考量的變數，但納入變數過多則相對提高問題的複雜性與演算推導的困難，因此實務應用上實有其困難。而鄭氏（1996）基於晶圓製造廠之交期考量需將投料、派工及系統的穩定性納入，因此發展的交期指派模式便將系統產能、現場在製品量及投料等因素納入，利用模擬工具估算流程時間與投料時點，進而決定各訂單批之交期。然而，該模式運作費時並忽略了派工法則將影響流程時間的事實將可能造成估算的偏誤。而 Philipoom 等 (1994) 與 Mamalis&Malagardis(1996)曾分別利用類神經網路（Neural Network）與模擬退火法（Simulated Annealing）的方法來估算典型零工式生產環境的流程時間以決定交期，彌補數學模式與電腦模擬耗時與計算困難的缺點。沙氏與許氏(2002c)便曾嘗試利用類神經網路來進行晶圓製造廠流程時間的估算，並將投料、派工甚至重加工策略納入考量，以提昇流程時間估算的準確性以決定合適的訂單交期。但其假設交期係由公司決定（internally set due date），未考量實際客戶需求為其不足之處。多數環境交期係由下單客戶與公司業務或生產管制人員所協商決定的。另外，未考量其他現場控制策略對交期的影響為其交期預測模式另一需再強化之處。

（四）部份整合性研究

Glassary & Resende(1988)發現晶圓廠排程的問題雖並不如投料控制那樣重要，但在其模擬研究中發現排程法則的好壞將明顯影響生產系統在在

製品、流程時間與產出率的表現。因此陸續有許多學者將晶圓廠排程法則的問題併入投料法則一同討論，希望能找出投料法則與排程派工法則間之最佳組合，如：Philipoom(1993)針對 PBB、MIL 及 IMM 三種投料法則與 SPT、CR 兩種派工法則之組合進行模擬研究，並針對各種績效衡量指標進行評估。Malhotra 等（1994）則針對常用之兩種投料法則與五種派工法則進行模擬研究。然而，上述研究的對象多僅針對零工式（job shop）生產的環境來進行，並未特別針對晶圓廠來模擬。Kim 等（1998）則特別針對晶圓廠進行模擬研究，該研究納入的包括：五種投料法則與五種排程派工法則進行整合性的模擬研究。並分別針對在製品、流程時間、產出率等進行衡量。

考量交期的部份整合性研究方面，Chang(1996)、Chang(1998)、Cheng&Jiang(1998)分別針對交期指派與派工法則進行整合評估，其中以 Cheng&Jiang 整合五種派工法則與四種交期指派法則較為完整。而 Liao(1998)除考慮此兩因素外，更進而將人員指派的策略因素納入，在雙重限制資源（設備與人員）限制下，整合派工、交期指派與人員指派法則以提昇整體效益。另外 Tsai（1997）考慮生產控制策略之交互影響故考量三種交期指派模式、三種投料法則與三種排程派工法則針對典型零工式生產環境進行整合研究。研究發現，整合交期指派模式與投料法則不僅提昇了流程時間估算的準確性，交期的達成績效也提高了。因此，本計畫擬針對晶圓製造廠進行生產控制策略組合之整合性研究。

（五）重加工

晶圓加工由於十分重視產出率，故對於製程中（微影黃光區）發生之不良品多未立即加以妥善處理（進行重加工）；以往學者所發展的投料與排程派工法則多忽略不良品的問題，當生產系統產生不良品需進行重加工時，整體生產績效便不如預期理想。根據 Zarger（1995）的研究指出，重加工雖將使生產系統的週期時間增長，但重加工將使生產系統產出的耗損降低。因此實有必要將重加工的策略納入晶圓製造生產系統的研究中，以符合晶圓製造之實際需要。重加工的研究方面，過去多偏向利用數學模式來進行探討，如 Gopalan&Kannan（1994,1995）、Ehteshami et al.（1992）、Liu&Yang（1996）等學者，然而此類的研究多僅將重加工納入考量，以探討包括瓶頸資源管理、製程規畫與批量訂定的策略，並未實際針對重加工的策略進行探討。直到 1995 年 Zarger 方提出晶圓廠微影黃光區重加工之四種策略，並利用等候線模式分析四種策略對製程週期時間的影響。陳氏（1998）則以 Zarger 的四種重加工策略為基礎發展第五種重加工策略，並利用電腦模擬與統計檢定的技巧，來驗證重加工策略對生產績效的貢獻。

（六）考慮重加工的部份整合性研究

經過上述文獻探討得知，投料與派工的決策對晶圓製造效率有很大的影響，投料與派工之部份整合型研究也提出較佳策略組合之建議，但忽略重加工的投料派工策略組合將使生產控制策略之最佳化優勢在現場發生重加工需求時被影響，進而直接影響生產效率。因此，本研究計畫主持人（沙氏等，2002）便利用模擬方法針對五種重加工策略與黃光區常用的排程派工法則進行研究，以找出重加工策略與派工策略間之交互關係，以供重加

工策略擬訂的參考。

整合上述所有相關文獻，為進一步考量納入交期指派法則、投料法則、派工法則與重加工法則以達到生產控制策略之全面性整合，本研究計畫除將進行各類現場控制策略的整合性研究外，更將利用類神經網路構建整合性交期預測模式外，提高交其生產系統交期預測能力，以利整合現場管理相關決策，提升管理效能，有效提升交期相關績效的表現，強化整體競爭力。

四、 研究方法

本研究屬實證性研究，除將發展以類神經網路為基礎之交期指派法則外，並將進行包括現場投料、派工、重工及交期指派等各類管理策略之整合性探討，期能提出整合性現場控制策略建議，有效改善晶圓廠整體績效。但由於在實際晶圓廠進行實證研究之成本過高且費時，因此本研究嘗試利用物件導向模擬軟體構建虛擬晶圓廠，並在虛擬晶圓廠上整合驗證各類型之現場控制策略，再利用統計軟體進行分析。在交期指派法則方面，則採用類神經網路、模擬軟體與統計分析等技巧來構建，分述如下：

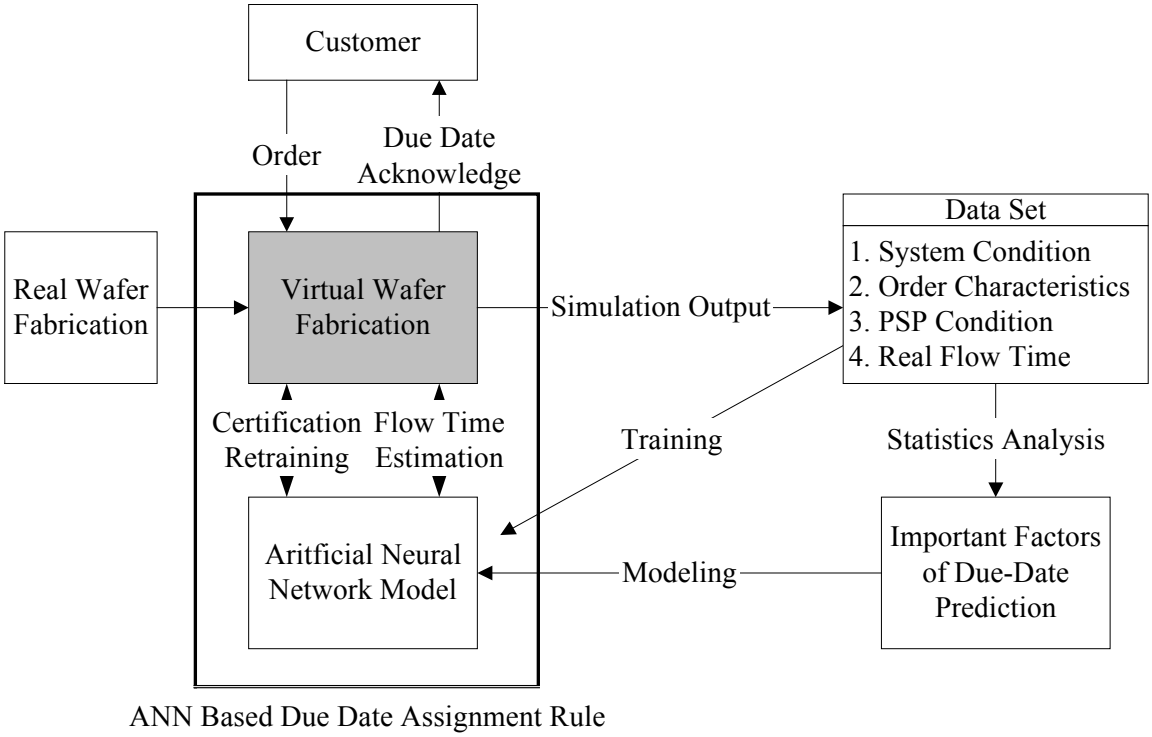
（一）虛擬晶圓廠之構建

電腦模擬的技巧過去便經常利用在晶圓廠現場控制策略的驗證上，但過去受限於電腦速度與軟體，多以簡化的模擬模式來進行，過度簡化的結果，常無法完整蒐集各類資訊以進行完整的分析。因此，本研究嘗試以新竹科學園區某實際晶圓廠為對象，透過物件導向模擬軟體 eM-Plant 來進行虛擬晶圓廠之構建。除將納入所有晶圓廠之機台外，更透過實際資料的統計分析來構建包括產品途程、加工時間、當機週期與修復時間等系統隨機行為模式，期使構建之虛擬晶圓廠能具代表性，進而確保後續驗證研究結果之可信性。

本研究構建之虛擬晶圓廠共包括 53 個工作站，共 301 台相關生產設備，廠內主要生產三種產品，產品組合分為：0.2、0.35 及 0.45，各產品層數為 16、17、及 18 層；加工時間則依據過去記錄採平均值±5%之均勻分配來預估，當機週期時間與修復時間以指數分配來估計；每一批共有二十四片晶圓放在同一晶舟上，加工之進行以晶舟為單位。

（二）以類神經網路為基礎之交期指派法則之構建

本研究構建之交期指派法則主要結合以類神經網路為基礎，並結合電腦模擬與統計分析等技巧，運作模式如圖二所示。以類神經網路為基礎的交期指派法則主要以本研究構建之虛擬晶圓廠為基礎，蒐集模擬產生之大量資料（包括：實際流程時間及涵蓋系統況狀、訂單特徵及投料前等候區狀況等三大類共九十二種交期相關預測因子之實際資訊），透過統計分析的技巧加以過濾篩選後，以關鍵性因子來構建類神經網路之 BPN 模式，並進行測試與修正；接著再將測試完成之 BPN 模式與原有之虛擬晶圓廠結合。當客戶提出新訂單需求的同時，系統便可蒐集當時相關預測因子之數據，透過 BPN 模式預測訂單可能完工時間，進而決定交期。



圖二 以類神經網路為基礎之交期指派法則運作模式

（三）實驗設計與統計分析

本研究以虛擬晶圓廠為基礎，進行四個主要的模擬實驗。說明如下：

實驗一探討不良品重工需求對晶圓廠現場控制策略的影響。主要納入的現場控制策略包括：七種投料法則及八種派工法則，均已實務上經常應用且具代表性的法則為限。透過模擬驗證探討在不同程度的不良品重工需求（1%-10%）下，各項績效指標之表現狀況。

實驗二以探討投料、派工、及重工等三種現場控制策略間之關係為核心，探討不同策略組合對晶圓廠系統績效的影響，嘗試發現各類績效合適之現場控制策略組合。

實驗三則驗證本研究發展之交期指派法則為主，實驗納入三類共九種交期指派法則，包括業界經常使用的三種通用性法則（TWK、JIQ、JIBQ）、四種學者常用的以迴歸為基礎之交期指派法則(KFM_Sep、KFM_Com、SFM_Sep、SFM_Com)及以類神經網路為基礎之法則（ANN_Sep、ANN_Com）等，在此投料、派工及重工法則分別採用 UNIF、FIFO 及 Lock-Step 等實務上通用法則。

實驗四則將探討不同投料及派工法則下，各類交期指派法則的績效表現狀況。納入的投料與派工、重工法則主要以實驗一、二之結果為基礎加以篩選，納入三種投料法則（UNIF、WR、TB）、六種派工法則（FIFO、EDD、CR、SRPT、COVERT、TB＋），重工法則則採用績效表現最佳的

Lock_Step。交期指派法則亦透過實驗三的結果加以篩選，共計納入包括：JIQ、TWK、ANN_Sep、ANN_Com、Reg_Sep 及 Reg_Com 等六種。

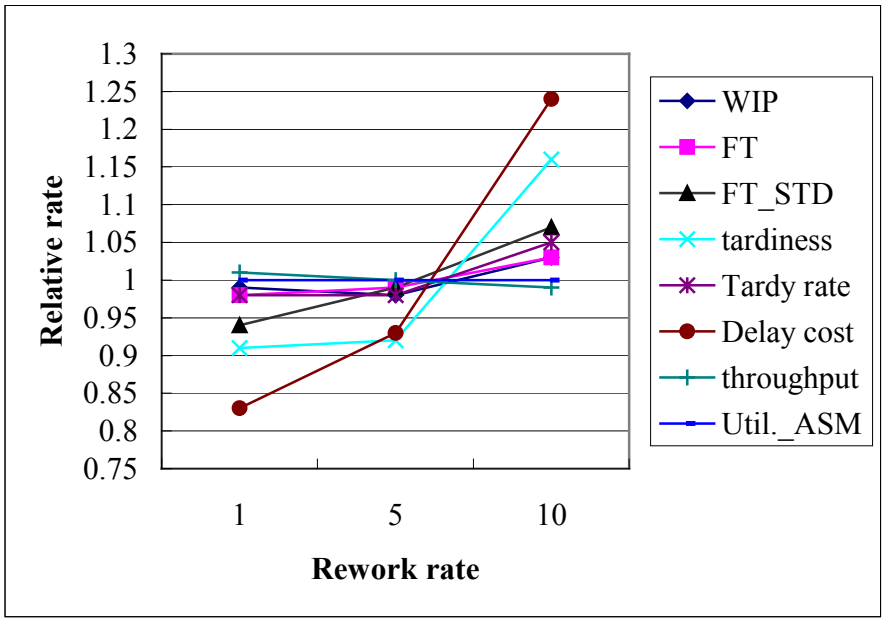
各模擬實驗在不同隨機亂樹下重複進行六次，每次隨機抽取（抽取率10%）3000 批的完工批量進行資訊蒐集，再利用統計軟體 SPSS 進行統計檢定與分析。績效指標方面包括流程時間（FT）、流程時間標準差（FT_STD）、在製品（WIP）、延遲時間（tardiness）、遲延時間（lateness）、延遲比率（% of lateness）、延遲成本（Delaying Cost）、達交率（% of on time）等均納入討論。

五、 結果與討論

本研究主要結果可分為四部分說明如下：

（一）良品重工對生產系統的影響

當生產系統發生不良品需進行重工作業時，對系統績效難免將造成影響，但為提高生產系統的良率，降低不良品廢棄的成本，適度進行重工實有其必要。由實驗一的研究結果發現，隨著重工率的提高系統績效有明顯惡化的跡象，但若重工率低於 5 % 則系統績效表現顯得較為穩定，因此可發現適度重工並不會嚴重影響系統績效。另外在重工需求與不同投料、派工法則的交互影響方面，研究結果發現若系統採用負荷導向型（load oriented）現場控制策略（如：WR、TB），有效掌控系統負荷，則系統績效明顯較不受重工需求的影響。



圖三 不良品重工對系統績效的影響

（二）投料、派工及重加工策略之整合性分析

由實驗二之研究結果發現，投料、派工及重工策略間之交互作用十分明顯，因此適當的策略組合搭配將可有效改善系統相關績效（如表一）。投料法則 TB 若能適度搭配 SRPT 及 Lot-split，則其 WIP 可由 620 下降至 417，FT 則可由 38.69 天縮短到 27.33 天）。

研究發現生產系統在考量各類現場控制策略時，實不應分開考量。傳統投料時點由生產計畫單位來決定，派工與重工則由現場人員負責，分開考量的結果通常無法有效改善整體績效。因此本研究嘗試整理出各績效指標下較合適的策略組合建議（如表二），明顯發現不同策略組合將明顯影響系統績效。因此生產系統控制策略之決策應進行整合性的考量考量，以有效改善系統績效。

表一 投料、派工及重工策略組合之系統績效改進效益分析

Strategy	WIP	FT	FT_STD	Tardiness	Tardy Rate	Delaying Cost
TB	620	38.69	7.36	1.97	0.22	45.30
TB*SRPT	441	28.88	7.46	0.10	0.02	18.82
TB*SRPT*Lot-split	417	27.33	7.54	0.11	0.03	20.68
TB	620	38.69	7.36	1.97	0.22	45.30
TB*EDD	455	29.46	6.70	0.08	0.02	18.04
TB* EDD*rendezvous	457	29.38	6.36	0.03	0.01	17.6
SA	938	56.62	17.58	13.37	0.64	579.85
SA*NexQL	796	48.2	17.04	7.90	0.42	282.01
SA* NexQL*Lot-split	639	39.84	13.12	2.75	0.23	75.52
WR	601	38.91	8.15	1.15	0.10	64.91
WR*EDD	520	34.01	4.37	0.08	0.02	13.48
WR*EDD*Lock-step	516	33.52	1.46	0.03	0.01	13.59

表二 生產現場控制策略組合建議

WIP		FT		FT_STD	Tardiness		Tardy Rate		Delaying Cost	
652[2]	(417[3])	652	(27.33)	161	(45.09,1.46[4])	622	(0.03)	622	(0.01)	161	(1.80)
653	(431)	682	(28.30)	163	(45.11,1.47)	641	(0.03)	641	(0.01)	231	(1.82)
682	(446)	653	(28.42)	131	(45.10,1.50)	682	(0.03)	682	(0.01)	163	(1.87)
621	(452)	622	(29.27)	133	(45.10,1.60)	122	(0.04)	122	(0.01)	131	(1.95)
622	(457)	623	(29.38)	231	(46.33,1.87)	161	(0.04)	623	(0.01)	133	(2.14)
623	(457)	621	(29.74)	661	(46.07,1.91)	623	(0.04)	652	(0.03)	661	(2.29)
651	(475)	651	(30.89)	233	(46.52,2.03)	163	(0.07)	621	(0.03)	233	(2.34)
642	(496)	642	(30.90)	263	(46.74,2.30)	131	(0.08)	653	(0.03)	261	(3.90)
671	(501)	643	(31.91)	261	(46.82,2.35)	133	(0.10)	161	(0.03)	162	(4.04)
122	(504)	122	(32.92)	633	(46.59,2.56)	652	(0.11)	123	(0.03)	132	(4.41)
643	(513)	641	(33.35)	162	(44.60,3.15)	621	(0.16)	651	(0.04)	263	(4.64)
121	(516)	671	(33.35)	631	(47.40,3.24)	123	(0.16)	671	(0.04)	633	(4.88)
		121	(33.52)	111	(43.46,3.40)	651	(0.17)	163	(0.05)	111	(5.76)
				132	(44.33,3.42)	653	(0.21)	642	(0.05)	113	(6.35)
				113	(43.24,3.62)	671	(0.26)	131	(0.05)	112	(6.75)
				663	(47.50,3.65)	642	(0.29)	141	(0.06)	662	(9.88)
				112	(43.63,3.74)	132	(0.31)	133	(0.06)	631	(12.66)
				662	(46.19,3.87)	162	(0.32)	643	(0.07)	123	(12.74)
				232	(47.33,4.12)	231	(0.33)	142	(0.08)	641	(13.59)
				641	(33.35,4.14)	661	(0.33)	143	(0.08)	232	(13.66)
avg.	822[5]	49.68		13.24	8.08		0.48		324.63	

1.the α of Duncan's Test is 0.01

2.the first number is ORR strategy (1:WR, 2:CONWIP, 3:SA, 4:UNIF, 5:POISS, 6:TB, 7:WCEDD), second number is dispatch strategy (1:FIFO, 2:EDD, 3:CR, 4:NexQL, 5:SRPT, 6:COVERT, 7:SA+, 8:TB+), and the third number is rework strategy (1:Lock-step, 2:Lot-split, 3:Rendezvous)

3.mean value of the performance indicators

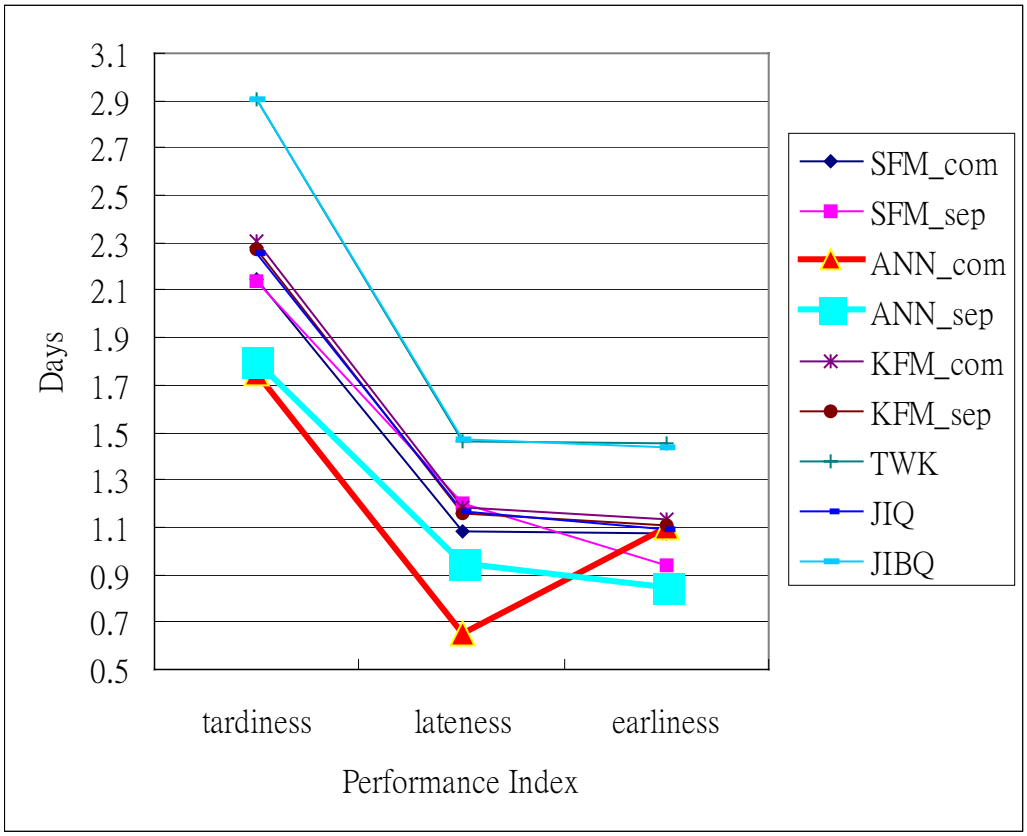
4.the mean and standard derivation of flow time

5.the mean of the total combination of SFC

（三）以類神經網路為基礎之交期指派法則

由實驗三的模擬結果發現，以類神經網路為基礎的交期指派法則明顯優於其他兩類交期指派法則（如圖四）。不管在延遲時間（tardiness）、遲延時間（lateness）及提前完工時間（earliness）等三種績效指標上皆相同。傳統通用式法則明顯最差，以迴歸為基礎的交期指派法則則次之。

因此本研究建議若生產系統中相關資訊的取得並不困難，則建議透過類神經網路來預測系統完工時間，以協助決定合適的交期。目前晶圓廠電腦化程度普遍十分深入，即時系統資訊的蒐集通常並不困難，因此構建以類神經網路為基礎之交期指派法則應可以充分應用在一般晶圓廠，以改善交期指派的品質，提升客戶滿意度。



圖四　各類交期指派法則之績效分析

（四）各類交期指派法則與現場控制策略之整合性探討

不同現場控制策略將直接影響工件流程時間，間接影響訂單之達交與否？因此交期指派的良窳將受現場採用之投料與派工法則的影響。此推論透過實驗四的結果將可得到驗證。

如表三所示，不同投料與派工法則下，各類交期指派法則的績效表現在 Duncan's test 下明顯存在差異，不同策略組合將有明顯較合適的交期指派法則，亦即考量系統管控需求，在採用特定投料、派工法則的狀況下，

應選用合適的交期指派方式，以改善交期相關的績效表現。表四便依據統計分析結果提出交期指派法則之建議。

表三 交期指派法則在不同投料、派工組合下之績效分析(Duncan's test)

Rule	Lateness	Tardiness	Earliness
WR*FIFO	3 1 6 4 2 5[2]	3 1 6 4 2 5	5 3 2 1 6 4
WR*EDD	1 3 6 4 2 5	1 3 4 6 2 5	5 3 1 6 2 4
WR*CR	3 6 1 2 4 5	3 2 6 1 4 5	3 6 1 2 4 5
WR*SRPT	4 3 1 6 2 5	4 6 3 1 2 5	1 5 4 3 2 6
WR*COVERT	3 6 1 2 4 5	3 2 1 6 4 5	3 6 1 2 4 5
UNIF*FIFO	3 1 6 4 2 5	3 1 6 4 2 5	3 1 4 6 2 5
UNIF*EDD	1 3 6 4 2 5	3 1 4 2 6 5	5 1 6 3 4 2
UNIF*CR	3 6 1 4 2 5	3 1 4 2 6 5	6 3 1 4 2 5
UNIF*SRPT	1 3 4 6 5 2	3 6 4 1 5 2	5 1 4 6 3 2
UNIF*COVERT	3 1 4 6 2 5	3 1 4 2 6 5	3 1 2 6 4 5
TB*FIFO	1 3 6 2 4 5	1 6 3 4 2 5	1 3 5 6 2 4
TB*EDD	3 1 4 6 2 5	3 1 4 6 5 2	5 1 3 4 2 6
TB*CR	1 3 6 2 4 5	1 3 4 2 6 5	1 6 3 2 4 5
TB*SRPT	3 1 2 6 4 5	3 2 1 6 4 5	3 2 1 5 6 4
TB*COVERT	3 6 2 4 1 5	1 3 2 4 6 5	3 6 2 4 1 5
TB*TB+	3 1 6 2 4 5	2 4 6 1 3 5	5 3 1 6 4 2

1. the α of Duncan's test is 0.01
2. the number is represent the rule of DDA(1:Reg-Sep, 2:JIQ, 3:ANN-Sep, 4:ANN-All, 5:Reg-All, 6:TWK)

表四 交期指派法則建議表

Rule	JIQ	Reg_Sep	Reg_Com	ANN_Sep	ANN_Com	TWK
WR*FIFO				◎		
WR*EDD		◎				
WR*CR				◎		
WR*SRPT					◎	
WR*COVERT				◎		
UNIF*FIFO				◎		
UNIF*EDD		◎				
UNIF*CR				◎		
UNIF*SRPT		◎		◎		
UNIF*COVERT				◎		
TB*FIFO		◎				
TB*EDD				◎		
TB*CR		◎				
TB*SRPT				◎		
TB*COVERT		◎		◎		
TB*TB+				◎		

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七、 計畫成果自評

本研究主要成果條列說明如下：

1.確認不良品重工對生產系統績效的影響，並提出在重工作業下，投料、及派工策略之建議。

不良品的線上即時重工的主要目的在於提高生產系統良率及降低不良品廢棄成本，尤其針對晶圓製造廠微影黃光區的製程更為迫切。本研究發現不良品重工的機會越高，系統績效將隨之惡化，但若重工率控制在百分之五以內，則系統績效可維持穩定（並未明顯惡化）。亦即適度進行不良品重工（5%以內）並不明顯影響系統績效。此發現可修正過去忽視重工或多另設維修站離線維修，甚直接丟棄不良品的錯誤決策。

另外，當系統現場控制策略採用類似 TB、WR 等負荷導向控制策略時，不良品重工對系統績效的影響更不明顯。因此若系統現場投料及派工均採用以嚴密監控系統負荷為基礎之負荷導向型策略，則將可有效降低不良品重工對系統績效的影響。

2.確認生產現場控制策略整合規劃之重要性與必要性，並提出投料、派工及重工策略之組合建議。

本研究透過模擬驗證的方式來進行晶圓製造現場生產控制策略之整合性研究，研究結果發現當適度選擇合適的投料、派工及重工法則加以組合後，將可有效提升各類系統績效達 30%以上。亦即合適的策略組合將可確保系統績效。研究中並進一步透過統計檢定分析的方式(Duncan's test)，提出合適的策略組合建議，其發現與建議頗具實用價值。

3.構建之「以類神經網路為基礎之交期指派法則」明顯提升交期預測績效

過去實務界預測交期多以直覺式法則（conventional rule）為主，學者的研究亦多傾向以線性迴歸為基礎來構建交期預測模式。本研究嘗試以類神經網路為基礎，結合電腦模擬與統計分析技術，針對製程複雜且流程冗長、不穩定性甚高的晶圓製造廠，構建「以類神經網路為基礎的交期指派法則」，經模擬驗證發現，以類神經網路為基礎的交期指派法則對交期預測的品質明顯明顯優於「直覺式法則」及「以迴歸為基礎的交期預測模式」。因此，若系統即時資訊蒐集並不困難（視生產現場控制資訊化程度而定），則建議採用本研究發展的交期預測模式決定交期。由於晶圓廠生產流程管控電腦化程度都具有一定的水準，因此在應用此交期預測模式上應無多大的障礙。

4.確認現場控制策略對各類交期指派法則績效的影響，並提出不同現場控制策略組合下之交期指派法則建議。

交期績效的好壞取決於生產流程時間的變異狀況，生產流程時間則直接受取決於生產流程時間的變異狀況，生產流程時間則直接受現場控制策略（投料及派工）的影響，因此欲提高生產系統產品之達交率，除選用合適的交期預測工具外，現場控制策略的影響不能忽視。本研究進一步將各類交期指派法則納入現場控制策略之整合性研究中，不但發現不同現場控制策略對各類交期指派法則績效的影響十分明顯，更進而透過統計分析提

出針對不同現場控制策略組合下，合適的交期指派法則建議。未來業界可以此成果為基礎，審慎進行包括交期指派、投料及派工等現場控制策略之整合規劃。

本研究屬實證性的研究，雖因考量驗證成本而未直接在實際晶圓廠進行驗證，改以電腦模擬方式來進行，但由於研究中採用先進的物件導向模擬軟體（eM-Plant）來構建虛擬晶圓廠，且以實際晶圓廠為基礎， 不但將廠內所有使用中機台納入，並透過長期歷史資料統計分析，構建系統中之隨機性行為（如：加工時間、當機週期與修復時間等）。因此其驗證成果較之過去僅以數個工作站簡單模擬晶圓廠的學術性研究而言，應頗具實務參考價值。

在研究成果的實務應用方面，傳統交期的決定、訂單投料與現場派工、重工，多採分工的方式進行，其中交期多由業務部門主導，訂單之投料時點與數量則由生產計畫或管理部門，透過工令來進行投料控制；派工及不良品重工則多由現場生產管制人員，甚至直接交由操作人員來決定，獨立進行決策的結果往往無法有效提升系統整體績效，甚至有相互抵銷與矛盾的現象。若生產系統的現場管理能打破過去專業分工的限制，利用本系統整合性規劃策略組合的相關建議，適度規劃合適的投料、派工及重工策略組合，應可大幅改善系統整體績效，並提高系統穩定度，簡化現場管理的複雜度。

另外，訂單交期的決策方面，過去多透過業務部門與生產管理部門的溝通與角力來完成。由於雙方立場不同，合適的交期多無法順利產生，缺乏穩定且可信的預測工具成為交期品質的致命傷。若能嘗試構建本研究提出之「以類神經網路為基礎之交期指派法則」，充分應用類神經網路在預測上的穩定性與可信性，及虛擬晶圓廠電腦模擬的即時性，應可充分改善現有交期決策的問題，有效提升交期預測的品質。

此外，在學術研究方面，本計畫的部分成果已分別於 2002 年中華民國工業工程年會及 2003 年 Proceedings of the Seventh Conference on Artificial Intelligence and Application 等研討會上發表；研究計畫成果之主要內容經整理投稿後也已獲得三個國際知名期刊接受並將加以刊載，列述如下：

1. D. Y. Sha, Sheng-Yuan Hsu, 2002.11,"The effects of Rework on the Shop Floor Control in Wafer Fabrication", ***Integrated Manufacturing Systems***, (Accepted) (EI)
2. D. Y. Sha, Sheng-Yuan Hsu, 2002.12,"Due Date Assignment in Wafer Fabrication Using Artificial Neural Networks", ***International Journal of Advanced Manufacturing Technology***, (Accepted) (SCI, EI)
3. D. Y. Sha, Chao-Yang Liu, 2002.9," A simulated annealing algorithm for integration of shop floor control strategies in semiconductor wafer fabrication ," ***International Journal of Advanced Manufacturing Technology*****,** (Accepted) (SCI, EI)
4. D. Y. Sha, Sheng-Yuan Hsu, 2003. 6, "De Date Assignment using Artificial Neural Network under Different Shop Floor Control Strategies,"

International Journal of Production Research, (Accepted) (SCI, EI)

5. D. Y. Sha, Sheng-Yuan Hsu, "The Integration of Shop Floor Control Strategies in Wafer Fabrication," ***Production Planning and Control***, (under reviewing, SCI, EI)
6. D. Y. Sha, Chao-Yang Liu, "A Tabu Search-Based Methodology for Shop Floor Control Integration Strategy in Semiconductor Wafer Fabrication," ***Integrated Manufacturing Systems***, (under reviewing) (EI)

本研究雖僅針對一實際個案構建之虛擬晶圓廠進行模擬驗證，但由於研究構建之虛擬晶圓廠已將各種晶圓製造廠之生產特性納入考慮，。並依據實際生產流程在各類虛擬加工設備上生產，雖然個案之機台數或產品數可能影響實際驗證結果，但各策略組合間之相對績效應不受此類因素影響，因此其結果應可適用在不同晶圓廠。當然若能依循本研究的作法，針對特定個案構建虛擬晶圓廠，並將各類法則納入模擬系統中，則更可進一步快速進行現場控制策略之整合性決策。

另外，由於晶圓廠製程複雜度甚高，因此在其他較單純的生產系統，如：典型零工式(job shop)生產的機械工廠，由於其生產特性亦類似於晶圓廠，因此本研究構建之「以類神經網路為基礎之交期指派法則」亦應適用之。在現場控制策略的整合方面，由於各類控制策略間之交互作用十分明顯，因此生產控制策略組合的概念，亦應值得其他各類型生產系統參考之。

附錄一、LIST OF ABBREVIATIONS

Abbreviation	Illustration
ORR	order review and release
DDA	due date assignment
WIP	work in process
ANN	artificial neural network
BPN	back-propagation network
SFC	shop floor control
AI	artificial intelligence
TWK	due date prediction rule based on total amount of works
SLK	due date prediction rule based on slack time
NOP	due date prediction rule based on number of operations
JIQ	due date prediction rule based on current queue length in system
JIBQ	due date prediction rule based on queue length in bottleneck station
WIP	work in process
PSP	pre-shop-pool
KFM	regression-based due date prediction rule considering key factor
SFM	regression-based due date prediction rule considering significant factors

附錄二、 METHODOLOGIES OF SFC RULES

2.1 Due Date Assignment Rules

1. TWK

This rule assigns due dates to each order as a multiple of the order's total processing time. TWK is widely used in practice. The TWK rule is as follows:

$$d_i = r_i + k * p_i$$

Where d_i denotes the assigned due date for order i and k is the parameter that reflects the expected queue time that order i will experience in the system. The k value is estimated based on the regression models.

2. JIQ (jobs in queue)

This method assigns due dates to each order as a multiple of the number of orders in the queue. JIQ is widely used in practice. The JIQ rule is as follows:

$$d_i = r_i + p_i + k * q_s$$

Where di denotes the assigned due date for order i and k is the parameter that reflects the expected queue time that order i will experience in the system. The k value is estimated based on the regression models.

3. JIBQ (jobs in bottleneck queue)

This method is used in the system having the significant bottleneck. The due date of each order is assigned just considering the length of the queue in the bottleneck workstation. The JIBQ rule is as follows:

$$d_i = r_i + p_i + k * q_{bottleneck}$$

Where di denotes the assigned due date for order i and k is the parameter that reflects the expected queue time that order i will experience in the system. The k value is estimated based on the regression models.

2.2 Order Release and Review Rules

1.WR(workload regulation, Wein 1988)

WR regulating new wafer releases to maintain a constant amount of expected work at a bottleneck station. WR monitor the sum of remaining processing times at the bottleneck workstation for all lots in the fab and release a new lot when this sum falls below a critical value. Here, throughput can be controlled by changing the critical value.

2.CONWIP(constant work in process)

CONWIP regulating new wafer releases to maintain a constant number of lots in the production system. CONWIP starts a new lot whenever a lot is completed. With this rule, throughput is controlled by the WP level.

3.SA (starvation avoiding, Glassey and Resende 1988)

SA released a new wafer lot to avoid starvation of a bottleneck workstation. SA starts a new lot to avoid idling the bottleneck workstation due to lack of work. More specifically, a new lot is released when virtual inventory at the bottleneck workstation falls down to a predetermined value. The virtual inventory at the bottleneck workstation can be estimated by the sum of the actual inventory at the workstation and WIP at upstream workstations that is expected to arrive at the bottleneck workstation within the lead time (L). Here the lead time is estimated with the sum of processing times operations that must be processed for a newly released lot before it visits the bottleneck for the first time. The predetermined value that triggers a lot release can be set to $\alpha \cdot L$, where α is a control parameter.

4.UNIF

Release a new lot into the fab at a constant rate, e.g. 16 lot/per-day independent of the current WIP level or system status.

5.POISS

Lots enter the fab according to a Poisson Distribution. New wafer releases time are randomly generated from Poisson distribution.

6.TB(two boundary, Lou and Kager 1989)

If the actual output of first layer < expected output and actual inventory of first layer< predetermined inventory level, the job will be a candidate. The candidates have the largest value of weight of product × difference in output will be released. TB uses two threshold values for each part type at each stage. The rule is motivated by analyzes of two machine tandem-systems with unreliable machines. It contains the following three steps to determine releasing and/or dispatching of a part:

Step1: Compute the WIP deviation and the surplus deviation, $\triangle_{bij} = h_{bij} - {}_{bij}$, $\triangle_{sij} = h_{sij} - s_{ij}$.

Step2: Job release: Load the candidate parts that has the largest $p_i\triangle_{si1}$. In other words, select the part type that is far behind its production plan and had, at the same time, a high priority.

Step3: Job dispatch into hub: Load the parts having the largest $p_j e_i \triangle_{sij}$.

7.WCEDD

Regulating new wafer releases to maintain their predetermined WIP level of main workstations.

2.3 Dispatching Rules

1.FIFO

Select the lot, which arrived in the queue at the earliest time.

2.EDD

Select the lot, which has the earliest due date in the queue.

3.CR

Smallest CR, CR=(due date-total remaining PT-present date) / total remaining PT

4.NexQL

The lot whose queue at the next station it will visit has the least amount of expected work per machine will be assigned high priority.

5.SRPT

Select the lot that has the shortest expected remaining processing time until it exist the fab.

6.COVERT

The job with the largest C will be assigned high priority, C = delaying cost/total remaining PT.

7.SA+(Glassey and Resende, 1988)

Assign high priority to jobs that are close to the bottleneck station and/or that contribute a large amount of work content to the station. The main characteristic of this SA-booster dispatching rule is its dynamic behavior. The rule combines two simple rules by mean of weights and dynamically changes the weights according to the state of the system. If the bottleneck is in no danger of starvation the dispatching rule gives more weight to the SRPT rule, while if there is imminent danger, more weight is given to a rule (SA+) that gives high priority to lots that are headed for the bottleneck station. The composite SA dispatching rule is a weighted mix of SRPT and SA+. Its normalized priority function is given by

$$\overline{p}_{SA} = (1-\gamma)\overline{p}_{SRPT} + \gamma(1-\overline{p}_{SA+})$$

Where $0 \leqq \gamma \leqq 1$ is the dynamic weight.

$$p_{SRPT} = \sum_{j=i}^{T} d_j \qquad p_{SA+} = \frac{d_{n_i}}{\sum_{j=i}^{n_i-1} d_j}$$

We require the dynamic weight γ to be close to 1 when there is imminent danger of bottleneck starvation (so that SA+ will dominate dispatching) and to approach 0 when the bottleneck is not in immediate danger of starving (forcing SRPT to be used to dispatch). This can be achieved in the following way.

Let τ be the critical work content discussed earlier (a constant parameter) and let W be the virtual inventory.

$\tau = \alpha$ L

$$W = (R + \sum_{i \in Q} K_i d_{n_i}) / m$$

By assuming that an infinite supply of new jobs is available for release we can guarantee that the SA release strategy will never allow W to become null.

The dynamic convex weight is defined for all values of W > 0, as

$$\gamma = \frac{\{1/(1+e^{-\tau/W}) - 1/2\}}{1/2}$$

This definition produces a dynamic weight function having the desired properties, i.e., $\gamma \rightarrow 0$ if W >> τ and $\gamma \rightarrow 1$ if W << τ .

Observe that P_{SA+} may not be defined for all lots. In particular, if the lot is at a bottleneck step or at a step at the end of the process, for which there is no future visit to the bottleneck, the priority function is undefined. For these two exceptions lots are displaced according to SRPT.

8.TB+(Lou and Kager, 1989)

If the actual output of each layer < expected output and actual inventory of each layer < predetermined inventory level, the job will be a candidate. The candidates have the largest value of weight of product × weight of layers × difference in output will be assigned high priority.

2.4 Rework Rules

1. Lock-step(Zager, 1995)

In this rule, the child lot must be defaulted as a hot lot that can directly be reworked in photolithography process without having to enter the queuing line. The mother lot shall wait to remerge with the child lot to become the original lot when rework is completed before continuing with the follow-up processes. Since the mother lot needs to wait for the rework on child lot, the total processing time for the wafer lot will be extended significantly.

2. Lot-split (Zager, 1995)

In this rule, the mother lot shall continue with follow-up processes without having to wait for the child lot. Since the mother lot does not need to wait for the child lot, the child lot remains as an ordinary lot without having to be defaulted as a hot lot and shall enter the queuing line waiting to be reworked. The reworked child lot will become a new independent lot to proceed with the follow-up processes.

3. Rendezvous (Sha et al. 2001)

The mother lot does not need to wait for the child lot in order to shorten the processing time and the child lot shall be defaulted as a hot lot without

having to queue up for rework in order to remerge with the separated mother lot. So, the mother lot shall proceed with follow-up processes and the child lot shall be reworked immediately after they separate. The child lot shall then follow the original mother lot to the next process where they shall remerge into the original lot.

附錄三、LIST OF PREDICTION FACTORS

Main Class	Subclass	Factors
1. System Condition	1.1 Shop status (8)	1. total WIP in the shop 2. total remaining workload in the shop 3. total WIP of DRAM in the shop 4. total WIP of SRAM in the shop 5. total WIP of LOGIC in the shop 6. total remaining workload of DRAM in the shop 7. total remaining workload of SRAM in the shop 8. total remaining workload of LOGIC in the shop
	1.2 Bottleneck status (10)	9. number of lots in the bottleneck 10. total remaining workload in the bottleneck 11. total remaining workload of DRAM in the bottleneck 12. total remaining workload of SRAM in the bottleneck 13. total remaining workload of LOGIC in the bottleneck 14. total WIP of DRAM in the bottleneck 15. total WIP of SRAM in the bottleneck 16. total WIP of LOGIC in the bottleneck 17. number of shot-down machine in the bottleneck 18. total remaining workload of the bottleneck in the shop

Main Class	Subclass	Factors
1.System Condition	1.3 Constraint resource status (50)	19. number of WIP in the IMPLANTER_H 20. number of WIP in the RCA_CLEAN 21. number of WIP in the GATE_OXIDE 22. number of WIP in the LPCVD_POLY 23. number of WIP in the N_DOPE 24. total remaining workload in the IMPLANTER_H 25. total remaining workload in the RCA_CLEAN 26. total remaining workload in the GATE_OXIDE 27. total remaining workload in the LPCVD_POLY 28. total remaining workload in the N_DOPE 29. the WIP of DRAM in the IMPLANTER_H 30. the WIP of SRAM in the IMPLANTER_H 31. the WIP of LOGIC in the IMPLANTER_H 32. the WIP of DRAM in the RCA_CLEAN 33. the WIP of SRAM in the RCA_CLEAN 34. the WIP of LOGIC in the RCA_CLEAN 35. the WIP of DRAM in the GATE_OXIDE 36. the WIP of SRAM in the GATE_OXIDE

Main Class	Subclass	Factors
1.System Condition	1.3 Constraint resource status (50)	37. the WIP of LOGIC in the GATE_OXIDE 38. the WIP of DRAM in the LPCVD_POLY 39. the WIP SRAM in the LPCVD_POLY 40. the WIP LOGIC in the LPCVD_POLY 41. the WIP of DRAM in the N_DOPE 42. the WIP of SRAM in the N_DOPE 43. the WIP of LOGIC in the N_DOPE 44. total remaining workload of DRAM in the IMPLANTER_H 45. total remaining workload of SRAM in the IMPLANTER_H 46. total remaining workload of LOGIC in the IMPLANTER_H 47. total remaining workload of DRAM in the RCA_CLEAN 48. total remaining workload of SRAM in the RCA_CLEAN 49. total remaining workload of LOGIC in the RCA_CLEAN 50. total remaining workload of DRAM in the GATE_OXIDE 51. total remaining workload of SRAM in the GATE_OXIDE 52. total remaining workload of LOGIC in the GATE_OXIDE 53. total remaining workload of DRAM in the LPCVD_POLY 54. total remaining workload of SRAM in the LPCVD_POLY 55. total remaining workload of LOGIC in the LPCVD_POLY 56. total remaining workload of DRAM in the N_DOPE 57. total remaining workload of SRAM in the N_DOPE 58. total remaining workload of LOGIC in the N_DOPE 59. number of shot-down machine in the N_DOPE 60. number of shot-down machine in the IMPLANTER_H

Main Class	Subclass	Factors
1.System Condition	1.3 Constraint resource status (50)	61. number of shot-down machine in the RCA_CLEAN 62. number of shot-down machine in the GATE_OXIDE 63. number of shot-down machine in the LPCVD_POLY 64. total remaining workload of IMPLANTER_H in the shop 65. total remaining workload of RCA_CLEAN in the shop 66. total remaining workload of GATE_OXIDE in the shop 67. total remaining workload of LPCVD_POLY in the shop 68. total remaining workload of N_DOPE in the shop
	1.4 Recently completed orders (8)	69. average flow time of three lots which had only just finished 70. average flow time (three lots) of SRAM, which had only just finished. 71. average flow time (three lots) of DRAM, which had only just finished. 72. average flow time (three lots) of LOGIC, which had only just finished. 73. average waiting time (three lots) in the shop which had only just finished 74. average waiting time (three lots) of DRAM in the shop which had only just finished 75. average waiting time (three lots) of SRAM in the shop which had only just finished 76. average waiting time (three lots) of LOGIC in the shop which had only just finished

Main Class	Subclass	Factors
2.Order Characteristics (8)		77. total workload of the order 78. total workload on the bottleneck of the order 79. total workload on the IMPLANTER_H of the order 80. total workload on the RCA_CLEAN of the order 81. total workload on the GATE_OXIDE of the order 82. total workload on the LPCVD_POLY of the order 83. total workload on the N_DOPE of the order 84. product type of the order (1.DRAM, 2.SRAM 3.LOGIC)
3.PSP Condition	3.1 PSP status (4)	85. number of lots in the pre-shop-pool 86. number of lots of DRAM in the pre-shop-pool 87. number of lots of SRAM in the pre-shop-poop 88. number of lots of LOGIC in the pre-shop-poop
	3.2 Recently Completed orders (4)	89. average waiting time (three lots) in the pre-shop-pool which had only just finished 90. average waiting time (three lots) of DRAM in the pre-shop-pool which had only just finished 91. average waiting time (three lots) of SRAM in the pre-shop-pool which had only just finished 92. average waiting time (three lots) of LOGIC in the pre-shop-pool which had only just finished

附錄四、LIST OF WORKSTATIONS IN THE WAFER FAB.

Workstation	No. of machine	Workstation	No. of machine	Workstation	No. of machine
0 ETCH	3	H2SO4 STAT	4	RS METER	3
10:1 BOE	5	H3PO4 WET	4	RTP	4
100:1 HF	2	IMPLANTER(H)	6	S/D DENSIFY	5
130:1 BOE	1	IMPLANTER(M)	5	SAC OXIDE	4
50:1 BOE	5	IN-LINE SEM	7	SCA	1
7:1 BOE	2	LASER MARK	1	SCOPE	18
ADI	9	LPCVD NITRI	7	SCRUBBER	6
50% HF	1	LPCVD POLY	6	SOG COATER	7
AEI	4	LPCVD TEOS	8	SOG CURING	4
ALLOY	3	M GAUGE	1	SOG ETCH	7
ALPHA STEP	2	MEGASONIC	2	SOLVENT STAT	4
BAKING	6	MET VIA ETCH	8	SPUTTER	13
BIORAD	2	METAL ETCH	36	STEPPER	24
BOX CLEANER	1	N+ DOPE	3	STEPPER(PAS)	1
CV PLOTTER	1	NITRIDE ETCH	9	STRESS MET	1
DEFECT INSP	1	OFF-LINE SEM	1	SURFACE SCAN	4
DESCUM(MAT)	6	OFF-LINE TRA	1	TEOS-BPSG	8
DESCUM(TOK)	2	OXIDE ETCH	17	THERMA-WAVE	1
DRY PR STRIP	19	PAD ETCH	6	TRACK	26
E/B	5	PAD OXIDE	4	TRK PYIMIDE	2
ELLIPSO MET	5	PE TEOS	1	UV CURING	6
FIELD OXIDE	5	PECVD NITRI	7	VAPOR HF	4
FILM MEASURE	1	PECVD OXIDE	13	W SILICIDE	8
FILM THICK	9	POLY ETCH	12	WAFER INSPEC	4
FTIR	1	POLY WET ETC	2	WAFER TRACK	1
FURN PYIMIDE	1	POST CLEAN	2	WAT	7
GAP METER	1	RCA CLEAN	12	WCVD	3
GATE OXIDE	6	REFLOW/DENS	4	WELL DIFF	5
GRINDER	2	RETICLE STOC	1	WET PR STRIP	6

.total of workstation is 87, total of machine is 488

.Total Output per month=46,000 pcs

附錄五、THE MODEL OF VIRTUAL WAFER FAB.