Low-Power High-Performance Non-Volatile Memory on a Flexible Substrate with Excellent Endurance

*Chun-Hu Cheng, Fon-Shan Yeh, and Albert Chin**

Plastic-substrate-based electronic devices are attractive because of their inherit merits of low cost, light weight, environmentally friendly low temperature processing, and the application in flexible displays and integrated circuits (ICs). Fast progress of logic ICs using thin-film transistors (TFT) on plastic has been demonstrated. However, one fundamental challenge for plastic electronics is the lack of good performance non-volatile memory (NVM) devices.[1–5] This is due to the degraded dielectric quality of charge-based flash (CTF) memory from the limited low temperature process.[2] Alternatively, the resistive random access memory (RRAM)[6–21] shows promising NVM performance on plastic even when processed at low temperature, but the large set and reset currents are the basic limitation for high-density and low-power operation. In addition, the large switching energies degrade the endurance due to excessive stress.

In this paper, record high-performance NVM has been demonstrated on low cost polyimide substrate. A very low set current of 1.6 μA at 3 V (4.8 μW) and reset current of –0.5 nA at –2 V (1 nW) were needed to reach the bistable resistance state, which led to a large memory window with a high- to low-resistance state ratio (HRS/LRS) of 9×10^2. Additionally, good retention was obtained with a small HRS/LRS decay from the initial 9×10^2 to 7×10^2 at 85 °C for 10^4 s. Furthermore, excellent endurance of 10^5 cycles was measured at a very fast 50 ns switching time. This is the lowest reported switching power NVM on plastic with excellent 10^5 cycling endurance and good retention. The excellent NVM performance on flexible plastic is due to the using novel ultra-low power hopping conduction mechanism[22] rather than the conductive filament in conventional RRAM.[17,18] This new RRAM device sets a new standard for NVM performance on low-cost flexible substrates.

Figure 1 shows the devices fabricated of Ni/GeO$_x$/HfON/TaN RRAM on flexible polyimide substrate. The simple metal-insulator-metal (MIM) structure is useful for embedded and 3D integration.

Figure 2a shows the swept current–voltage (*I*–*V*) curves of Ni/GeO$_x$/Hf$_{0.38}$O$_{0.39}$N$_{0.23}$/TaN RRAM on flexible polyimide. The arrows indicate the sweeping direction. The Hf$_{0.38}$O$_{0.39}$N$_{0.23}$ (HfON) composition was determined by X-ray photoelectron spectroscopy (XPS), which was controlled by O$_2$/N$_2$ in a sputter system. The HfON has been used as the charge-trapping layer for CTF[23] NVM due to its high density traps and deep trapping energy. A very low self-compliance set current of 1.6 μA at 3 V, an even lower reset current of –0.5 nA at –2 V, and a large HRS/LRS memory window of 9×10^2 at 0.5 V were all obtained at the same time. These are the lowest set and reset currents of RRAM devices on a plastic film[3–5] and are much lower than the conventional RRAM using metallic-filament conduction.[17,18] The asymmetric switching *I*–*V* curves are ascribed to the different work function for electron injection of the bottom TaN (4.6 eV) and top Ni electrode (5.1 eV). The self-compliance current is useful to prevent abrupt increase of set current, which causes hard breakdown. Such very small reset current and asymmetric *I*–*V* can be driven by a Schottky diode at reverse bias voltage to form the simple 1-RRAM-1-doide (1R1D) structure with the small $4F^2$ cell size, where F is the minimum feature size. It is important to note that the proper bias scheme is essential to reach the low switching current. Figure 2b shows the same Ni/GeO$_x$/HfON/TaN RRAM on flexible polyimide biased at the conventional unipolar mode, where a high compliance current of 1 mA is used during set to LRS. However,

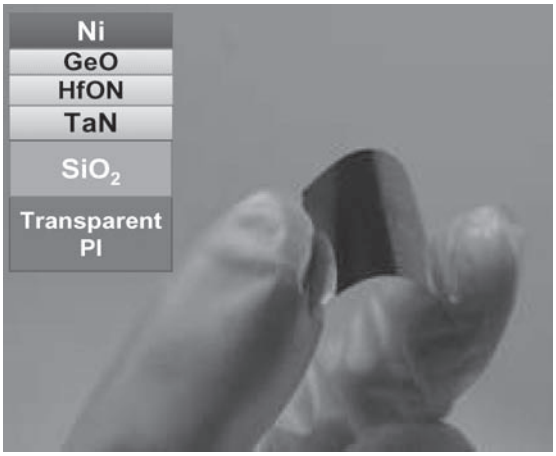

Figure 1. Photograph of flexible Ni/GeO$_x$/HfON/TaN NVM devices.

Prof. A. Chin
Depatment of Electronics Engineering
National Chiao-Tung University
Hsinchu, 30010, Taiwan
E-mail: albert_achin@hotmail.com
Dr. C. H. Cheng
Department of Electronics Engineering and Institute of Electronics Engineering
National Tsing-Hua University
Hsinchu, 30010, Taiwan
Prof. F. S. Yeh
Department of Electronics Engineering and Institute of Electronics Engineering
National Tsing-Hua University
Hsinchu, 30010, Taiwan

DOI: 10.1002/adma.201002946

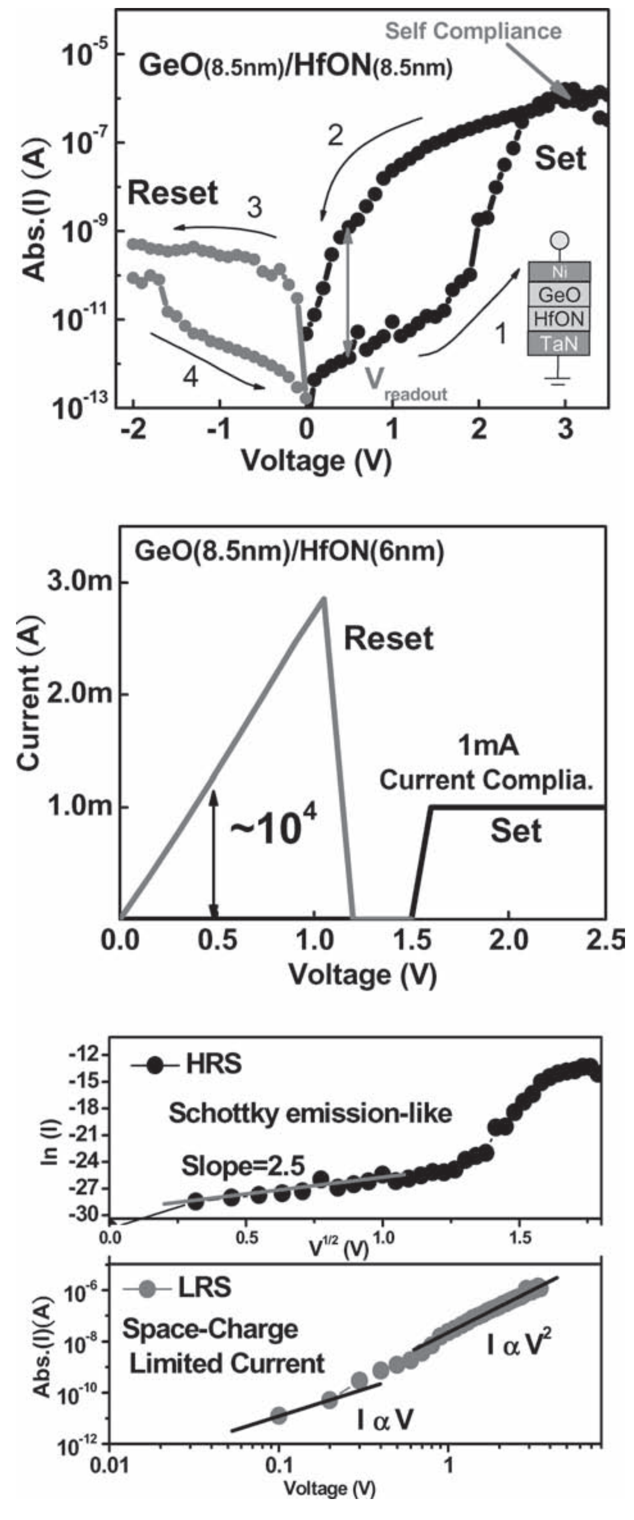

Figure 2. a) Swept *I–V* curves of Ni/GeO$_x$/HfON/TaN RRAM on flexible polyimide. b) The same device operated under unipolar mode. c) *I–V* at HRS and LRS by fitting with Schottky-emission and SCLC conduction mechanisms, respectively.

this mode suffers from the high reset current to HRS, poor endurance, and a large-size transistor to deliver the high LRS and HRS currents. To understand such low switching currents, we have analyzed the current conduction mechanism. Figure 2c shows the measured and fitted *I–V* characteristics at HRS and LRS, respectively. The very small HRS current is due to Schottky emission via high work function Ni. Similar Schottky emission governed by current conduction was also found in the MIM capacitors used for dynamic random access memory (DRAM) application.[24] The current at LRS is ruled by space–charge-limited current (SCLC), indicating the current conduction of LRS is due to traps[25] in dielectrics of HfON and GeO$_x$. From XPS measurements, the oxygen vacancies and nitrogen vacancies were identified in GeO$_x$ and HfON. Therefore, the very low set current may be due to the electron hopping via these defects.[22,26] This is further verified by the measured negative temperature coefficient (TC)[22,26] that is quite different from the positive TC in a conductive metallic filament of traditional metal-oxide RRAM with large set and reset currents. In addition, no metallic filament can be formed in covalently bonded GeO$_x$, which also leads to different mechanism from metallic filament conduction of traditional metal-oxide RRAM. The hopping conduction also provides a very large resistance,[26] which leads to a small self-compliance set current.

Good endurance is the fundamental challenge for NVM.[27] **Figure 3**a shows the impulse voltage response of Ni/GeO$_x$/HfON/TaN RRAM on polyimide, where the voltage pulse is applied to a 4 MΩ resistor that is series connected to the RRAM. Fast RRAM switching time of 50 ns is measured at an applied over-stressed set pulse of 50 ns and 3.5 V, where the distorted output waveform is due to the parasitic capacitance and bonding wire. Figure 3b shows the measured endurance characteristics as a function of the over-stressed voltage cycles. Excellent electrical endurance of 10^5 cycles is obtained, which is even comparable with flash NVM.[27] The increase of the HRS leakage current with increasing stress cycles is also found in MIM capacitors and is due to stress-induced leakage current (SILC) via generated defects.[28] The decrease in LRS current after continuous stress may be related to the redistribution of charged oxygen/nitrogen vacancies[29] under a switching electric field, where the SCLC conduction for LSR current is highly related to the traps. The mechanical endurance is the necessary factor for flexible electronics. Figure 3c shows the mechanical endurance, where the mechanical stress is applied by bending the RRAM devices on polyimide to a small 9-mm radius at every second. Excellent mechanical endurance is observed from the stable HRS and LRS values up to 10^5 bending instances and is useful for flexible electronics.

The retention characteristics are important parameter for a NVM device. **Figure 4** shows the measured 85 °C retention characteristics of Ni/GeO$_x$/HfON/TaN RRAM on polyimide. Good retention is obtained with small HRS/LRS decay from the initial 9×10^2 to 7×10^2 for 10^4 s at 85 °C, which may be related to the deep trap energy in HfON and the large conduction band offset between GeO$_x$ and HfON for charge hopping conduction. Since the RRAM has a uniquely low switching power, the device temperature on flexible plastic should be significantly lower than the typical 85 °C retention temperature used for a NVM IC test in a computer. Therefore, the cycling endurance may be a major limiting factor for device lifetime beyond retention.

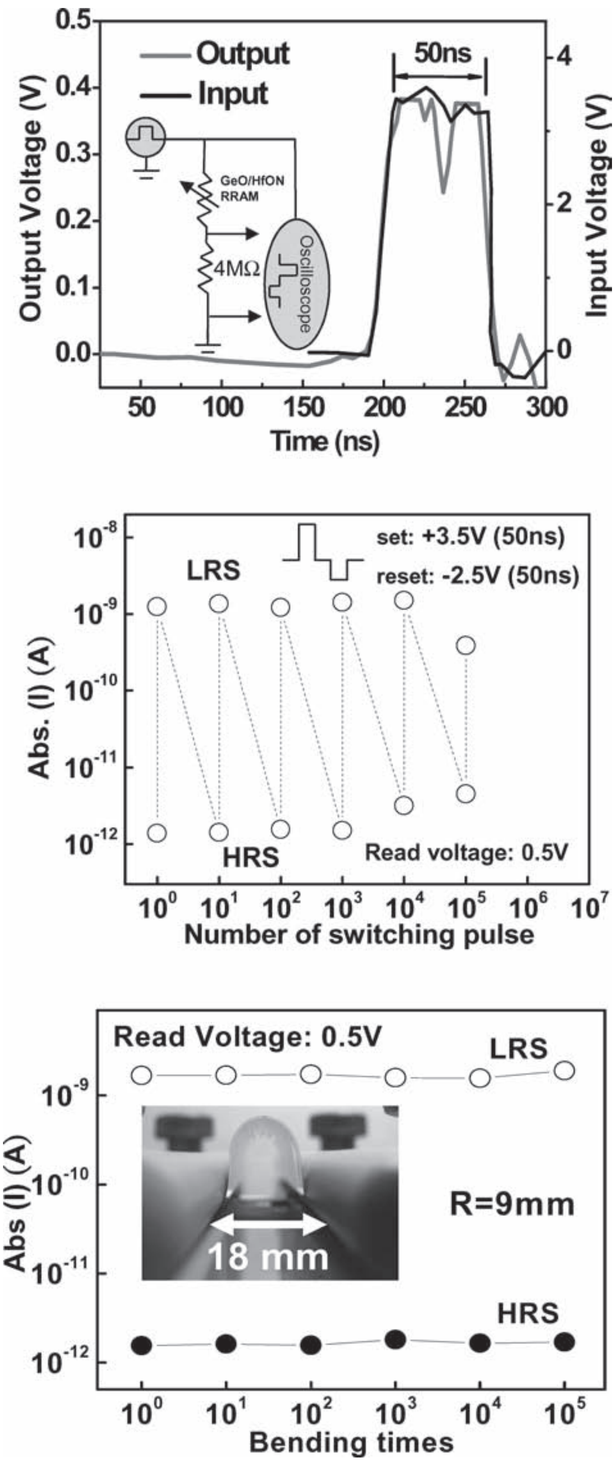

Figure 3. a) Impulse voltage response, b) electrical endurance, and c) mechanical endurance of flexible Ni/GeO$_x$/HfON/TaN RRAMs.

In conclusion, this new flexible RRAM device has the lowest recorded switching power (4.8 μW/1 nW), large on/off memory window, good 85 °C retention, a fast 50 ns switching time, and excellent 10^5 electrical and mechanical endurance. Such excellent performances are even comparable to flash NVM on Si.

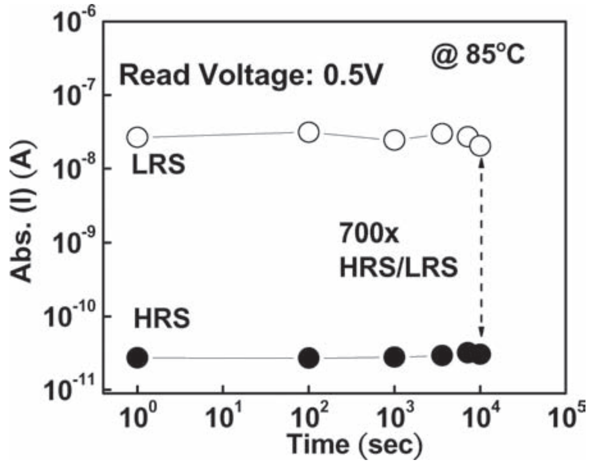

Figure 4. Retention characteristics of Ni/GeO$_x$/HfON/TaN RRAM on flexible polyimide.

Experimental Section

The RRAM devices were fabricated on low-cost flexible polyimide substrates, as shown in Figure 1a. The RRAM had the same metal-insulator-metal (MIM) structure as analog RF and DRAM capacitors. A thin 100 nm SiO_2 buffer layer was first deposited on polyimide. Then, 100 nm TaN was deposited by sputtering and patterned as a bottom electrode. After that, the 8.5-nm-thick hafnium oxynitride ($Hf_{0.38}O_{0.39}N_{0.23}$) was deposited. The HfON composition was determined by X-ray photoelectron spectroscopy (XPS). Sequentially, the 8.5-nm-thick GeO$_x$ dielectrics were deposited. Finally, the 50-nm Ni top electrode was deposited and patterned by a metal mask.

Acknowledgements

The authors would like to thank the important help from Director Toshihko Kanayama at National Institute of Advance Industrial Science and Technology, Japan.
The paper publication was supported by National Science Council of Taiwan.

Received: August 16, 2010
Published online: December 20, 2010

---

[1] K. J. Baeg, Y. Y. Noh, J. Ghim, S. J. Kang, H. Lee, D. Y. Kim, *Adv. Mater.* **2006**, *18*, 3179.
[2] M. F. Chang, P. T. Lee, S. P. McAlister, A. Chin, *Appl. Phys. Lett.* **2008**, *93*, 233302.
[3] M.-J. Lee, C. B. Lee, S. Kim, H. Yin, J. Park, S. E. Ahn, B. S. Kang, K. H. Kim, G. Stefanovich, I. Song, S. W. Kim, J. H. Lee, S. J. Chung, Y. H. Kim, C. S. Lee, J. B. Park, I. G. Baek, C. J. Kim, Y. Park, *IEDM Tech. Dig.* **2008**, *85*.
[4] S. Kim, H. Moon, D. Gupta, S. Yoo, Y. K. Choi, *IEEE Trans. Electron Device* **2009**, *56*, 696.
[5] J. W. Seo, J. W. Park, K. S. Lin, S. J. Kang, Y. H. Hong, J. H. Yang, L. Fang, G. Y. Sung, H. K. Kim, *Appl. Phys. Lett.* **2009**, *95*, 133508.
[6] G. H. Buh, I. Hwang, B. H. Park, *Appl. Phys. Lett.* **2009**, *95*, 142101.
[7] X. Wu, P. Zhou, J. Li, L. Y. Chen, H. B. Lv, Y. Y. Lin, T. A. Tang, *Appl. Phys. Lett.* **2007**, *90*, 183507.

[8] B. Sun, Y. X. Liu, L. F. Liu, N. Xu, Y. Wang, X. Y. Liu, R. Q. Han, J. F. Kang, *Appl. Phys. Lett.* **2009**, *105*, 061630.
[9] W. Guan, S. Long, R. Jia, M. Liu, *Appl. Phys. Lett.* **2007**, *91*, 062111.
[10] N. Xu, L. Liu, X. Sun, X. Liu, D. Han, Y. Wang, R. Han, J. Kang, B. Yu, *Appl. Phys. Lett.* **2008**, *92*, 232112.
[11] C. Yoshida, K. Tsunoda, H. Noshiro, Y. Sugiyama, *Appl. Phys. Lett.* **2007**, *91*, 223510.
[12] R. Dong, D. S. Lee, W. F. Xiang, S. J. Oh, D. J. Seong, S. H. Heo, H. J. Choi, M. J. Kwon, S. N. Seo, M. B. Pyun, M. Hasan, H. Hwang, *Appl. Phys. Lett.* **2007**, *90*, 042107.
[13] P. Zhou, M. Yin, H. J. Wan, H. B. Lu, T. A. Tang, Y. Y. Lin, *Appl. Phys. Lett.* **2009**, *94*, 053510.
[14] D. Lee, D. J. Seong, I. Jo, F. Xiang, R. Dong, S. Oh, H. Hwang, *Appl. Phys. Lett.* **2007**, *90*, 122104.
[15] D. Choi, D. Lee, H. Sim, M. Chang, H. Hwang, *Appl. Phys. Lett.* **2006**, *88*, 082904.
[16] M. C. Ni, S. M. Guo, H. F. Tian, Y. G. Zhao, J. Q. Li, *Appl. Phys. Lett.* **2007**, *91*, 183502.
[17] R. Waser, M. Aono, *Nat. Mater.* **2007**, *6*, 833.
[18] C. Cagli, F. Nardi, D. Ielmini, *IEEE Trans. Electron Devices* **2009**, *56*, 1712.
[19] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, M.-J. Tsai, *IEDM Tech. Dig.* **2008**, 297.
[20] M. Janousch, G. I. Meijer, U. Staub, B. Delley, S. F. Karg, B. P. Andreasson, *Adv. Mater.* **2007**, *19*, 2232.
[21] R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.
[22] C. H. Cheng, A. Chin, F. S. Yeh, *VLSI Symp. Tech. Dig.* **2010**, *85*.
[23] S. H. Lin, A. Chin, F. S. Yeh, S. P. McAlister, *IEDM Tech. Dig.* **2008**, *843*.
[24] K. C. Chiang, C. H. Cheng, H. C. Pan, C. N. Hsiao, C. P. Chou, A. Chin, H. L. Hwang, *IEEE Electron Device Lett.* **2007**, *28*, 235.
[25] A. Rose, *Phys. Rev.* **1955**, *97*, 1538.
[26] A. Chin, K. Lee, B. C. Lin, S. Horng, *Appl. Phys. Lett.* **1996**, *69*, 653.
[27] International Technology Roadmap for Semiconductors (ITRS), **2009**, www.itrs.net (accessed August 2010).
[28] S. B. Chen, J. H. Lai, A. Chin, J. C. Hsieh, J. Liu, *IEEE Electron Device Lett.* **2002**, *23*, 185.
[29] W. Shen, R. Dittmann, U. Breuer, R. Waser, *Appl. Phys. Lett.* **2008**, *93*, 222102.