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子計劃三：以智財單元為基系統晶片設計之測試技術研究

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以智財單元為基系統晶片設計之測試技術研究(III)
Testing Technology Exploitation for IP-Based SOC Design(III)

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一、中文摘要

本計畫是在"以智財單元為基系統晶片設計之驗證與測試技術開發研究"總計畫項下之一子計畫，目的是研究有關以智財單元為基之系統晶片於深次微米情況下之測試諸問題。本計畫分三年執行，本年度(第三年)之執行計劃摘要如下：

(一)、信號傳輸線之信號傳輸完整性與測試研究：

於本子題中，吾人對深次微米信號傳輸線中因耦合效果而產生之突波障礙與延遲障礙之相互關係做一深入研究，並發展了一套統合的測試方式。

(二)、類比智財之測試與診斷：

於本子題中，吾人對類比智財中之時鐘信號之不穩度(Jitter)，發展了一個量測電路。此電路解析度可達 49.3ps，且能建構於 SOC 晶片中。

(三)、一個應用於 DAC 測試之高度線性 VCO 電路：

於本子題中，吾人發展了一個可應用於DAC測試之高度線性隻電壓控制振盪器(VCO)。此振盪器線路簡單，成本低廉，精確度可達9 bits，是一可應用於SOC晶片中作一般DAC測試或其他高線性電壓控制振盪器應用之IP。

(四)、一測試耦合障礙之內建式自我測試線路：

於本子題中，吾人對深次微米邏輯電路所產生之耦合障礙，提出一個內建式自我測試線路。吾人提出一個簡單模擬耦合串音雜訊之邏輯符號，而使得產生測試圖樣簡單化。

(五)、液晶顯示器推動線路IC之測試：

於本子題中，吾人對液晶顯示器推動線路IC藉重新推導其障礙模式，發展了一個改進的測試方法，並增進測試效率。並利用加壓加速測試方法，增進了IC的可靠度。

Abstract

This project is one of sub-projects of the integrated joint project "Verification and Testing Technology Exploitation for IP-Based SOC Design". It aims to study issues and problems encountered in testing for the IP-based SOC design in the deep submicron regime. The topics and works accomplished for this year are:

(1) Signal integrity study and test generation:

For this topic, we have studied the relationship between glitches and induced-delays of crosstalk faults for the deep submicron interconnection lines. A unified test scheme is proposed and demonstrated to test both types of crosstalk faults.

(2) Analog IP testing and diagnoses:

For this topic, we have developed an on-chip jitter measurement circuit for clock signals in an SOC chip. The circuit can measure clock jitter up to a resolution of 49.3 ps and can be embedded into SOC as a BIST circuit.

(3) A highly linear VCO for DAC testing:

For this sub-topic, we have developed a highly linear VCO which can be used as the signal generator for DAC testing. It is simple, has a prevision up to 9 bits and can be incorporated into an SOC chip.

(4) A BIST circuit for testing crosstalk faults:

For this topic, we have developed a BIST circuit which can be incorporated into the boundary so an environment to test crosstalk – induced glitch faults for deep submicron circuits. For this circuit, a simple logic symbol is proposed to model the crosstalk effect and this makes test generation simple.

(5) Testing of TFT LCD source driver IC:

For this topic, we have classified fault models according to special features of the TFT LCD source driver circuit and developed simplified test set to improve test efficiency. In addition, we have also adopted a stress test methodology to improve the reliability of the IC.

Keywords: VLSI Testing, IP, Jitter, Analog Circuit Testing, BIST, TFT Driver Circuit.

二、緣由與目的

(一)、信號傳輸線之信號傳輸完整性與測試研究：

此問題之發生是因深次微米SOC晶片中，因傳輸線間距太過緻密，在近距離電容耦合效應下，會導致兩類之藕合障礙，即一為串音雜波，另一為延遲障礙。此二類藕合障礙皆需用不同之測試方法，而其後者更是需用特別的時脈信號與線路安排才能測試。本子題即在研究此二類藕合障礙之相互關係，並期望發展出一統合方法，能同時測試兩類障礙，如此可大大減低測試之複雜度與成本。

(二)、類比智財之測試與診斷：

當類比智財應用於 SOC 晶片中時，一極重要之要素為其皆由一主時脈信號(master clock)來控制其相互間之同步與工作。故於一 SOC 晶片中，時脈信號之穩定性成為一重要課題。於 SOC 測試中，常希望測得該晶片之時脈信號之穩定度為何。且進行此測試時，最好其測試線路亦可內建於 SOC 晶片中。本子題即為在研究並提出一此內建式測試線路。而此提出之內建式時脈測試線路本身亦可視為一智財。

(三)、一個應用於 DAC 測試之高度線性 VCO 電路：

於 SOC 中 DAC 測試時，常需於其輸出端接一 ADC。此 ADC 需要有高度線性特性。一 VCO 極為一此類 ADC。但過往一般之 VCO 其線性範圍不高(5~6 bits)，如何提高一 VCO 之線性度範圍是一研究課題。於本子題中，吾人嘗試發展一 EMOS 元件，架構簡單之 VCO 而其線性範圍可高達至 9bits。此 VCO 可輕易地內建於一 SOC 之，亦可單獨作一電壓控制振盪器之用。

(四)、一測試藕何障礙之內建式自我測試線路：

如前所述，於深次微米晶片中，為保證晶片正常工作效能，藕合障礙是一必須測試之項目。但藕合障礙之測試，特別是其測試圖樣之產生，因牽涉到時序問題，並不容易。如何能想出一方法，能簡化此測試圖樣產生過程，且將測試方法應用於在邊界掃描(Boundary Scan)之設計環境中是一大課題。本子題極為在解決上述問題。

(五)、液晶顯示器推動線路 IC 之測試：

液晶顯示器已是本國兩大支柱產業之一。而液晶顯示器中一重要元件：退動線路 IC，因此 IC 之線路結構特殊，是由一類如 DAC 元件排列成記憶體型式而成，其測

試需要特別考量。目前半導體大廠如華邦等，其測試皆是循一般類如記憶體測試之方式達成。其真正之障礙涵蓋率，測試效率等皆無人作系統性研究過。本子題即針對上述原因對此類 IC 作系統性之研究。

三、結果與討論

(1) Signal integrity study and test generation:

For the deep submicron integrated circuit, signal integrity and propagation becomes an issue due to crosstalk effects. In general, there are two fault effects, namely crosstalk-induced glitches, and the crosstalk-induced delay. In this work, we investigate the origin of their occurrence, their relationship and identify their respective importance in affecting the circuit performance, and propose an approach for which both glitches and delay can be tested in a uniform way. With the proposed method, fault detection for crosstalk noises can be greatly simplified. The work also investigates the process variation issue for the proposed scheme. The results of this work have been written into a paper and submitted to ISCAS 2004 for consideration for presentation [1].

(2) Analog IP testing and diagnosis:

PLL is an important circuit module in providing clock signals to all other circuit blocks of an SOC. This work proposes and demonstrates a built-on-chip PLL jitter measurement circuit, which utilizes the vernier delay line principle but transforms timing difference signals into digital words. It has a self calibration capability to minimize the mismatched error caused by the process variation. The circuit offers a high resolution that a 49.3 ps resolution can be obtained for a 0.35μm technology implementation. The results of this have been written into a paper to be presented in ATS 2003 [2].

(3) A highly linear VCO for DAC testing:

For the DAC testing, especially for on-chip testing, usually a highly linear ADC is needed to calibrate the output of the DAC. In this work, we present a high linearity VCO which is simple and can be incorporated easily into the SOC chip for the on-chip testing. The VCO is constructed by using the conventional oscillation ring structure but a feed back mechanism using the OP loop is adopted to achieve the high linearity. A parameter “***VCO Linearity***” is proposed to characterize the linearity of the VCO. The VCO presented is shown to be able to give a ***VCO Linearity*** of 532 which corresponds to a 9-bit resolution, as compared to the 4-bit resolution of the conventional VCO. It is suitable to be incorporated into the SOC chip for the purpose of the on-chip testing. Results of this work are being written into a paper to be submitted to Electronics Letters [3].

(4) A BIST circuit for testing glitch crosstalk faults:

Crosstalk faults are difficult to test due to their pattern dependency and unpredictivity in timing. In this work, a BIST scheme based on a square wave oscillation test signal to test the induced-pulse type of the crosstalk fault of embedded circuits in the boundary scan environment for deep sub-micron VLSI is proposed. The scheme applies square wave oscillation test signals in conjunction with pseudo random patterns to induce pulses which are caused by crosstalk faults and tests them. Modifications on boundary scan cells with simple added detection circuits to facilitate this test scheme are presented. Experimental results show that the average fault coverage obtained by applying the scheme to large size benchmark circuits can easily reach 90%.

Results of this work have been written into a paper for consideration in IEEE Design and Test [4].

(5) Testing of TFT LCD source driver IC:

For this topic, at first, according to the physical layout, the circuit diagram and

function of the circuit, 13 function fault models are derived with their syndrome. A complete set of all-code-diagonal patterns is used to replace the original high-voltage-code-diagonal patterns to test the circuit to achieve higher fault coverage. A formula to calculate the required number of test patterns for the parallel multiplexers has also been derived. Furthermore, a "stress test" method using high-voltage and high-temperature, incorporated with the all-code-diagonal pattern is adopted to test the circuit and the standby-current (Isb) is measured to screen out the weak defective chips to achieve Early-Failure-Rate reduction. Results of the work is being written into a paper for submission to ITC.

四、計畫成果自評

本計畫於第一年已建立智財單元本身與相互間連線的測試機制，在第二年執行期間也順利地分別對數位、類比與混合訊號電智財單元提出有效的測試與診斷的架構與方法。於第三年期間對上述各課題有更深入之研究並提出了解決方法。大部分的研究成果皆符合吾人原提計劃，完成度應達 80%以上，且部分成果已或將發表於國際會議或期刊[1-4]，或碩士論文中[5-8]。

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