行政院國家科學委員會專題研究計畫　成果報告

總計劃

計畫類別：整合型計畫
計畫編號：NSC91-2215-E-009-078-
執行期間：91 年 08 月 01 日至 92 年 07 月 31 日
執行單位：國立交通大學電子工程學系

計畫主持人：李崇仁
共同主持人：董蘭榮，陳竹一

報告類型：精簡報告

處理方式：本計畫可公開查詢

中　華　民　國 92 年 10 月 28 日

行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告 □期中進度報告

對以智財單元為基系統晶片設計之驗證與測試技術開發研究

計畫類別：□ 個別型計畫　　■ 整合型計畫
計畫編號：NSC 91－2215－E－009－078
執行期間：　91 年　8 月　1 日至　92 年　7 月　31 日

主持人：李崇仁教授　交通大學電子工程系

共同主持人：董蘭榮教授　交通大學電機與控制工程系

陳竹一教授　中華大學電機系

成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

本成果報告包括以下應繳交之附件：
□赴國外出差或研習心得報告一份
□赴大陸地區出差或研習心得報告一份
□出席國際學術會議心得報告及發表之論文各一份
□國際合作研究計畫國外研究報告書一份

處理方式：除產學合作研究計畫、提升產業技術及人才培育研究計畫、列管計畫及下列情形者外，得立即公開查詢
□涉及專利或其他智慧財產權，□一年□二年後可公開查詢

執行單位：國立交通大學電子工程學系

中　華　民　國　九十二年　十月　二十八

對以智財單元為基系統晶片設計之驗證與測試技術開發研究(III)
Verification and Testing Technology Exploitation for IP-Based SOC Design(III)

計畫編號：NSC 91-2215-E-009-078

執行期限：2002 年 8 月 1 日至 2003 年 7 月 31 日

主持人：李崇仁教授　交通大學電子工程系
共同主持人：董蘭榮教授　交通大學電機與控制工程系
陳竹一教授　中華大學電機系

一、中文摘要

以系統晶片來實現複雜的系統已成為積體電路設計的主要趨勢。系統晶片的設計一方面要利用強大計算機輔助設計整合多個智財(IP)單元於單一的系統晶片上，另一方面要驗證設計結果以符合系統要求。為達成後者目的需要有強大有效之驗證測試系統。本研究團隊基於多年研究積體電路驗證測試技術的經驗提出此計畫以開發出完整的系統晶片驗證測試技術。

本計劃第三執行年度分成三子計劃，分別為：(1)於組織探索階段互動之系統階層驗證技術；(2)以智財為基系統晶片設計之測試技術研究；與(3)系統晶片矽晶偵錯之良率提昇。分別於系統階層驗證、IP 單元測試、與元件偵錯三層面上發展驗證、測試、偵錯與良率提昇技術，以減少再設計週期。

關鍵詞：系統晶片、驗證、測試、偵錯、超大型積體電路/計算機輔助設計、良率

Abstract

To use an SOC (System-On-a-Chip) realize a complex system has become the main trend for today's IC design. To design an SOC, in one hand, it needs to have a powerful CAD system to incorporate many IP's into one single chip; in the other hand, it needs to verify the designed system and test the finally fabricated chip to guarantee its proper function and performance. To achieve the latter goal, it needs to have a powerful and effective verification, testing and debug system. In view of this, this integrated joint project is proposed to investigate the verification, testing and diagnostic technology for the SOC design.

The project, to be carried out in three year period, has three sub-projects in the third year, which are : (1) system-level verification interacting with architecture exploration; (2) Testing technology development for IP-based SOC design; and (4) SOC silicon diagnostics and yield improvement. It is dedicated to investigate the verification, testing and debug techniques at three levels, i.e., system level, IP-level and silicon wafer debug of SOC design.

Keywords: SOC, Verification, Testing, Diagnosis, VLSI/CAD, Yield

二、緣由與目的

系統晶片的設計一方面要整合多個智財(IP)單元於單一的系統晶片上，另一方面要驗證設計結果以符合系統要求。合成智財單元與整合系統晶片的過程繁複已屬不易，而要確認該系統晶片製造完成後，是否能正確地運作則是更大的挑戰。目前學術及產業界大多投入於系統晶片的開發設計上，對於系統晶片的驗證測試技術則著墨不多。鑑於此，本研究團隊提出此計畫以開發出完整的系統晶片驗證測試技術。

系統晶片設計通常採用由上而下的

流程，分為 System-Level Design，Circuit-Level Design 以及 Manufacturing，在每一層次設計均產生 intermediate 設計結果供下一層次之設計使用。在每進入下一個層次之前，必須先確認設計結果之正確性與其之可測試性。我們所提出一套結合設計流程的驗證程序，分階段地：即 System level, Circuit level 及 Manufacturing level 完成系統晶片的驗證工作及產生測試偵錯圖樣(test and diagnostic patterns)。

第一階段主要是由第一子計畫執行，其主要工作是成本評估、效能模型、軟硬體共模擬。此計畫首先就耗電功率、面積、延遲時間三項因素來評估系統之組織成本。根據與系統組織配置的設計階段互動，一方面驗證該組織是否符合系統要求、一方面提供組織配置的設計參考。此步驟完成後，再在效能抽像階層上模擬候選組織。在此階層的模型不強調實際的資料值而僅考慮系統內的資料流動。因此，由於模型複雜度的簡化縮短模擬時間。而設計者依據時間性效能的模擬結果驗證候選組織並進而改善設計。完成此二步驟後，軟硬體共模擬開始就包含軟、硬體元件的異質組織實施模擬以驗證系統晶片行為結果。至此，系統階層驗證便告完成。此時將再進行下列階段 Circuit-level 之驗證。

第二階段主要是由第二子計畫執行。於 SOC 設計過程中, 除各層次之設計驗證外，為保證系統晶片製造出來時，無因製程缺陷等因素而發生不能工作情況，必須加入可測試性設計之考慮, 並對各 IP 產生其測試與偵錯圖樣。晶片測試，長久以來即是一困難問題。於系統晶片設計中，由於晶片之規模是更大而複雜，且其中許多 IP，皆是由不同公司或設計者提供，所設計出來之晶片測試問題更是嚴重。又未來之系統晶片，必是屬混合信號(mixed-signal)，其製造技術亦必是以深次微米為主之技術，其信號傳輸是以奈秒(nano-seconds)(甚至以下)為單位。對於此種晶片，有一些新的現象，如：信號於 interconnection wires 傳輸所花費時間將超過於 MOSFET 電晶體傳輸所花費時間，interconnection wires 間之信號干擾現象嚴重，MOSFET 漏電流增大等，晶片測試需要有新的考量。
故第二子計畫：在下列數方向對 SOC 晶片測試之諸問題，作一研究：(1) 信號傳輸線之信號傳輸完整性與測試研究; (2) 類比智財之測試與診斷；(3) 一個應用於 DAC 測試之高度線性 VCO 電路; (4) 一測試藕合障礙之內建式自我測試線路; (5) 液晶顯示器推動線路 IC 之測試。

於第三晶片製造階段, 由於製程初始之 immature tuning，所生產之晶片良率必低，或於晶片測試時發現晶片不符規格，必須經由晶片偵錯，甚或設計偵錯，發現原因，而提升晶片生產良率。此時甚或需全面檢討晶片設計，以求達到最符經濟效率的測試與晶圓良率，此階段工作係由第三子計畫執行。其於矽晶片製造完成後，就其測試資料，即 wafer map，尋求設計、測試與製造流程之缺失，並藉統計理論分析良率以增進晶片良率與提升晶片品質。另外亦欲以系統分析方式研究系統晶片之整個設計、測試與製造的流程，以改進晶片良率與提升晶片品質。最後此子計畫更擬研究系統晶片之 Test Economics, 希望能建構一軟體系統，考量各 IP 特性與測試機之規格與限制，對一系統晶片之測試成本效益能有一預估並做最佳化。

由上所述可知，各子計畫於本整合計畫各佔地位且環環相扣，互為幫補。計畫之完成將對國內 SOC 驗證及測試技術之提升有幫助。

三、結果與討論

A. System-level verification interacting with architecture exploration:

The co-simulation engine is based on a high-level model describing the interactions of an IP with the rest of the system, and a multi-layered wrapping scheme of an IP core. Using the interaction models and the

wrapping scheme, it allows plug-and-play IP integration and validation, and heterogeneous co-simulation.

Several issues must be considered when integrating an IP core. One paramount issue is the intended interaction of the foreign IP with the rest of the system. We describe such knowledge in a high-level model that forms the basis for the synthesis of the IP-specific interfaces to the rest of the system. Consider for example the high-level model of a master/slave interaction depicted in Figure 8.a. Here, both the master and the slave are Intellectual Property cores. In the context of Figure 1, the master is the DSP processor, and the slave is one of the ASICs.

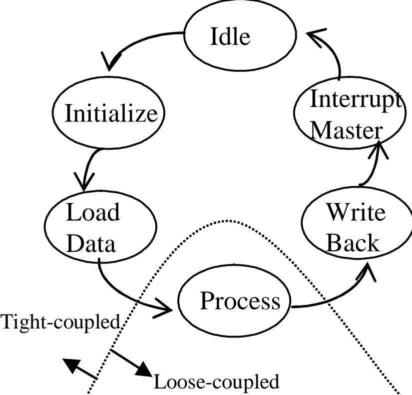

Fig.1 Master/Slave Interaction

An example scenario of a master/slave interaction, as shown in Fig.1, is as follows. Initially, the slave is in an "IDLE" state, waiting for orders from its master. It then moves to an "Initialization" state triggered by the master. During that state, the master is in charge of initializing its slave. Typically, the master will reset the IP core, and write into the register file of the slave to set the necessary information for the execution and completion of the allocated task. For instance, the master can set the pointers to the program and data memories of the slave. It also sets other core-specific information such as the mode of operation. During the following state, the master will initialize the DMA to write the block of data (to be processed) to the local memory of the slave. Finally, when the data is transferred, the master supplies a "go" signal to its slave, triggering it to move to a "Process" state. During that state, the interaction between the master and the slave becomes loose (that is no lock-step simulation is needed). Upon completion of the execution of the allocated task, the slave gets into a "Write Back" state, during which the results are written back to the global memory. The slave then interrupts its master, informing it of the completion of the task. It then moves back to the original "IDLE" state where it waits for new orders from its master.

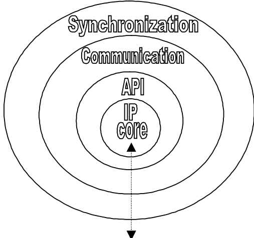

Fig.2 Integration layers of an IP core

Consider the IP model shown in Fig.2. The IP core is wrapped with three layers: the API layer, the communication layer, and the synchronization layer. Such a multi-layered model allows a seamless integration of IP cores of different origins and in different forms. Typically, each IP can be accompanied by its own different set of verification and modeling tools. Such tools include HDL models, Instruction Set Simulators (ISS), C models, and emulator boards. These vary in speed, accuracy, and level of abstraction, and they are often used interchangeably during the design cycle. The goal of our multi-layered wrapping scheme is

to allow IP-based system integrators to use IP cores in a plug-and-play fashion, and integrate and reuse different IP models interchangeably.

The IP reuse technology described in this paper is being used successfully in real industrial environments. It is proving to be an efficient and fast way to run heterogeneous co-simulation, and quickly incorporate foreign IP cores into embedded systems. Substantial productivity gains and design-time reductions have resulted from its use. In a high-density central site modem (HDCSM) application, we have been able to wrap several in-house IP cores and set up a heterogeneous co-simulation system platform in less than two weeks. This includes the development of the API functions for the IP cores, and the interaction models with the system. We have developed and tested the heterogeneous co-simulation IP models with little knowledge about the cores themselves. Applying different speedup techniques, we have been able to accelerate the heterogeneous system co-simulation substantially (often by three orders of magnitude). For example, we have been able to speed up the system simulation of the HDCSM application from three instructions per second (RTL) to 1600 instructions per second. Thus far, the IP-based synthesis technology is only partially automated. The communication layer and the client/server interfaces are generated automatically. However, the designer's assistance is needed to define the interaction model, and the API functions. Figure 3 illustrates analysis environment using the proposed co-simulation engine.

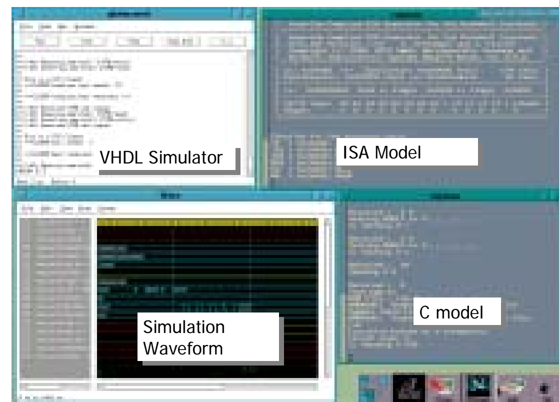

Fig. 3 HW/SW co-simulation environment

B. Testing technology development for IP-based SOC design:

For the third year of the sub-project, there are five topics under investigation. For all the topics, significant progress has been obtained and some of results are being or have been written into papers for publication:

2.1

(1) Signal integrity study and test generation:

For this topic, we have studied the relationship between glitches and induced-delays of crosstalk faults for the deep submicron interconnection lines. A unified test scheme is proposed and demonstrated to test both types of crosstalk faults.

(2) Analog IP testing and diagnoses:

For this topic, we have developed an on-chip jitter measurement circuit for clock signals in an SOC chip. The circuit can measure clock jitter up to a resolution of 49.3 ps and can be embedded into SOC as a BIST circuit.

(3) A highly linear VCO for DAC testing:

For this sub-topic, we have developed a highly linear VCO which can be used as the signal generator for DAC testing. It is simple, has a prevision up to 9 bits and can be incorporated into an SOC chip.

(4) A BIST circuit for testing crosstalk faults:

For this topic, we have developed a BIST circuit which can be incorporated into the boundary so an environment to test crosstalk – induced glitch faults for deep submicron circuits. For this circuit, a simple logic symbol is proposed to model the crosstalk effect and this makes test generation simple.

(5) Testing of TFT LCD source driver IC:

For this topic, we have classified fault models according to special features of the TFT LCD source driver circuit and developed simplified test set to improve test efficiency. In addition, we have also adopted a stress test methodology to improve the reliability of the IC.

(C) **SOC silicon diagnostics and yield improvement:**

於本年計畫達成規劃書所列的目標之五項工作，分述於下：

(1) **互補式金氧半電晶體不匹配及電路效能評估之相關性分析**

電路模擬時，電晶體參數在製程上的變動須做考量外，元件參數彼此間相關性的考量亦不容忽略，本報告之中，主要在探討電晶體參數的相關性，以及參數彼此間的關係。傳統在做電路的容忍度分析模擬時，將變動變數視為彼此獨立之變數，由於電晶體彼此間的參數變動是有所關聯性，所以我們提出一個模擬方法，在做電路容忍度分析時，加入相關性的探討，分析類比電路效能的表現。

(2) **一個適於變異製程的疊代良率評估**

本篇報告是一個適於變異製程的疊代良率評估，假設產品為常態分佈特性之結合，對於數位IC測試其良率與品質做出評估，進而預估在固定品質下其產品良率的走勢，本論文推導出變異製程之產品製造後分佈方程式，對於未來工業界將面臨測試上的問題，提供一個新的觀點，進一步將它系統結構化，以便我們預測數位產品進步曲線，及其相對之良率品質。

(3)**激突分析和週期性激突識別的實現**

本篇報告我們提出Jitter在時域上的分解方法，藉著長條圖尾部曲線的擬合，我們可以分解 Jitter 為兩部分 ：隨機性和決定性 Jitter，並且，估量它們對電路的影響。我們也用累計時分析去找出Periodic Jitter 的症狀，提供了有效的觀察點，可以對時序電路快速的分析，去消除設計不良所產生的 Jitter。

(4) **連續參考值產生器之空間相關分析**

本篇報告是以相關性為考量，假設元件與元件之間是有相關性的，採用連續參考值產生器的電路架構，並引進元件彼此之間相關性。利用元件在空間上的排列方式，改善電路的線性度。我們推論出有規則性的一維排列方式，不但可以改善電路的線性度，並可以抑制梯度誤差。當元件的匹配性不高時，採用本篇論文提出的電阻二維排列方式，可以獲得較好的線性度。

在未來類比積體電路中，元件參數的匹配特性將會越來越重要。本報告採用相關性的亂數，探討元件參數在空間上的匹配特性，並且利用電阻在二維空間上的排列，使電路的積分非線性誤差維持在較小的範圍之內。

(5)**晶圓圖分析的應用對於良率的影響**

本報告主要是從眾多的半導體產業公司和學術機構中，調查和研究有關晶圓圖、晶圓缺陷、晶圓錯誤、積體電路在操作時所產生的問題或症狀…等等，作一整體性的資料蒐集、整理、分析，並加以描述和呈現這些觀點，對於整個半導體製程的影響，最終能將這些現象的資料彙整作為晶圓製造的索引，藉由運用其資料的結果能使半導體製程得到良率的提升。

四、計畫成果自評

子計畫一：本計畫第三年成功建立軟硬體共模擬環境，可有助於組織探索階段完成軟硬體互動之驗證工作。此技術已應用於各種有線通信及多媒體 SOC 設計上。本計畫之研究成果已發表兩篇國際會議論文[1-2]與一篇國內會議論文。另外，部分研究成果正投稿于 IEEE 期刊。

經由本計畫之執行已培養四名碩士畢業生。該四名碩士畢業生目前服務於系統晶片相關之高科技企業。

子計畫二：本計畫於第一年已建立智財單元本身與相互間連線的測試機制，在第二年的期間也順利地分別對數位、類比與混合訊號電智財單元提出有效的測試與診斷的架構與方法，相信將有助於後續計劃之執行。於第三年期間對上述各課題有更深入之研究並提出了解決方法。大部分的研究成果皆符合吾人原提計劃，完成度應達 80%以上，且部分成果已或將發表於國際會議或期刊[4-7]，或碩士論文中[8-11]。

子計畫三：本計畫研究內容與原計畫目標相符，尤其是在類良率模型的建立，以此模型所做的良率評估，可使吾人分段模擬，其結果幾乎與不分段一致；另外對於不同規格參數轉換的探討，不僅可用於設計時做最佳化之指引(尤其是高靈敏度電路如:高速數位電路、類比電路、高頻電路)，亦可用於測試圖樣產生時最佳測試參數選取以及測試圖樣減少的指引，亦可用於晶片測試時做為晶片診斷的指引。是以本計畫在這一年度的工作中，獲得豐碩的成果，亦在許多項目上值得繼續延伸。

五、參考文獻

[1] Hsien-Wen Cheng and Lan-Rong Dung, 2002, “EFBLA: A Two-phase matching algorithm for FAST motion estimation,” PCM 2002 .

[2] Hsien-Wen Cheng and Lan-Rong Dung, 2003, “A Novel Vario-Power Architecture of Motion Estimation Using a Content-based Subsample Algorithm,” SiPS 2003.

[3] Hsien-Wen Cheng and Lan-Rong Dung, 2003, “A Power-Aware Architecture for Motion Estimation,” the 14th VLSI/CAD 2003.

[4] S. M. Lee, C. L. Lee, and J.E. Chen, “Fault Effects and Detection for Inteconnection Bus Crosstalk Faults in Deep Submicron VLSI”, submitted to ISCAS 2004.

[5] Ching Cheng Tsai, and Chung Len Lee, “An On-Chip Jitter Measurement Circuit for PLL”, presented at ATS 2003.

[6] Ja Hou Yang, and Chung Len Lee, “A Highly Linear VCO”, to be submitted to Electronics Letters.

[7] Ming Shair Wu, C. L. Lee and J. E Chen, “A BIST Scheme for Testing Crosstalk Faults Based on Oscillation Signal in Boundary Scan Environment for Deep Submicron VLSI”, submitted to IEEE Design and Test.

[8] Tsui Ching Chiu, “TFT LCD Source Driver IC Testing – Fault Model and Test Generation”, M. S. Thesis, Department of E.E., NCTU. 2002

[9] Tseng Yin Yang, “TFT LCD Source Driver IC Testing – Fault Coverage Improvement and Early Failure Rate Reduction”, M.S. Thesis, Department of E.E., NCTU, 2002.

[10] Ching Cheng Tsai, “An On-Chip Jitter Measurement Circuit for PLL”, M.S. Thesis, Department of E.E., NCTU, 2002.

[11] Ja Hou Yang “A Highly Linear CMOS VCO”, M.S. Thesis, Department of E.E., NCTU, 2002.