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蕭特基能障 SOI 金氧半電晶體元件研製與分析(II)

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計畫主持人：黃調元

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蕭特基能障金氧半電晶體元件研製與理論分析－子計畫二:

蕭特基能障 SOI 金氧半電晶體元件研製與分析(II)

Fabrication and Characterization of SOI Schottky Barrier MOSFET (II)

計畫編號：NSC 91-2215-E-009-042

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1、摘要

在本篇論文中，我們提出並驗證了一種新結構的奈米元件，此一元件是以 Fin 結構為基礎而製作於 SOI 晶片上，更結合了以金屬矽化物形成之源/汲極和電場感應出的源/汲極延伸區為其主要特色。此元件是以金屬矽化物代替高摻雜的半導體作為源/汲極之用，使得其在製程上較為簡單且製程溫度較低。然而傳統的蕭特基源/汲極元件由於金屬與半導體接面在汲極為高電場下易產生場發射的漏電流機制，造成其具有較大之漏電流而大大地降低其開/關之電流比，也因此扼殺了蕭特基電晶體的實用性。然而在這新元件中加上的汲極延伸結構能完全地抑制此一漏電流機制，且元件導通電流亦隨著延伸區電壓加大而增大，完全地改善了傳統蕭特基源/汲極元件的缺點。從量測中，我們在同一元件中得到兩種模式(n 通道及 p 通道)操作下的開/關電流比都接近於 10^9，且因 Fin 結構的作用， 亦獲得了接近物理極限的次起始斜率(subthreshold slope)值，即趨近於 60mV/decade。

Abstract

In this thesis, we proposed and demonstrated a novel nano-scale silicon-on-insulator (SOI) FinFET device. The new device features a metallic silicided source/drain and field-induced S/D extensions. Schottky barrier (SB) MOSFETs generally enjoy simpler and low-temperature processing compared to conventional MOS transistors by employing metallic silicide, in lieu of heavily-doped region, as the source/drain. However, conventional Schottky barrier (SB) MOSFETs were known to suffer from intolerantly high leakage current caused by the field emission of carriers from the drain junction. The high leakage severely degrades the on-/off-state current ratio and essentially rules out their applications to mainstream integrated circuits. In our new device, this problem was effectively solved by the formation of an electrical drain junction which was induced by the sub-gate bias, $V_{G,sub}$. Excellent subthreshold characteristics with high on-/off-state current ratio (close to or higher than 10^9) and near-ideal subthreshold slope (~ 60 mV/decade) are realized, for the first time, on a single device.

Keywords: *SOI, Schottky barrier, field-induced drain (FID), On/Off current ratio, FinFET*

2、Introduction

As the complementary metal oxide semiconductor (CMOS) transistors' feature size is scaled down to below 0.1 μm, the challenges to overcome the short channel effect (SCE) and dopant fluctuation effect become more and more difficult [1]. To relax these constraints, some advanced structures, such as FinFETs [2], ultra-thin body SOI [3], and silicided source/drain SOI [4], have been proposed.

Specifically, FinFETs belong to the family of double-gate (DG) silicon-on-insulator (SOI) transistors, in which two gates are employed to control the channel carrier charges. FinFETs thus exhibit attractive advantages in comparison with the conventional bulk MOS or single-gate SOI counterparts. The device displays high transconductance, nearly ideal subthreshold swing, improved current drive capability, and lower direct-tunneling gate leakage current. Moreover, the double-gates structure provides better controllability of the drain electrostatic field lines, thus minimizes drain-induced barrier lowering (DIBL) and threshold variation with channel length [5]~[9]. As a result, DG MOSFET offers the potential for scaling the channel

length down to the 10 nm [7][10].

Particular attention is called for on the parasitic series resistance in the source/drain regions of SOI FinFET devices, since it would increase significantly as the fin width is scaled down. One approach for reducing the source/drain series resistance is to employ the salicide materials. For nano-scale FinFET device, Schottky barrier source/drain formed by low-resistivity silicide represents a promising alternative to the heavily doped source/drain due to the low S/D series resistance and simpler fabrication process. The good behavior in short-channel effect control owing to the inherently sharp silicon/silicide interface is another merit for adopting Schottky junction in nano device applications [11].

3、Fabrication

The proposed SOI FinFET device employed silicided Schottky-barrier source/drain and field-induced source/drain extensions. 6-inch p-type SIMOX wafers with background doping of around 5 x 10^{15} cm^{-3} were used as the starting wafers. The active Si device layer was thinned down to 80nm by thermal oxidation. E-beam system applied to pattern the fin width. A vertical furnace was employed to grow gate oxide (2.2 nm) and subsequently deposit the phosphorous-doped polysilicon gate in clustered chambers. E-beam system and high selectivity RIE were employed to define and etch the gate length, respectively. Then, depositing LP-TEOS and etching to define different offset length. Co silicide was formed to as Schottky source/drain. Figures 1 are SEM pictures for those shown a top view of the devices' central portion before the silicidation step.

4、Results and Discussion

As mentioned previously, conventional SB-MOSFETs suffer from intolerantly high off-state leakage current owing to the field-emission carriers injecting from the drain side. In our new device, the fin structure combining with field-induced extensions could effectively suppress the off-state leakage current while retaining the on-state current. As a result, extremely high on-/off-state current ratio can be obtained.

Figure 2 shows the ambipolar characteristics of a device with channel length = 470 nm, fin width = 50 nm, and offset length = 100nm. Sub-gate bias is fixed at 7.5V for n-channel operation, and -7.5V for p-channel operation. The sub-gate bias voltages are chosen so that they are high enough to sufficiently improve the on-/off-state current ratio while low enough so that it would not degrade the reliability of the dielectric underneath the sub-gate plate. Our experimental results show that extremely high on-/off-state current ratios (>10^9 and >10^8 for p- and n-channel operation, respectively) are obtained on a single device. The subthreshold slop is 60.6mV/decade for n-channel operation, and 60.8mV/decade for p-channel operation at room temperature. These values are close to the ideal case, e.g., 60mV/decade. Almost identical results are also observed in the self-aligned counterpart, except for the slightly larger off-state leakage current, as shown in Fig. 3. The subthreshold swings of 61.1mV/decade for n-channel operation and 61.2mV/decade for p-channel operation are realized. The on-/off-state current ratios are still higher than 10^8 for both n- and p-channel operations. To the best of our knowledge, such superior ambipolar characteristics on a single device have never been achieved before.

When the fin width is increased to 2 μm, as shown in Fig. 4, the subthreshold slopes increase to around 66 and 67mV/decade for n- and p-channel modes, respectively. In addition, drain-induced barrier lowering (DIBL) effect (~ 40 mV) becomes visible. This trend is further highlighted in Fig. 5, in which the subthreshold slope is shown as a function

of fin width. It can be seen that the subthreshold slope increases with increasing fin width, consistent with the trend previously reported on MOS FinFET devices [12]. The corresponding characteristics in self-aligned devices are shown in Fig. 6. These results indicate that, when the fin is scaled into the nano-meter region, the channel is easier to be depleted and the ultra-thin body of the FinFET would effectively prevent the source/drain punch-through.

Moreover, the simple process of SB FinFET device makes it feasible to achieve larger effective channel width by increasing the number of Si fins, to further increase the drive current. Figure 7 depicts the drive current of two devices with 470 nm channel length and 50 nm fin width for p-channel operation. The 3-fins device conducts three times the current of a single-fin device. The same result is also derived on n-channel operation, as shown in Fig. 8. It is thus expected that, if closely spaced Si fins can be fabricated with an advanced lithography tool, the SB FinFET device can be used to fabricate ultrahigh-density integrated circuits.

5、Conclusion

In this work, a novel nano-scale SB FinFET device is fabricated and characterized. Extremely low off-state leakage current is achieved by using a fie[illegible] Excell
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subthreshold swing (~ 60 mV/dec.) and high on/off current ratio (close to or higher than 10^9) are demonstrated, for the first time, on a single device.

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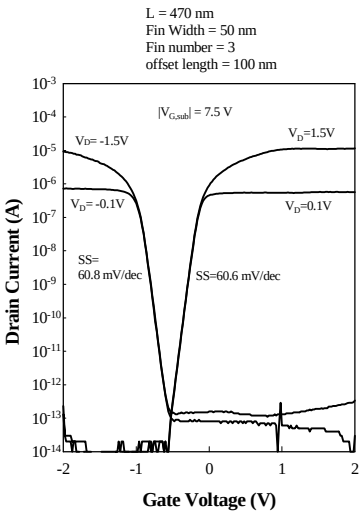

Figure 2 Ambipolar subthreshold characteristics of a device with 100 nm offset length. Near-ideal subthreshold slop (SS) is observed.

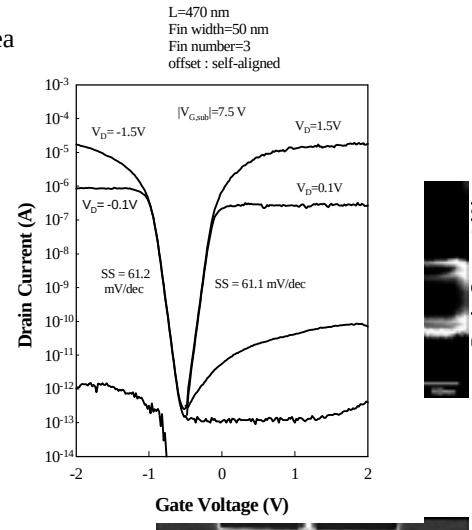

Figure 3 Ambipolar subthreshold characteristics of a device having self-aligned offset.

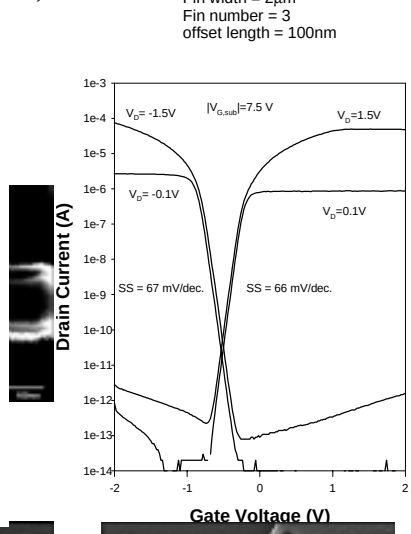

Figure 4 Ambipolar subthreshold characteristics of a device with 100 nm offset length and fin width of 2