行政院國家科學委員會專題研究計畫　成果報告

低溫快速金屬誘發非晶矽結晶化製作複晶矽薄膜電晶體

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計畫主持人：馮明憲
共同主持人：吳耀銓
計畫參與人員：趙志偉　施協志

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行政院國家科學委員會補助專題研究計畫成果報告

低溫快速金屬誘發非晶矽結晶化製作複晶矽薄膜電晶體

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計畫主持人：馮明憲
共同主持人：
計畫參與人員： 趙志偉 施協志

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<u>中文摘要</u>

Abstract

Compared with conventional solid phase crystallized (SPC) thin-film transistors (TFTs), metal-induced laterally crystallized (MILC) TFTs exhibit significantly enhanced performance. Metal films are usually deposited by the physical vapor deposition (PVD) method, which is time-consuming and expensive in terms of equipment cost. In this work, a simpler electroless plating Ni was introduced to replace PVD Ni. It was found that the morphologies and the device characteristics of Ni-induced lateral crystallization TFT were as good as those of PVD Ni-induced lateral crystallization TFT.

Low

一 前言:

低溫複晶矽薄膜電晶體（Low Temperature Poly-Silicon；LTPS）是新一代薄膜電晶體液晶顯示器（TFT LCD）的製造流程。隨著高畫質以及低耗電量的要求傳統之非晶矽薄膜電晶體(amorphous silicon) 電特性無法符合此一要求，因此發展複晶矽薄膜電晶體製作技術，由於複晶矽薄膜電晶體擁有較高的電子遷移率，所以能夠同時符合這兩項要求。然而若以傳統複晶矽製作方式其製程溫度皆高於玻璃基板軟化溫度(600℃)並不適用於 LCD 面板製作，所以許多研究相繼投入低溫複晶矽薄膜製作研究，目前在現有技術中以準分子雷射退火製作複晶矽薄膜的技術最為成熟但仍有均勻性差、設備昂貴等缺點所以相繼有新的技術被提出其中以金屬誘發非晶矽結晶化/金屬誘發側向非晶矽結晶化(metal induced crystallization of amorphous silicon/ metal induced lateral crystallization of amorphous silicon ;MIC/MILC)的技術最為突出，MIC/MILC 的技術能夠得到均勻性佳的複晶矽薄膜而且設備較便宜；除此之外利用 MIC/MILC 技術所製作出的複晶矽薄膜是由單一平面方向的矽晶粒，所以 MIC/MILC 技術所製作出的複晶矽薄膜用來製作薄膜電晶體能夠擁有極佳的電性。

在 MIC/MILC 製程中，傳統上是利用物理氣相沉積鎳金屬薄膜作誘發非晶矽結晶化之觸媒層。

二 研究目的:

根據文獻指出 MIC/MILC 複晶矽薄膜利用準分子雷射退火後能夠同時擁有高品質及性質均勻之複晶矽薄膜，此一為新技術並且具有量產化之可能，所以本計劃跟據文獻中所提之製程實際作薄膜電晶體元件建立起元件參數，可以將此項技術轉移給廠商，此外文獻本身對於其結晶化成長機制並無做完整之討論，這對於實際元件製作上會對於元件特性造成不穩定的變數。所以本計劃主要目的有二:第一根據文獻實際製作元件並且建立起元件製作參數，第二建立準分子雷射輔助金屬誘發非晶矽結晶化薄膜結晶化機制。

三 文獻探討:

The polycrystalline silicon (poly-Si) TFT has attracted considerable attention for active matrix liquid crystal displays (AMLCD) application due to its good electrical properties and capability of integrating peripheral circuits on inexpensive glass substrates. Intensive studies have been carried out to lower the crystallization temperature of amorphous Si (a-Si). Metal-induced crystallization of *a*-Si is one of these efforts. A thin metal layer was deposited on the top of an a-Si film, which was followed by crystallization at a temperature lower than 600℃. The metal film (Ni[1-4], Pd[5] or Al[6]) is usually deposited by the PVD method, which is time-consuming and expensive in terms of equipment cost.

To replace PVD, an electroless plating Ni method was proposed in our previous study.[7] Since there is no vacuum process involved, the plating method is much simpler, faster, and cheaper than the traditional PVD method. After samples were annealed, needlelike poly-Si grains were observed. In this study, the morphologies and the device characteristics of these needlelike grains were measured. For comparison, the morphologies and the device characteristics of SPC and PVD Ni-induced crystallization TFTs were also measured.

2. Experiment

Silicon (100) wafers were used as the substrates in this study. After 500-nm-thick wet oxide layers were grown on the wafers, a 100 nm silane-based *a*-Si film was deposited by low-pressure chemical vapor deposition (LPCVD). The deposition pressure and temperature were 100 mTorr and 550℃, respectively. After the a-Si deposition, wafers were etched for 10 s in diluted HF solution (H_2O:HF=1:100), and then washed with DI water.

Four methods were employed to induce the crystallization of a-Si films. The details of these processes are described in the following section and summarized in Table I.

(a) EPIC (electroless plating Ni-induced crystallization) poly-Si films: Samples were dipped into the plating solution for 5 min. As shown in Fig. 1, Ni clusters were uniformly distributed on the top of a-Si films. Samples were then annealed in an nitrogen atmosphere at 550℃ for 6 h to crystallize the Si films.

(b) EPILC (electroless plating Ni-induced lateral crystallization) poly-Si films: Ni films were selectively deposited on the source and drain areas of TFT by the electroless plating method. The photoresist was first patterned to form the desired Ni features, and then samples were dipped into the plating bath for 15 min. The SEM image of Ni film (bright area) on the a-Si is shown in Fig.2. Samples were then annealed at 550℃ for 6 h.

(c) PVDILC (PVD Ni-induced lateral crystallization) poly-Si films: A photoresist was also patterned to form the desired Ni features, and then a 100-Å-thick Ni film was deposited on a-Si by the sputtering method. Samples were subsequently annealed at 550℃ for 6 h.

(d) SPC poly-Si films: No Ni was coated on the a-Si. The Si films were annealed at 600℃ for 24 h.

After annealing, all Ni-coated Si films were dipped into HCl solution to remove Ni residues. The TFTs were then fabricated by defining the active areas on all four types of poly-Si films. A 100-nm-thick SiO_2 film for gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD). Subsequently, a 200-nm-thick SiH_4-based *a*-Si film was deposited at 550°C by the LPCVD system and lithographically patterned as gates. The gate electrode and source/drain were doped by self-aligned phosphorus implantation at a dose of 5×10^{15} ions/cm^2. Then dopant activation and crystallization of *a*-Si gate electrodes were performed at 550℃ for 9 h in N_2 ambient. A 500-nm-thick silicon oxide film was used as the passivation layer. A 500 nm Al film for interconnection was formed after the contact holes were opened. Finally, the hydrogen plasma treatment was performed after TFTs were fabricated.

3. Results and Discussion

The results of this study will be discussed with regard to the morphologies and the device characteristics of the four poly-Si films.

A. Poly-Si Morphology

a. EPIC

In the EPIC method, the Ni clusters were sparsely distributed on the a-Si film (Fig. 1). The diameter of each Ni cluster was about 300 nm. Every cluster was a site to induce crystallization of a-Si. As shown in Fig. 3, after samples were annealed for 6 h, most of the a-Si was crystallized to needlelike poly-Si. The width of the needlelike grains was about 30 nm and the length was several microns. Most of the angles between the needlelike poly-Si were about 70.5°. Similar angles have been reported by Hayzelden and Batstone,[8)] who studied the nucleation and growth mechanism of isolated nickel silicide precipitates in Ni-implanted amorphous Si and the subsequent silicide-mediated crystallization of a-Si. They found that the crystallization of silicon proceeded via the migration of the nickel silicide through the a-Si. This resulted in epitaxial growth of Si constrained to < 111> directions. Since the angle between two <111> directions is 70.5°, the angle between the poly-Si grains is also 70.5°.

b. EPILC and PVDILC

In the EPILC and PVDILC methods, Ni was only deposited on the source and drain areas of TFTs. After 6 h of annealing, the channel between source and drain was fully crystallized. In order to have a clear view of the growth of the poly-Si, an image of Si film was taken after annealing at 550℃for 2 h. After Secco etching[9)], two regions were found on the EPILC: (1) Ni island and (2) needlelike poly-Si grains at the

periphery of the island, as shown in Fig. 4. The same morphologies were also found on the PVDILC sample. The growth rate of PVDILC poly-Si was about 2.5 μ m/h, which was a little higher than that of EPILC (2.15μm/h).

Similar needlelike grains at the periphery of the Ni islands have been reported by Jin *et al.*[10] who induced lateral crystallization of a-Si by depositing 5-nm-thick Ni islands on the top of a-Si thin film. After the samples were annealed, they found that the growth direction of needle poly-Si was perpendicular to the periphery of the Ni islands. This is because, at the edges of a Ni island, many of the $NiSi_2$ nodules moved laterally into the a-Si region and any a-Si along the path would be crystallized. As the crystallization occurred, any slow moving nodules would be quickly trapped within a short distance from the edges of the Ni-covered region, leaving only the fast moving nodules at the crystallization front.

c. SPC

SPC poly-Si had a columnar grain structure with grain boundaries randomly oriented.[11] The maximum grain size was about 500 nm.

B. Device Characterization

For each of the four types of poly-Si thin films, thirty devices were randomly chosen for measurement. After analysis, within each group, the devices were found to possess very consistent characteristics. However, the characteristics of each of the four groups were very distinct from the others. Figure 5 and Table II show the different device characteristics of the four types of poly-Si films. The performance of the EPILC-TFT was almost the same as that of PVDILC-TFT. Their performance was far superior to that of the

SPC-TFT, which had the lowest mobility (μ), largest subthreshold slope (S), and highest V_t among the four TFTs.

In a previous study, Bhat *et al.*[11] also found that PVDILC-TFTs exhibit significantly enhanced performance compared with SPC-TFTs. This was because due to the fact that SPC poly-Si had a columnar grain structure with grain boundaries randomly oriented with respect to the direction of drain current (I_d) shown in the Fig. 6(a).[11] These grain boundaries trapped charge carriers and built up potential barriers to the flow of carriers. The presence of these grain boundaries degraded μ, S and V_t. Fortunately, this degradation could be improved by using PVDILC poly-Si because its longitudinal grains and their boundaries were largely parallel to I_d hence less impeding to carrier flow. Therefore, PVDILC had lower V_t, smaller S, higher μ, and higher on-current.

In this study, the poly-Si grains of EPILC and PVDILC were also induced by lateral crystallization of a-Si. They both had longitudinal grains parallel to I_d, as illustrated in Fig. 6(c). Therefore, they had lower V_t, smaller S, higher μ, faster turn-on, and higher on-current, as shown in Fig. 5 and Table II. In other words, this simple electroless plating method can replace the PVD method in the Ni-induced lateral crystallization of a-Si. As for the EPIC-TFT, the longitudinal grain structure was still present but with grain boundaries randomly oriented with respect to the direction of I_d, as shown in Fig. 6(b). Therefore, the performance of EPIC-TFT was better than that of SPC-TFT but not as good as those of EPILC-TFT and PVDILC-TFT. Besides, in contrast to the other three TFTs, the EPIC-TFT had a negative threshold voltage of -3.0 V. To investigate the cause of this phenomenon, SIMS analysis was employed. The analysis revealed lots of phosphor impurities in the EPIC poly-Si films, which are due to the fact that the electroless plating Ni contained about 10% phosphor.[12] Since the phosphor atoms in the channel of EPIC

poly-Si TFT were the donor ions, the threshold voltage was shifted to negative value.

In addition, Fig. 5 and Table II indicate that EPILC-TFT and PVDILC-TFT have similar levels of leakage current, which are higher than that of SPC-TFT but lower than that of EPIC-TFT. This is because the grain boundaries would trap Ni or $NiSi_2$ precipitates, and enhance the leakage current.[10-11, 13-14] Since SPC devices did not have the Ni contamination problem, obviously, SPC-TFT had the lowest leakage current. On the other hand, as shown in Fig. 6(b), EPIC-TFT has randomly oriented needlelike grains along the channel. Due to the highest density of trapped Ni or $NiSi_2$ along the active channel, EPIC devices had the highest leakage current.

4. **Conclusions**

In summary, an investigation of the device characteristics of poly-Si TFT fabricated by electroless plating Ni-induced lateral crystallization (EPILC) of a-Si has led to the development of a simple, fast and inexpensive process for preparing poly-Si films. It was found that the morphologies and the device characteristics of EPILC-TFT were as good as those of PVDILC-TFT.在早期最常用的方式為固相結晶法(solid phase crystallization, SPC)[1-2]其做法是將非晶矽薄膜置於爐管內退火，退火溫度為 600°C退火時間為數十個小時才能得到完全結晶化的複晶矽薄膜。SPC 的方法既耗時而爐溫又高，玻璃基材很容易在這高溫長時間的退火製程下發生熱變形。所以許多研究開始致力於降低退火溫度及退火時間；其中以金屬誘發非晶矽結晶化(Metal Induced Crystallization of amorphous silicon, MIC)以及金屬誘發側向非晶矽結晶化(Metal Induced Lateral Crystallization of amorphous silicon, MILC ）為最有效降低複晶矽結晶化

溫度及減少結晶化所需時間的製程。MIC/MILC 的方法主要是非晶矽薄膜在退火之前先鍍覆一層金屬(Ni、Pd、Al、Co 等[3-6])；在退火時這一層金屬會與非晶矽薄膜產生反應進而降低結晶化溫度及減少結晶化所需時間。目前已有許多廠商(如 sharp 所提出的 CG silicon)及研究單位(如英國 Philip Research Lab 所提出的 MILC)已經成功的將 MIC/MILC 的方式用在低溫複晶矽薄膜電晶體的製作，在較低的退火溫度及退火時間所做出的薄膜電晶體其元件特性優良已能取代 SPC 所製作出之薄膜電晶體元件。[7-9]

而 MIC/MILC 有其缺點，針對此一缺點 2001 年 Murley [10]等人提出利用準分子雷射輔助金屬誘發非晶矽結晶化來提高複晶矽薄膜電性，之後也有許多研究團體投入同一製程研究並且發表文章。

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[7] S. W. Lee et al., IEEE Electron Device Letter, 17, p160 (1996)

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[9] S. Y. Yoon et al., J. Appl. Phys. 87, p609 (1994).

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[11]K. C. Park, J. H. Lee, I. H. Song, S. H. Jung, M. K. Han, J. of Non-Crystalline Solids, 299–302 1330–1334 (2002)

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[13]S. Y. Yoon, N. Young, P.J.vanderZaag, and D. McCulloch, IEEE TRANSACTIONS ON ELECTRON DEVICES, **24**, 22 (2003).

四 研究方法:

步驟一:以四吋 P 型(100)矽晶圓經過溼式氧化製程氧化形成 500nm 厚的氧化矽膜模擬玻離基板，利用低壓化學氣相蒸鍍(low pressure chemical vapor deposition, LPCVD) 鍍出約為 100nm 厚的非晶矽薄膜如圖一(a)。

步驟二:利用電漿輔助化學氣相沉積系統(Plasma Enhance Chemical Vapor Deposition System, PECVD)沉積出 5000A 的氧化矽之後，表面旋塗上光阻利用黃光微影定義出金屬與非晶矽接觸區域如圖一(b)。

步驟三:利用 BOE (buffer oxide etching solution)將未覆蓋光阻之區域的氧化矽薄膜除去如圖一(c)。

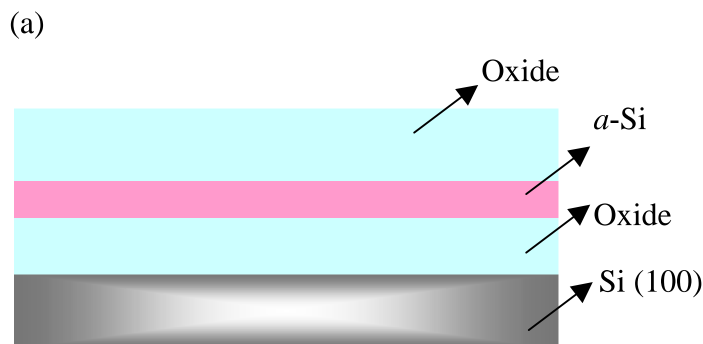
步驟四:利用物理氣相蒸鍍(physical vapor deposition, PVD) 蒸鍍出約 10nm 厚之鎳金屬如圖一(d)。

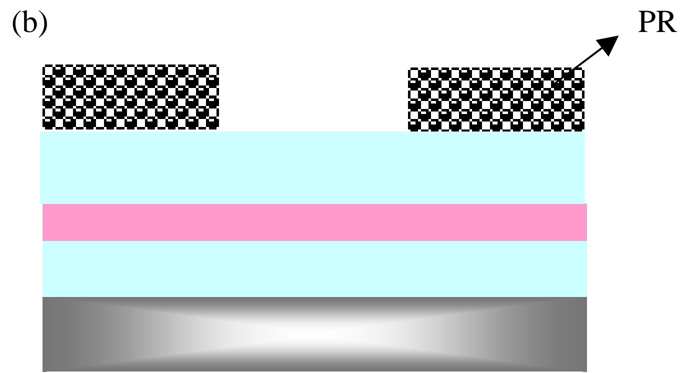
步驟五:將矽晶圓浸入丙酮內將光阻除去如圖一(e)。

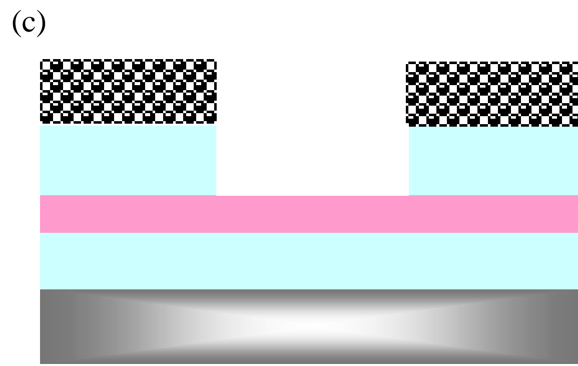
步驟六:將矽晶圓經過 550°C48h 之熱處理後得到適合長度(註一)之 MILC 複晶矽薄膜之後。在室溫下，經過不同能量之雷射退火(註二)後得到 MILC-ELA 複晶矽薄膜如圖一(f)。

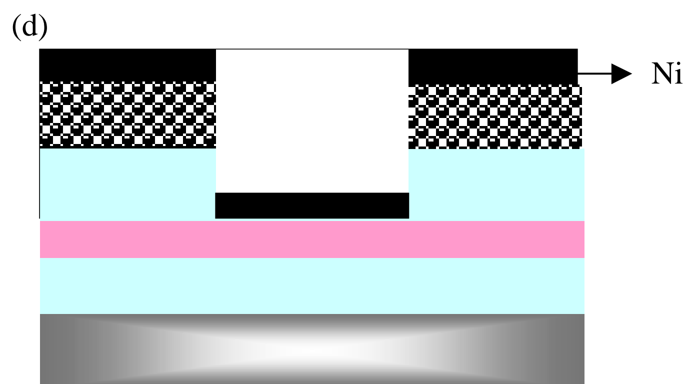
利用掃描式電子顯微鏡 穿透式電子顯微鏡及拉曼光譜儀分析 MILC-ELA 複晶矽薄膜之結晶性及晶粒形態，另外利用原子力薄膜顯微鏡分析 MILC-ELA 複晶矽薄膜表面之型態。

(a)

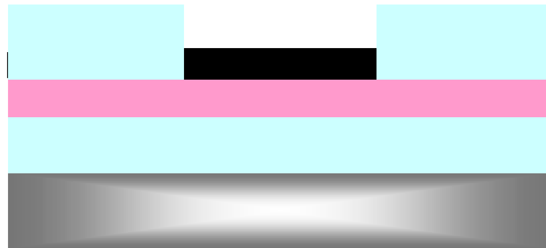



(b)
PR

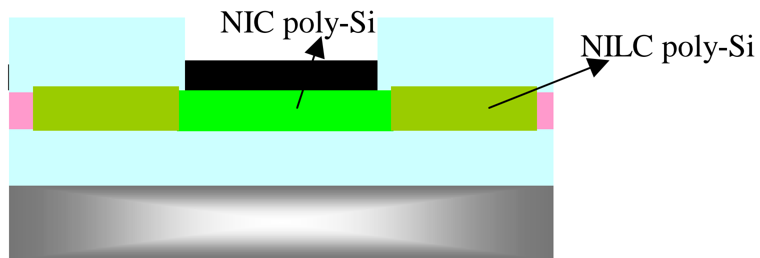

(c)


(d)
Ni

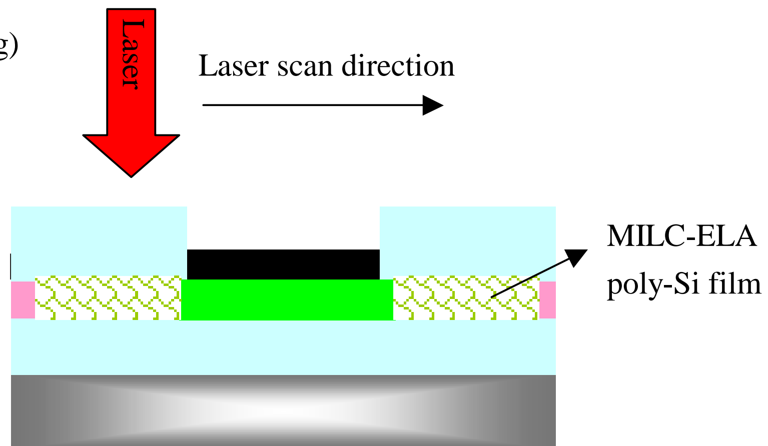
(e)



(f)



(g)



圖一 ELC 複晶矽薄膜製作流程

薄膜電晶體製作流程如下:

步驟一: 將鎳薄膜及氧化矽薄膜除去後如圖二(a)所示複晶薄膜經過第一道黃光製程及乾式蝕刻後定義出薄膜電晶體主動層利用電漿輔助化學氣相沉積系統(Plasma Enhance Chemical Vapor Deposition System, PECVD)沉積出 1000A 的氧化矽當作薄膜電晶體的閘極氧化層,再利用 LPCVD 沉積出 2000A 的非晶矽薄膜來當作薄膜電晶體的閘極圖二(b)所示。

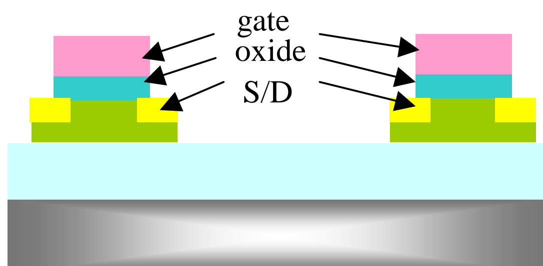
步驟二: 經第二道黃光製程以及乾式蝕刻後除去多餘的氧化矽及非晶矽定義出薄膜電晶體的閘極氧化層(Gate Oxide)及閘極(Gate) 之後利用自動對準(self-align)的方式將磷植入源極及汲極之位置如圖二(c)。

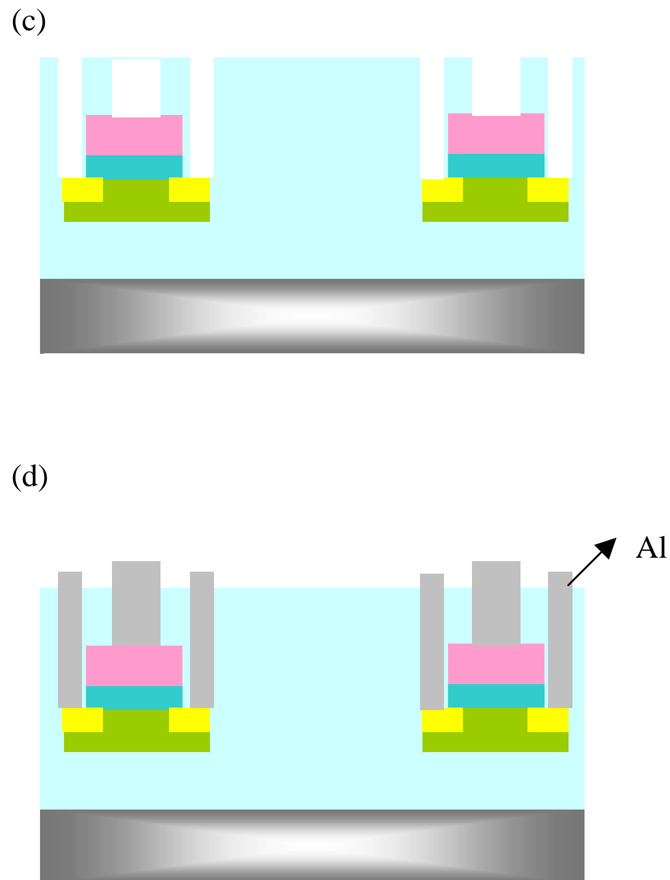
步驟三:利用 PECVD 沉積出 4000 A 的氧化矽薄膜再經第三道黃光製程及乾式蝕刻定義出接觸窗(contact hole)如圖二(d)所示。

步驟四:最後利用熱蒸鍍(thermal coater)上鋁導線經第四到黃光製程以及鋁蝕刻定義出鋁墊如圖二(e)所示製程,至此已完成元件製作,量其薄膜電晶體電性

(a)

(b)





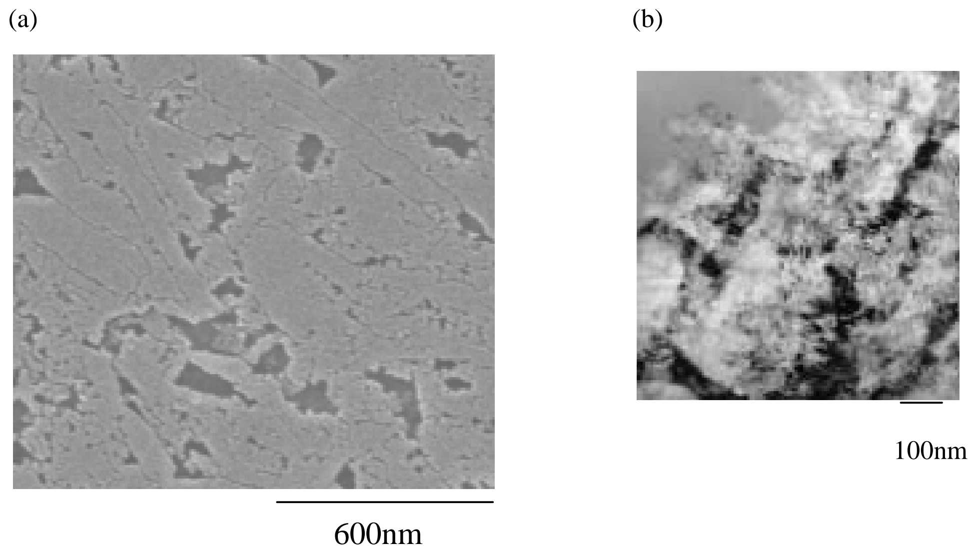
圖二 ELC 複晶矽薄膜電晶體製作流程

註一:適當之 MILC 長度需要視金屬與薄膜電晶體主動層位置而定義，在本計劃中所使用之光罩所需要之 MILC 長度必須為 90μm

註二:所使用之雷射機台為半導體中心提供之 KrF excimer laser (Lambda Physik LPX-210i, λ~248 nm)

五結果與討論:

圖三(a)為 MILC 複晶矽薄膜經過 secco 蝕刻液處理過後之 SEM 圖圖三(b)為 MILC 複晶矽薄膜之 TEM 圖。可以看出 MILC 複晶矽薄膜主要是由針狀的複晶矽晶粒所組成。其針狀複晶矽晶粒的寬度為約 50nm 長度為約 700nm。而在晶粒之間有被蝕刻出之凹洞代表 MILC 複晶矽薄膜內有缺陷或者是未結晶化之區域。



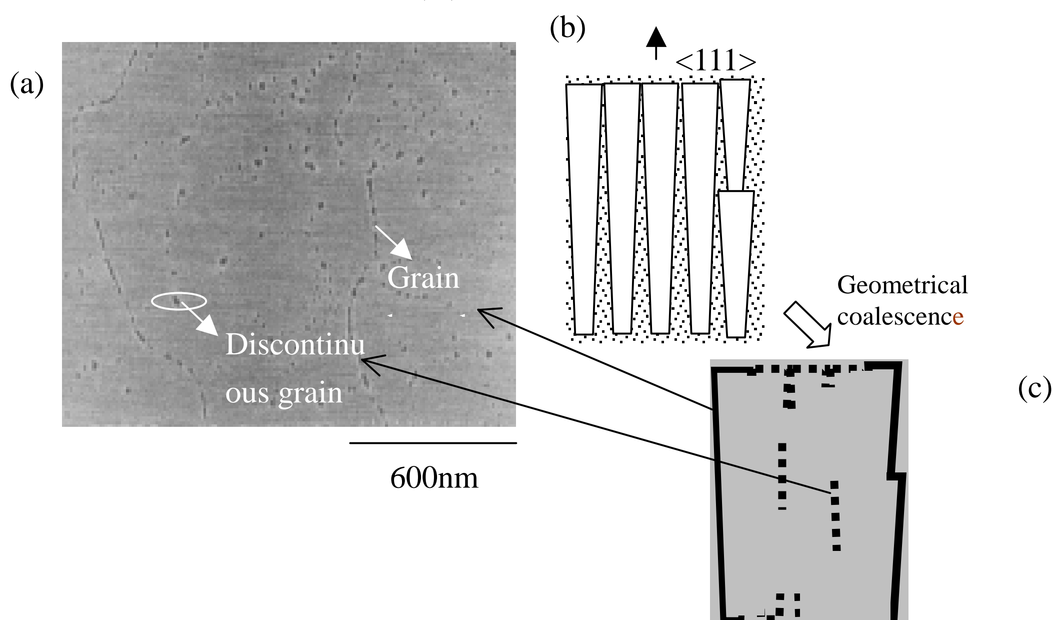
圖三(a)為 MILC 複晶矽薄膜經過 secco 蝕刻液處理過後之 SEM 圖
(b) 為 MILC 複晶矽薄膜之 TEM 圖

圖四及圖五為 MILC 複晶矽薄膜經過不同能量密度之雷射退火之 SEM 圖, 由這些圖可以發現 MILC 複晶矽薄膜經過不同能量密度之雷射退火主要有三種結晶化階段，這三階段分別為(1)非晶矽熔解階段(2)接近完全熔解階段(3) 完全熔解階段。當雷射能量密度低於 230mJ/cm^2 時，MILC-ELA 複晶矽薄膜為非晶矽熔解階段，因為在此一階段之 MILC-ELA 複晶矽薄膜之晶粒型態仍然為針狀複晶矽晶粒近似於未經過雷射退火之 MILC 複晶矽薄膜之晶粒型態，所以表示經過此一能量密度以下之雷射照射時, 只有晶粒間非晶之區域(包含缺陷)開始熔解而且隨著能量密度越接近 230mJ/cm^2 晶粒間非晶之區域熔解面積越大，直至能量密度到達 230mJ/cm^2 所有晶粒間非晶之區域完全熔化。當雷射能量密度繼續增加至 265mJ/cm^2，MILC-ELA 複晶矽薄膜為接近完全熔解階段，在此一階段中複晶矽之晶粒寬度由原本的50nm劇烈成長至600nm而且還發現非連續晶界存在如圖四(a)所示。當雷射能亮密度持續增加至 295mJ/cm^{2}時晶粒形狀由單軸長之針狀晶粒變

成等軸晶而且晶粒尺寸也跟著縮小，代表著經經過此一能量密度以下之雷射照射時，MILC-ELA 複晶矽薄膜為完全熔解階段。

同樣的融解階段與雷射能量變化之情況由 Chen 等人提出[1]他們研究中是針對直接沉積複晶矽(as-deposited poly-Si)對不同能量密度雷射退火之情形，他們發現在複晶矽晶粒間之非晶矽區域會比複晶矽晶粒在較低能量密度之雷射退火下熔化，因為非晶矽本身的熔點低於複晶矽本身的熔點。同理在本研究中因為針狀複晶矽晶粒本身的熔點高於複晶矽晶粒間之非晶矽區域的熔點，所以當能量漸漸增加非晶矽區域熔化區域會漸漸增加。

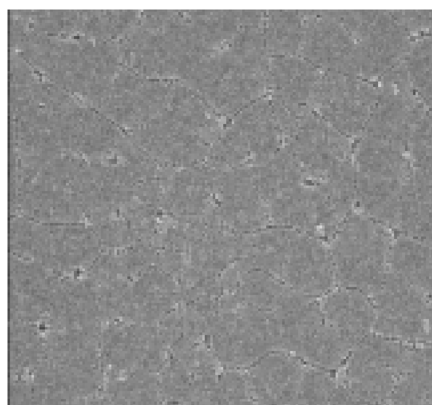
當雷射能量密度繼續增加至接近完全熔解階段，大部份的複晶矽晶粒間之非晶矽區域及複晶矽晶粒皆熔化但一些尺寸較大之複晶矽晶粒並沒有完全熔化。當開始固化時這些未熔化之晶粒則當作固化的核去成長新的晶粒如圖四(a)所示，這些複晶矽晶粒寬度由原本的 50nm 劇烈成長至 600nm 是因為幾何聚集效應(geometrical coalescence)所導致的。幾何聚集效應簡單的描述就是兩個晶粒方向接近之晶粒在晶粒成長的時候，晶界會消失使得晶粒成長。[2] 幾何聚集效應要發生之必要條件為必須兩個相鄰之晶粒有相似之方向。而在本研究中的 MILC 複晶矽晶粒即具備此一條件。由之前的文獻[3]證明 MILC 複晶矽晶粒擁有從優方向<111>之特性如圖四(b)所示，所以 MILC 複晶矽薄膜經適當能量之雷射退火後擁有幾何聚集效應快速晶粒成長的現象發生，但由於雷射退火的固化速率很快由 1200°C降至室溫只有 90nsec 的時間[4]使得幾何聚集效應無法達到平衡所以會有非連續晶界產生如圖四(c)所示。



圖四在接近完全熔解階段下形成之 MILC-ELA 複晶矽薄膜(雷射能量密度在 265 mJ/cm²) (a) MILC-ELA 複晶矽薄的 SEM 圖其雷射退火前後的示意圖分別以 (b) 及 (c)表示

當雷射能量密度超過完全熔解階段，MILC 複晶矽薄膜完全熔解，所以固化出之矽晶粒為均勻成核之細小晶粒如圖五所示。

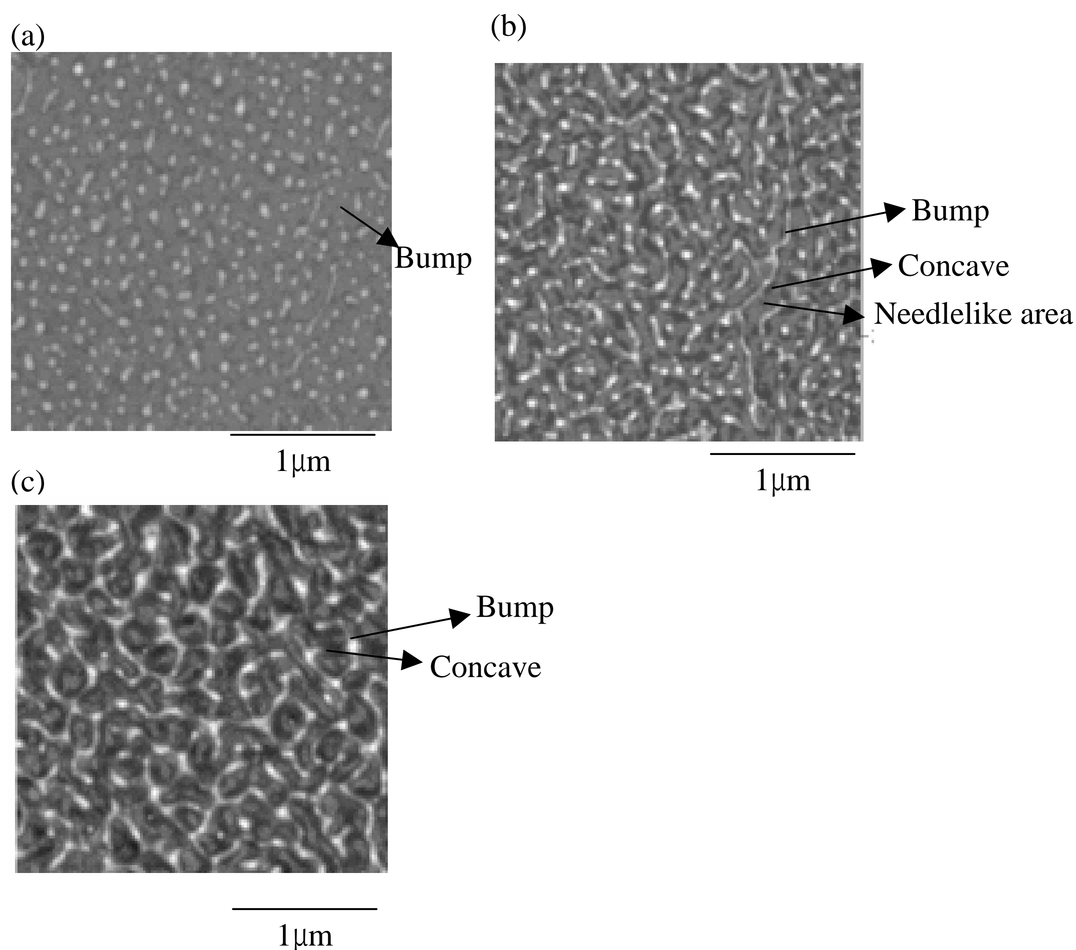
除了 SEM 之外 AFM 也用來研究雷射能量密度對結晶化機制的影響。在雷射退火之前，MILC 複晶矽薄膜表面是非常平坦。在雷射退火之後，複晶矽薄膜表面開始發現突起(明亮處)及凹下(黑暗處)的區域。當雷射能量是處在非晶矽熔解階段，可以發現突起與凹下處圍繞出針狀區域如圖六所示。 而且發現突起及凹下的區域會隨著雷射能量增加而增加，直到能量達到接近完全熔解階段， 針 狀晶粒之寬度變大如圖六所示。當能量增加超過完全熔解階段，針狀區域消失突起與凹下圍繞出的形狀變成等軸且較小的晶粒。



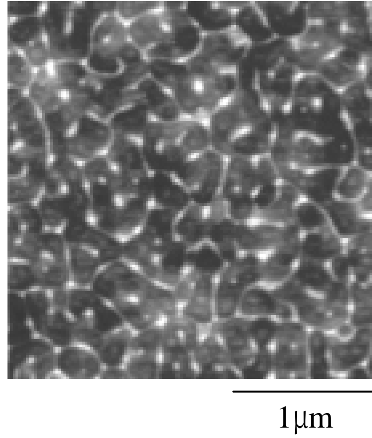
圖五在完全熔解階段下形成之 MILC-ELA 複晶矽薄膜之 SEM 圖(雷射能量密度在 295 mJ/cm²)

由 AFM 量測結果與圖二 SEM 觀察結果比較。在經過雷射退火之前，MILC 複晶矽薄膜表面是平坦。在雷射退火之後，複晶矽薄膜表面開始發現突起(明亮處)及凹下(黑暗處)的區域。導因於液態矽本身密度約為 2.53 g/cm³ 大於 2.30 g/cm³ 的固態矽密度造成結晶化時期先固化之區域形成凹洞的區域最後會形成突起的

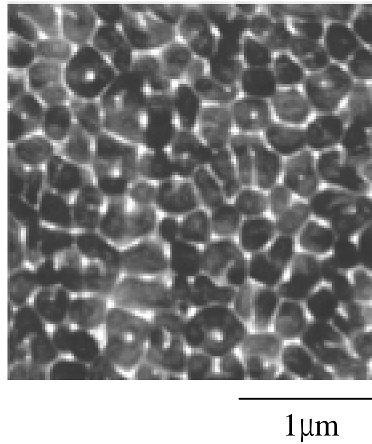
區域。[1][4] 在非晶矽熔解階段，MILC 複晶矽薄膜表面經過(125,165 及 200 mJ/cm²)雷射退火照射過後如圖五所示，會隨著雷射能量增加而使得突起及凹下的區域增加。這個改變趨勢並不會超出我們的預期因為非晶矽熔解區域面積會隨著雷射能量增加而增加，所以依照此一假設則可以得知突起及凹下的區域會隨著雷射能量增加如圖四所示。當能量增加至接近完全熔解階段，複晶矽晶粒間之非晶矽區域及複晶矽晶粒皆開始熔化但一些尺寸較大之複晶矽晶粒並沒有完全熔化。這些沒溶化之晶粒可以當作固化之結晶合所以矽晶粒尺寸開始劇烈成長如圖七。最後當能量增加超過 295mJ/cm²，MILC 複晶矽薄膜完全熔解所以當完全溶解時固化時為均質成核所以晶粒尺寸變小如圖八。



圖六 MILC-ELA 複晶矽薄膜 在非晶矽熔解階段的 AFM 圖(a) 125mJ/cm² (b) 165 mJ/cm²(C)200 mJ/cm².

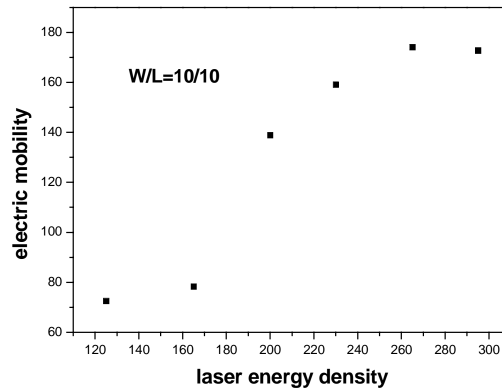


圖七 MILC-ELA 複晶矽薄膜在接近完全熔解階段的 AFM 圖



圖八 MILC-ELA 複晶矽薄膜在完全熔解階段的 AFM 圖

圖九為 MILC-ELA 複晶矽薄膜電晶體(通道尺寸為 10/10μｍ)其電子遷移率與雷射能量之關係圖，可以看出矽晶粒尺寸最大之接近完全熔解階段的雷射能量擁有最佳電性表現，之後根據材料分析結果得知在接近完全熔解階段其 MILC-ELA 複晶矽薄膜的晶粒尺寸約為 2~3μｍ所以我們將複晶矽薄膜電晶體尺寸縮小至 2/2μｍ所得電性獲得很大提升如表一所示。



圖九為 MILC-ELA 複晶矽薄膜電晶體其電子遷移率與雷射能量之關係圖

表一不同尺寸之複晶矽薄膜電晶體電性比較

W/L	S	μ	Vth	Leakage current	On/Off
10/10	0.806	180	0.43	1.02E-9A	3.63E5
3/3	0.397	286.1	-2.0	2.4E-9 A	1.83E5

六 結論與建議

本研究計劃已經成功執行製作出高品質之 MILC-ELA 複晶矽薄膜並且建立起 MILC-ELA 複晶矽薄膜結晶化成長機制。而且根據結晶化成長機制成功製作出高效能之薄膜電晶體及其製程參數。

七 計畫成果自評:

本計畫已經符合當初預期的目標建立起 MILC-ELA 複晶矽薄膜結晶化成長機制並且根據結晶化成長機制成功製作出高效能之薄膜電晶體及其製程參數。已經能夠完成第一年計畫之目標。