行政院國家科學委員會專題研究計畫　成果報告

一種新式氮化矽快閃式記憶元件研究(2/2)

計畫類別：個別型計畫
計畫編號：NSC91-2215-E-009-019-
執行期間：91 年 08 月 01 日至 92 年 07 月 31 日
執行單位：國立交通大學電子工程學系

計畫主持人：汪大暉

報告類型：完整報告
報告附件：出席國際會議研究心得報告及發表論文
處理方式：本計畫可公開查詢

中　華　民　國 92 年 10 月 30 日

一種新式氮化矽快閃式記憶元件研究

摘要

本計畫著重於新式氮化矽快閃式記憶元件所發生的可靠性問題。其中包括重複寫入/抹除之耐久性、抹除狀態之臨界電壓漂移、寫入狀態之資料保存、讀取時擾動與儲存時間加速測試方法。而在此研究中，氮化矽快閃式記憶元件為一 n 型通道 MOSFET 加上 ONO 閘極結構而構成。不像傳統之 SONOS，此特殊元件有較厚之底部氧化層，可避免電荷直接穿隧且操作方式分別藉由熱電子寫入（hot electron program）與熱電洞抹除（BTBT hot hole erase)。由於這種絕佳的操作模式，使得每個電晶體可以儲存兩個位元。

關於可靠性議題方面，臨界電壓準位皆隨著寫入/抹除次數的增加而向上揚升。此重複寫入抹除之耐久性機制，將在此被探討。此外，抹除狀態資料遺失也被發現。首先，在一經過 P/E 加壓後之元件，抹除狀態之臨界電壓會隨著儲存時間而漂移。此現象與溫度有著微弱的關係並且在大約 1k 次左右的寫入抹除下，有最大值。此特殊之次數關係，與底部氧化層中帶正電性陷住電荷的生成有密切關係。其時間與臨界電壓漂移的關係，可用穿隧波前模型來完整的描述。此外，在兩位元操作，有著明顯的讀取擾動效應。臨界電壓漂移，分別顯示了 t^n 或是 log(t)的關係，取決於讀取位元偏壓大小。因此，在使用汲極擾動加速測試生命期方法，必須非常注意。而一正電性氧化層電荷幫助通道電子注入之解析模型，被用來解釋此讀取擾動特性。

氮化矽層電荷透過氧化層缺陷幫助穿隧而造成之資料遺失，在此也被描述。Frenkel-Poole 散失為此最主要的機制。而資料流失與氮化矽層之電場呈現平方根之關係也被觀察到。我們發現此與浮動閘極快閃元件與傳統 SONOS 元件有著迥異之電荷流失機制。例如在浮動閘極快閃元件為缺陷協助穿隧而 SONOS 元件為電荷直接穿隧。最後，對於元件資料保存時間之測試，提出一閘極偏壓加速方法。

關鍵詞：氮化矽快閃式記憶元件，重複寫入/抹除之耐久性，抹除狀態之臨界電壓漂移，寫入狀態之資料保存，讀取時擾動，儲存時間加速測試方法，正電性陷住電荷，穿隧波前模型，正電性氧化層電荷幫助通道電子注入，氧化層缺陷幫助穿隧，Frenkel-Poole 散失，閘極偏壓加速

Physics, Characterization and Design of Oxide-Nitride-Oxide Flash EEPROM Devices

Abstract

This project addresses the reliability issues of new SONOS Flash EEPROM cells, which include program/erase cycling endurance, erase state threshold voltage drift, program state charge retention loss, read-disturb and accelerating lifetime measurement methods. In this study, the new type SONOS cell is made of a n-channel MOSFET with an oxide-nitride-oxide gate structure. Unlike conventional SONOS cells, this cell has a relatively thick bottom oxide to avoid charge direct tunneling and is operated by means of channel hot electron program and band-to-band hot hole erase, respectively. Due to this operation mode, two bits per cell will be realized.

With respect to the cell reliability, the threshold voltage window may shift upward as P/E cycle number increases. The mechanism for this cycling endurance issue will be investigated. In addition, erase-state data loss is explored. First, an erase-state threshold drift with storage time is observed in a P/E cycled cell. This drift has insignificant temperature dependence and has a peak around 1k P/E cycles. This peculiar cycle number dependence is strongly related to creation of positive trapped charge in the bottom oxide. The temporal evolution of the threshold voltage drift can be well described by the tunneling front model. Furthermore,

significant read-disturb effect is noticed in two-bit operation. The threshold voltage shift exhibits either t^n or log(t) behavior, depending on read bitline voltage. Therefore, one must be very cautious to use the V_d acceleration in read-disturb lifetime measurement. An analytical model based on positive oxide charge assisted channel hot electron injection has been developed to explain the read-disturb behavior.

Program-state retention loss due to nitride charge escape via oxide trap assisted tunneling is also characterized. Frenkel-Poole emission is found to be the dominant mechanism. A square root dependence of charge loss on nitride electric field is observed. We find that this feature is unique in this cell since floating gate flash cells and conventional SONOS cells have different charge loss mechanisms, i.e. trap-assisted tunneling (SILC) in floating gate flash cells and charge direct tunneling in SONOS cells. Finally, a V_g acceleration method for retention lifetime measurement is proposed.

Keywords: SONOS Flash EEPROM, program/erase cycling endurance, erase state threshold voltage drift, program state charge retention loss, read-disturb, accelerating lifetime measurement methods, positive trapped charge, tunneling front model, positive oxide charge assisted channel hot electron injection, oxide trap assisted tunneling, Frenkel-Poole emission, V_g acceleration method.

Contents

Chapter 1
Introduction

The nonvolatility of semiconductor memory devices is usually achieved by charge storage in the multilayer gate structure of a field effect transistor or by polarizing the ferroelectric material in a ferroelectric capacitor/transistor. With respect to charge storage devices, there are two kinds of them. (a) Charge Trapping Devices: Charge is stored in the traps at the interfaces of a multilayer gate structure and/or in the insulator bulk, such as the metal nitride oxide silicon (MNOS) structure, proposed first in [1], [2]. (b) Floating Gate Devices: Charge is stored in a thin conducting or semiconductor layer or conducting particles sandwiched between insulators [3], [4]. Since its invention in 1967, nitride-based nonvolatile memory structures, both MNOS and polysilicon blocking oxide-nitride-oxide silicon (SONOS) [5]-[9], have received limited commercial acceptance due to their employment of ultra-thin dielectric (~20A) and their non-ideal charge retention characteristics.

In conventional SONOS cells, charges are stored uniformly in the nitride layer. This SONOS concept has recently evolved into a two-bit storage cell (NROM) [10]. The NROM flash EEPROM cells have soon received much interest for their small size per bit [10], [11] less fabrication complexity [12], no drain turn-on and better charge retentivity [13]. The NROM cell is made of a n-channel MOSFET with an oxide-nitride-oxide gate dielectric structure, as depicted in Fig.1.1. The charge is stored *locally* in the nitride layer above the n^+ source and drain junctions. Unlike the SONOS cell, the bottom oxide in the NROM cell is normally thicker than 40Å [11] to avoid charge direct tunneling and to improve retention

characteristics. Channel hot electron injection and band-to-band hot hole injection are utilized for programming and erasing, respectively. The I_d-V_{gs} of program state and erase state are depicted in Fig.1.2. by using a reverse read scheme. The subthreshold swing deterioration in program state is due to a narrow charge trapping region, typically tens of nano-meter. To allow for two-bit operation, the applied bitline voltage in reverse-read must be sufficiently large (>1.5V) to be able to "read-through" the trapped charge in the neighboring bit. Because of a thicker bottom oxide and higher read bitline voltage, the reliability issues in a NROM cell are quite different from the conventional SONOS cells. Thus, some new reliability concerns arise in the NROM cells. In this thesis we will investigate program/erase cycling endurance, erase-state threshold voltage drift, read-disturb, program-state charge retention loss, and accelerating lifetime measurement methods.

There are four chapters in this report. Chapter 1 is Introduction and we will introduce the evolution of the nitride based nonvolatile cells. In Chapter 2, the endurance failure of the NROM cell is discussed and recommendations for improvement of endurance will be made. In Chapter 3, data retention loss in erase-state is discussed. Room temperature threshold voltage drift and read-disturb effects are studied. In Chapter 4, we will investigate the charge loss mechanisms and characteristics in program state. A square-root electric field dependence of charge loss is observed. The corresponding mechanism is explored. Finally, we will propose an Vg-accelerated method to measure retention lifetime.

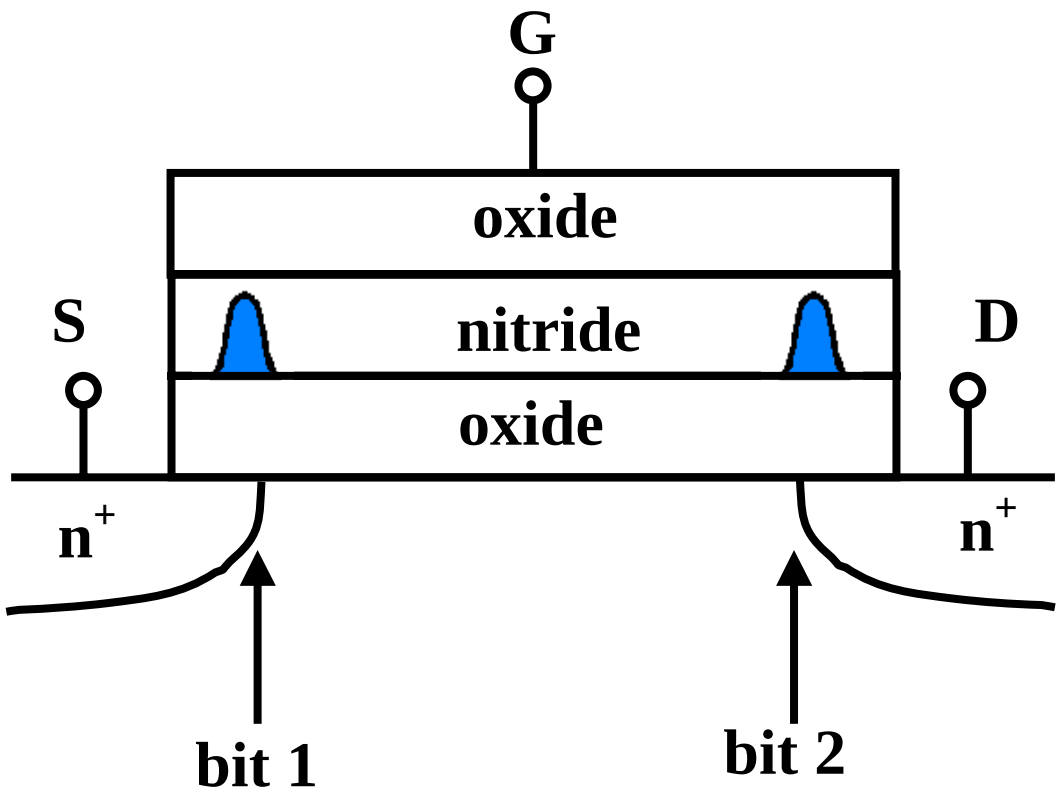


Fig. 1.1 Schematic representation of a NROM cell and two-bit storage. The shaded area in the nitride layer represents stored charges.

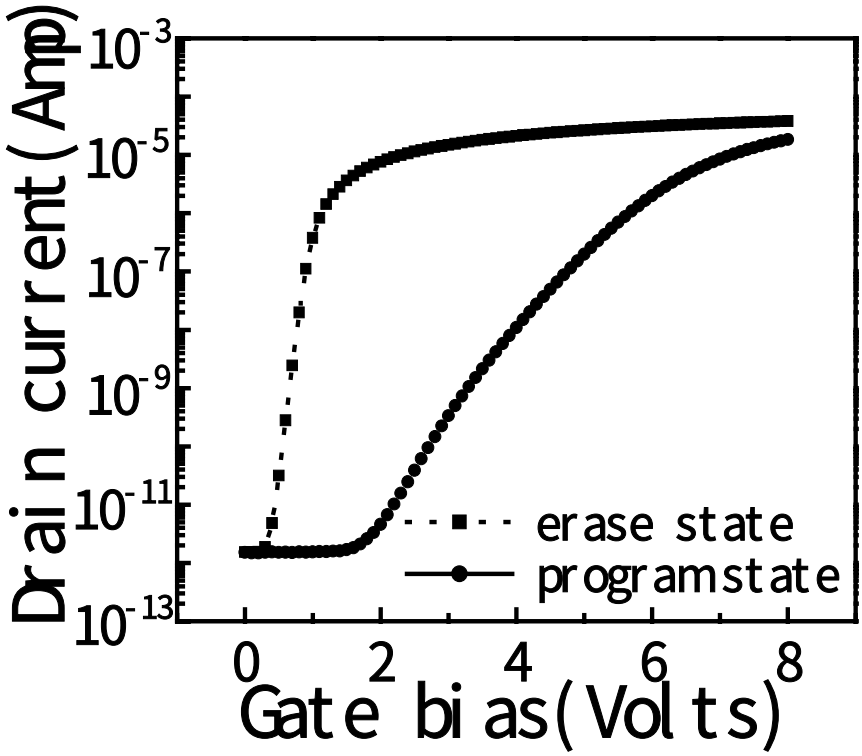


Fig. 1.2 Drain current versus gate bias in erase state and in program state.

Chapter 2
Cycling Endurance of NROM Cells

2.1 Introduction

Endurance is an important issue in nonvolatile memory. It's defined by the number of data changes that can be performed in every cell of a given memory chip before one of the cells fails to meet the data sheet specifications. It describes the reliability of a device in terms of the number of program/erase (P/E) operations that can be performed on it without failure. Today, most commercially available nonvolatile memory products are guaranteed to withstand, at least 10,000 P/E cycles [14]. In a floating gate memory, electron trapping after numerous P/E cycles in tunnel oxide builds up a permanent negative charge, thereby reducing the electric field and injected tunneling current for the same applied terminal voltage. For a constant program voltage and program time, this reduces the program-state threshold voltage whereas increases the erase-state threshold voltage, resulting in a threshold voltage window closure problem [15]. In NROM devices, the window closure is not observed (Fig. 2.1). Instead, there appears an upward shift of both program-state and erase-state threshold voltages after P/E stress. We will discuss the cause for this endurance degradation in NROM cells.

2.2 Endurance Failure in NROM Cells

In conventional EEPROM memories, the degradation of the threshold voltage window

with P/E cycles is due to trap generation in the tunnel oxide. Threshold voltage window opening in the initial tens of cycles is caused by positive charge trapping, whereas window closing after 10^4-10^5 cycles is caused by electron trapping in the oxide (Fig. 2.2)[16]. The NROM cells apparently exhibit a different feature. Both program-state and erase-state threshold voltages move upward in parallel (Fig. 2.1). This characteristic reveals that programming and erasing speeds are not degraded after cycling stress and implies that the failure of endurance may result from the aging of the tunnel oxide, including interface state creation or oxide charge accumulation caused by cycling stress. Interface state creation can be easily excluded since the subthreshold swing in a 100k-P/E-cycled device is similar to that of the fresh one, no matter in program state or in erase state, as shown in Fig. 2.3. Based on the above observation, it seems that oxide trap/oxide charge creation should be responsible for the endurance failure.

2.3 Evidence of Negative Charge Creation

The subthreshold characteristics at program state and erase state in a fresh device and in a cycled device are compared in Fig. 2.3. Although no significant swing degradation is observed, we do observe a parallel shift of the I-V curve before and after P/E stress. The parallel shift in Fig. 2.3 is usually attributed to negative trapped charge creation in the bottom oxide. Thus, the ONO dielectric layers actually consist of two kinds of charge in program state; negative trapped charge in the bottom oxide (Q_R) and negative charge in the nitride (Q_{pm}), as illustrated in Fig. 2.4. In erase state, the nitride charge (Q_{pm}) can be neutralized by

band-to-band hot hole injection through either electron-hole recombination or compensation while Q_R is still present in the bottom oxide. Fig. 2.4 is a diagram illustrating the charge distribution in the ONO in program state (Fig. 2.4(b)) and in erase state (Fig. 2.4(c)). Q_R is negligible in a fresh device and increases with P/E stress. The build-up of the bottom oxide charge Q_R, which cannot be removed by erase, explains the upward shift of the threshold window with P/E cycles. The relative positions of Q_R and Q_{pm} depicted in Fig. 2.4 are constructed by the following measurements. A fresh device and a 100k cycling stressed device are used for this study. GIDL current and threshold voltage are measured. GIDL current is used as a monitor for the charge in the ONO layers above the n+ drain region while threshold voltage can be used to measure the ONO charge in the channel region (please refer to Fig. 2.5). First, we adjust the programming bias condition for each device to make sure that program-state GIDL current is the same in each device. The measured program-state threshold voltage is 3.75V in the fresh device and 4.27V in the 100k device. The same GIDL current means the two devices have the same amount of charge above the n+ drain. The higher threshold in the 100k cell is believed due to the additional stress created oxide charge $Q_{R.}$. Then, the erase characteristics of the two devices are measured. Fig. 2.6 shows the threshold voltage shift with erase time in the two devices. It is interesting to note that the two curves in Fig. 2.6 are almost identical. Two questions are brought about. First, why the two devices have the same erasing speed? This can be understood because the two devices have the same GIDL current. The readers should be reminded that GIDL reflects the strength of hot hole erasing. Second, why the erasing in the 100k cell stops around 1millisecond and the threshold

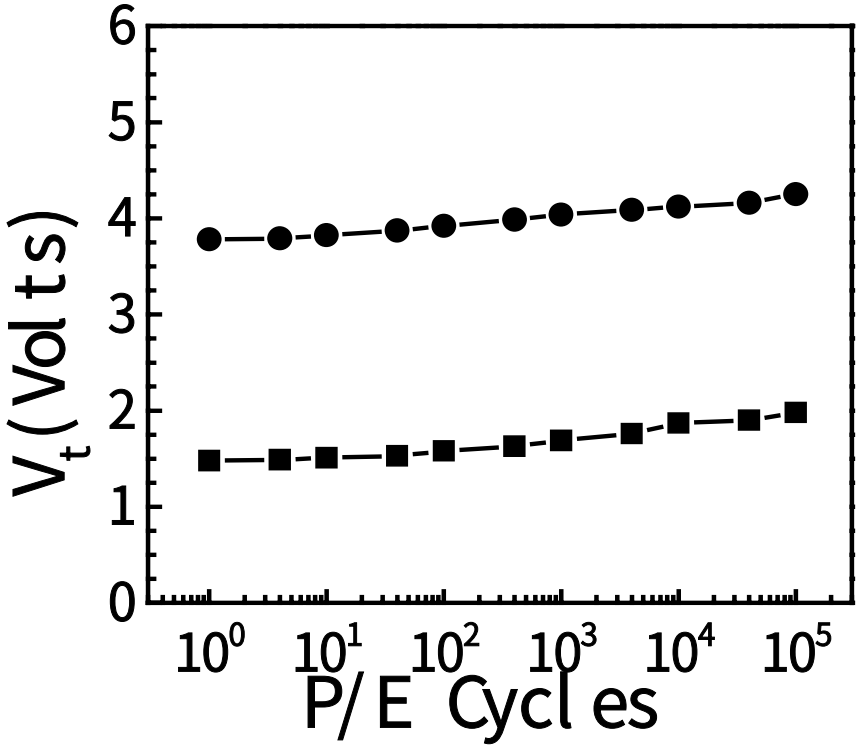


Fig. 2.1 Endurance characteristics of a NROM cell operation window. Program @V_{ds}=4.7V, V_{gs}=11V, 10ms and erase @ V_{ds}=7.0V, V_{gs}=-3V, 3ms. The thickness of each ONO layer is 70Å, 60 Å and 70 Å.

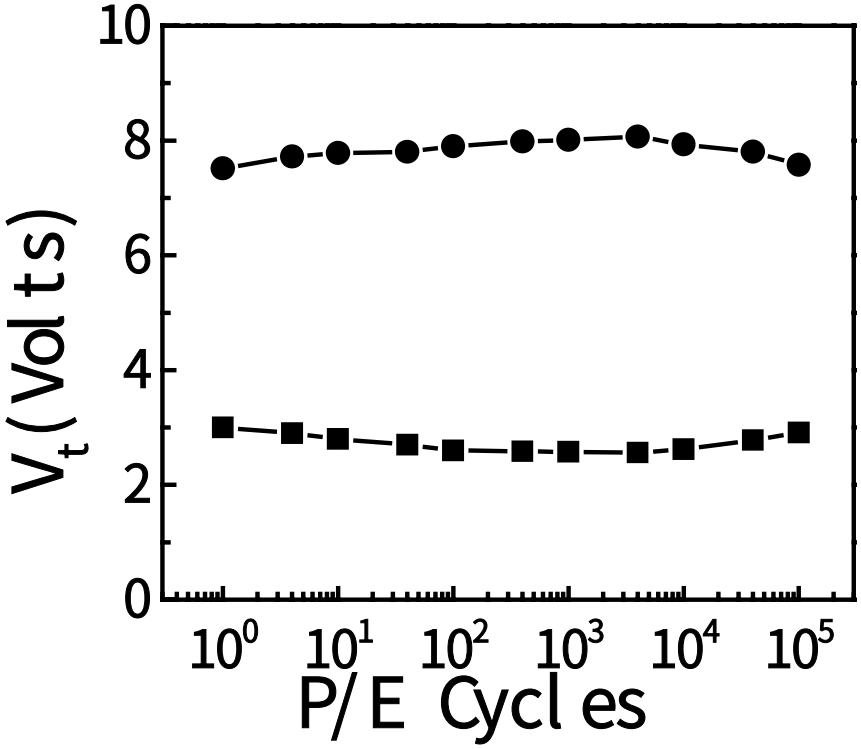


Fig. 2.2 Endurance characteristics of a floating-gate flash cell showing the window opening and closing.

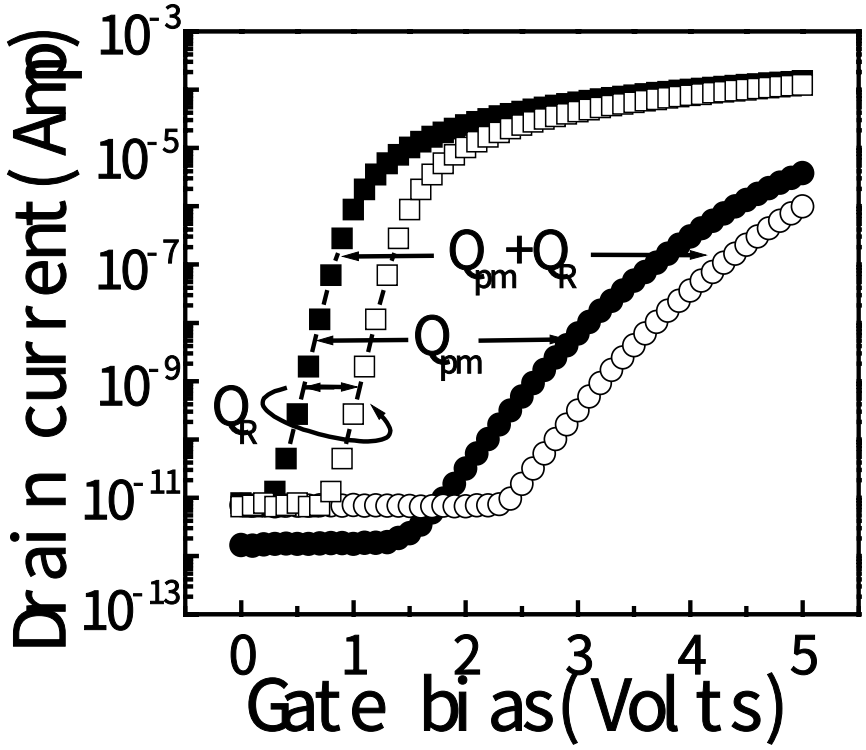


Fig. 2.3 NROM cell subthreshold characteristics in erase state and in program state before stress and after 100k cycling stress. Q_{pm} and Q_R represent the charge created by P/E stress and the injected charge by programming, respectively.

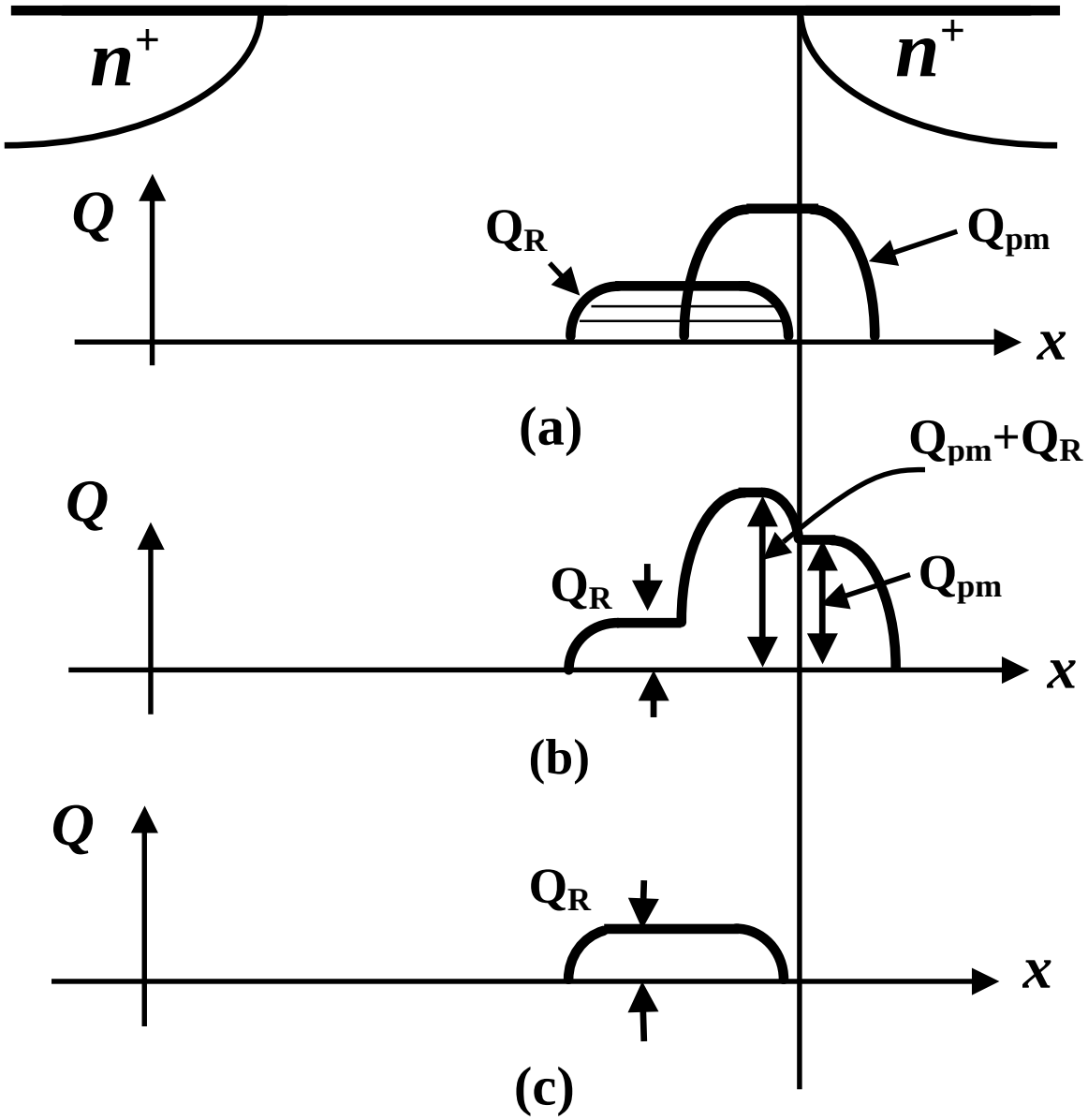


Fig. 2.4(a) The relative position of Q_R and Q_{pm} in a cycled cell. The x-axis is the channel direction. There is an overlap between Q_R and Q_{pm}.

Fig 2.4(b) The charge distribution of Q_R and Q_{pm} in program state after cycling stress.

Fig 2.4(c) Q_R in erase state in a stressed cell.

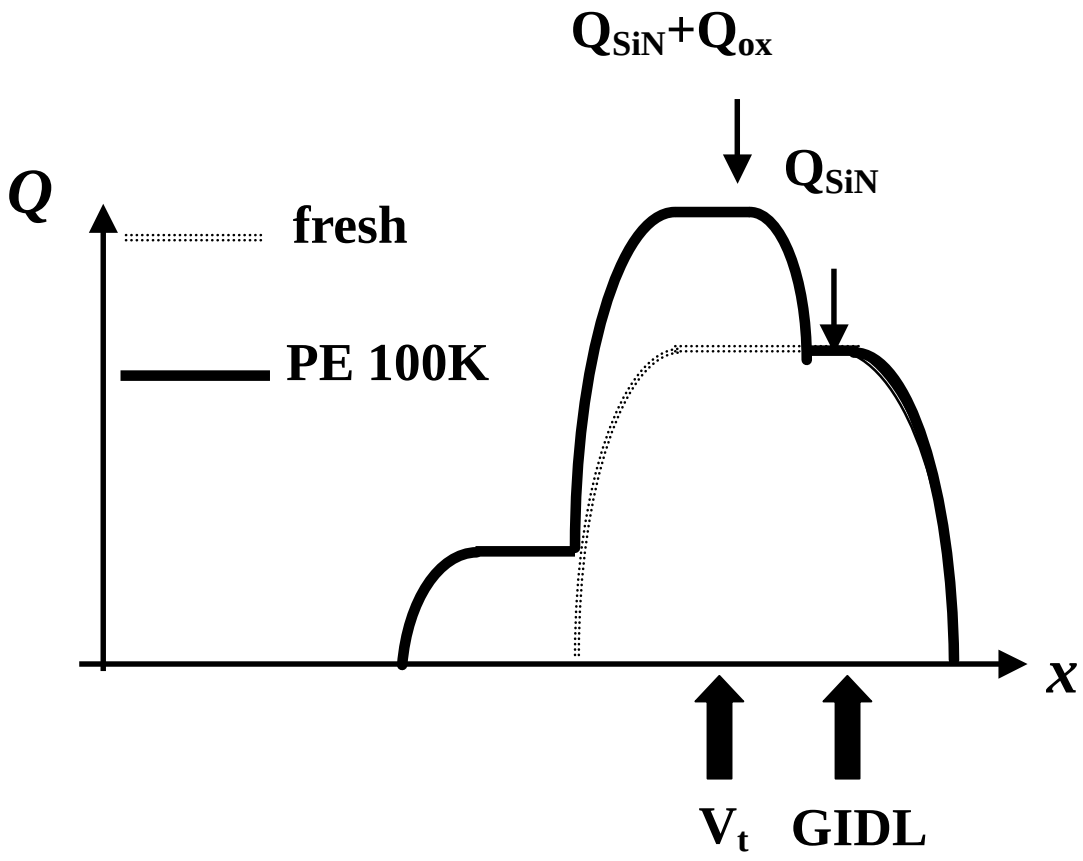


Fig. 2.5 Illustration of the charge distribution in the fresh and the 100k P/E devices. The two devices are

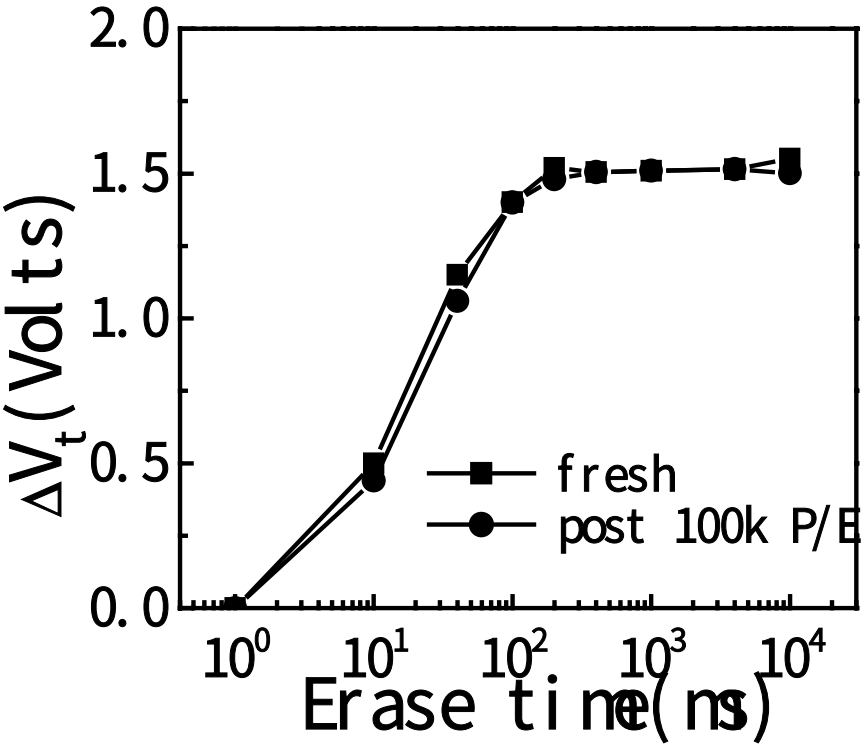


Fig. 2.6 Threshold voltage shift with erase time in a fresh cell and in a 100k cycled cell

shift is the same as in the fresh cell although the program-state threshold in the 100k device is about 0.5V higher ? This implies that part of the ONO charge in the 100k device, amounting to 0.5V threshold voltage shift, cannot be erased. Why this charge cannot be erased ? What kind of charge is it ? We believe the answer is oxide trapped charge Q_R. From the above arguments, the picture of the oxide charge and the nitride charge distributions in the 100k device is constructed as in Fig. 2.6.

In the second experiment, both the devices are programmed to have the same threshold voltage. The measured GIDL current in the 100k device is found to be smaller than that in the fresh device. Fig. 2.7 shows the measured result and the corresponding charge distributions. Again, the threshold voltage shift versus erase time in the devices are measured (Fig. 2.8). Now, the fresh device has a larger threshold shift. Our explanation is as follows. Although the total ONO charge in the channel region in the two devices are equal (i.e. the same program-state threshold), the ONO charge in the fresh cell is completely the erasable nitride charge and thus the threshold voltage shift in the fresh device during erase is larger.

Finally, we would like to compare the P/E stress effects in the conventional gate MOSFET and in the NROM cell. Fig. 2.9 shows the threshold voltage shift in the MOSFET and in the NROM cell. Since oxide charge creation is the only cause for the shift in the NMOSFET, the similarity between the NMOSFET and the NROM in Fig. 2.9 indicates that solely oxide charge creation can explain the observed endurance degradation in the NROM cell.

2.4 Improvement of Cycling Endurance

From the above study, we conclude that the shift of the threshold voltage window in the NROM cell is attributed to bottom oxide charge creation. The endurance of the operation window can be improved by increasing bottom oxide robustness. It has been well reported in literature that thinner oxide has less charge creation [17]. The reduction of bottom oxide thickness should be an effective approach to improving the endurance. Another approach is to strengthen the erase bias condition. A stronger erase will result in accumulation of excess holes in the nitride to compensate for the negative oxide charge or even increases the possibility of recombination of injected hot holes and oxide trapped electrons.

Fig. 2.10 shows the threshold voltage window by using a stronger erase bias. Endurance up to 10^6 cycles can be achieved.

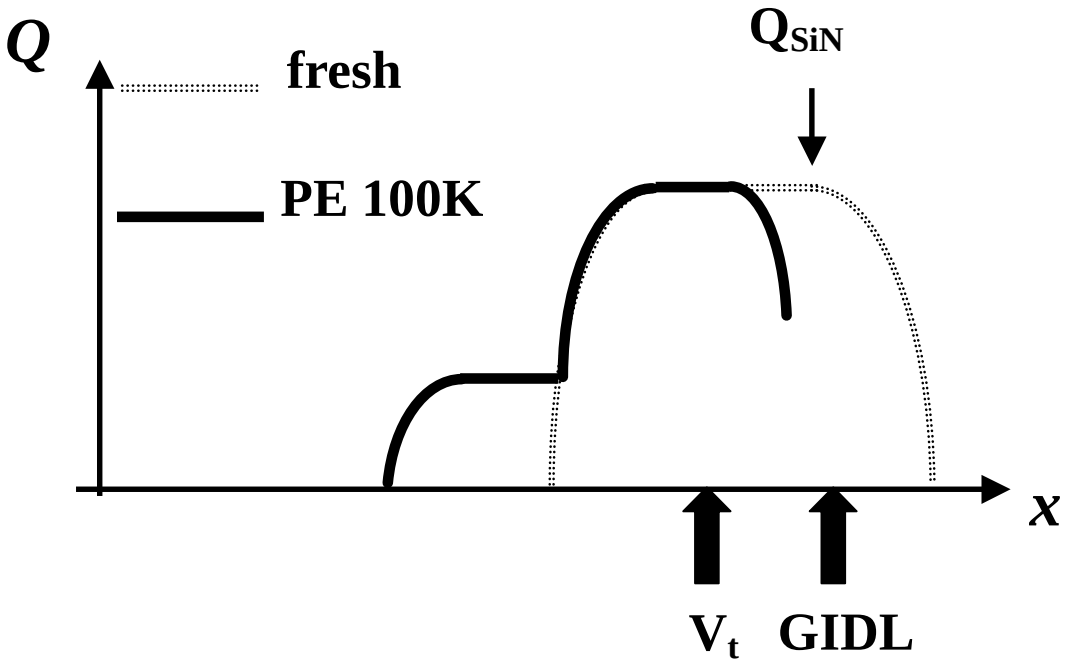


Fig. 2.7 Illustration of the charge distribution in the fresh and 100k P/E devices. The two devices are programmed to have the same threshold voltage.

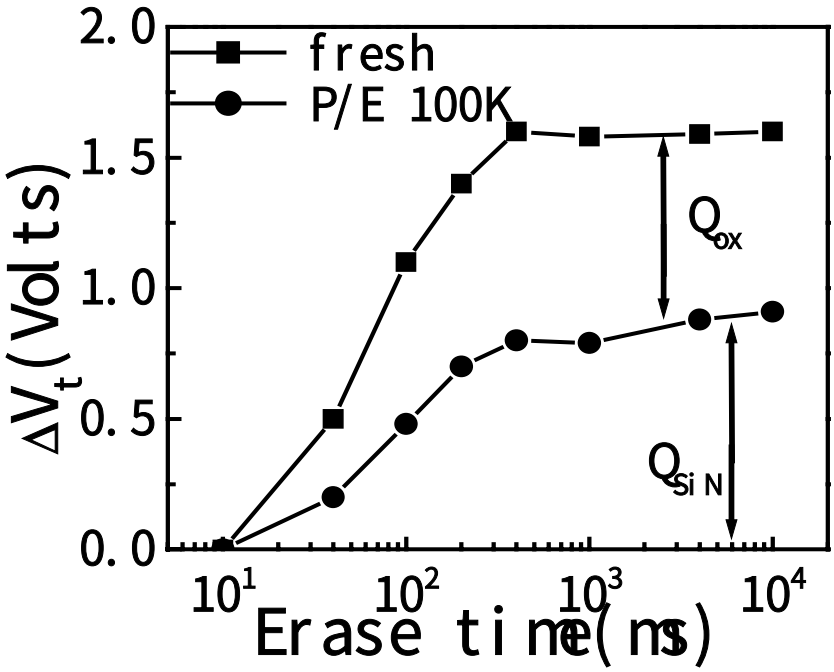


Fig. 2.8 The erase characteristics in the fresh and in the 100k P/E devices. The two devices have the same program - state threshold voltage.

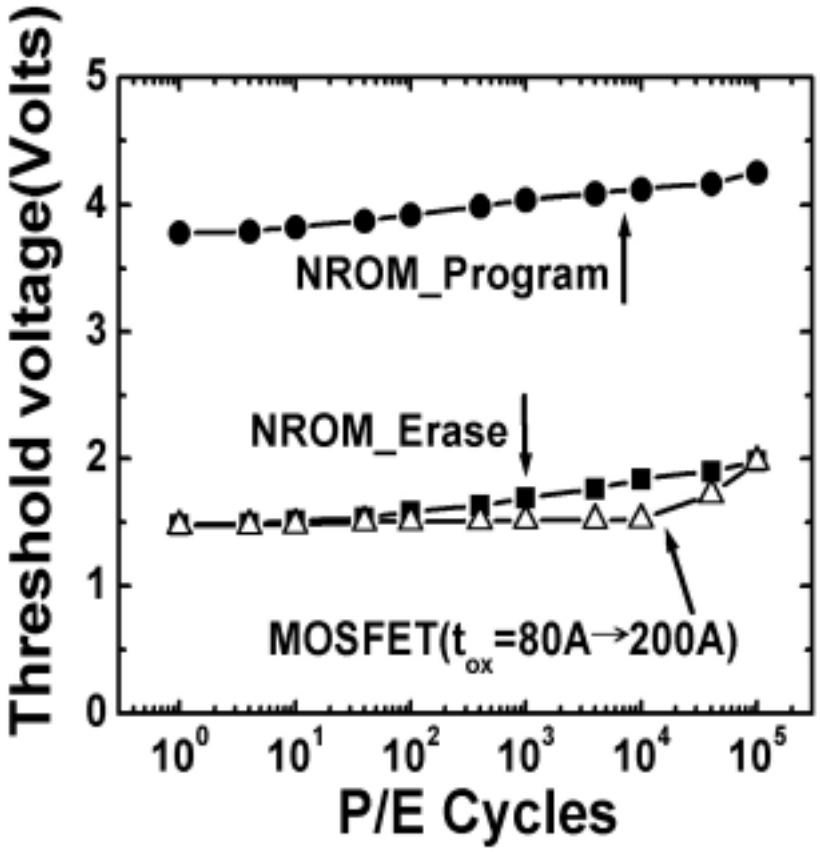


Fig. 2.9 Threshold voltage variation versus P/E cycle number in a conventional gate MOSFET and in a NROM.

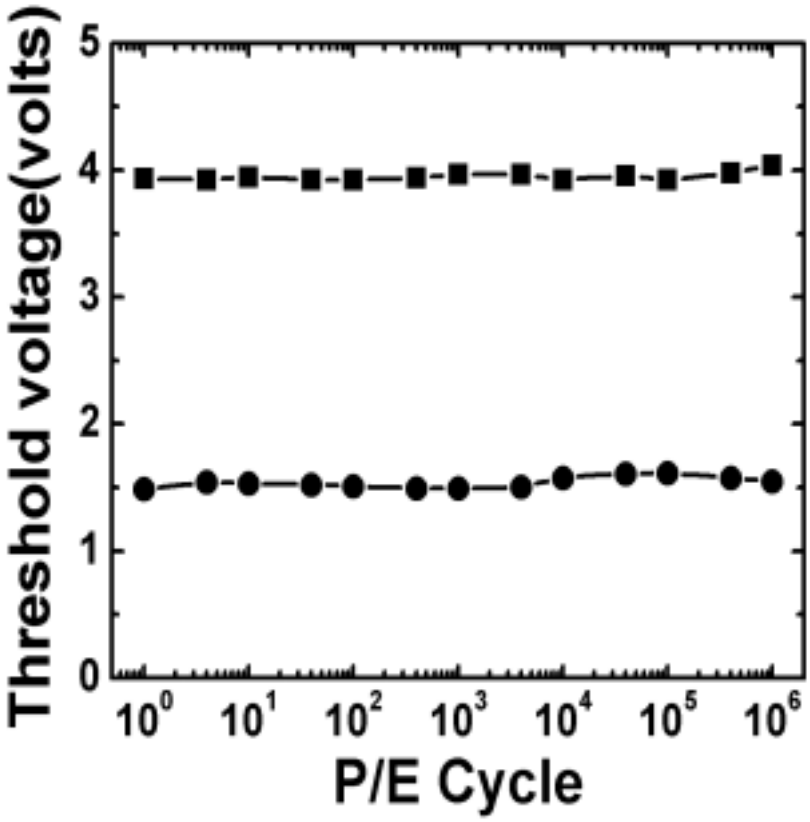


Fig. 2.10 Threshold voltage versus P/E cycle number in a NROM cell with a stronger erase bias

Chapter 3
Erase State Data Retention Loss

3.1 Introduction

As mentioned previously, the bottom oxide in the NROM cell is normally thicker than 40Å to avoid charge direct tunneling. The charge trapping area is very narrow, typically tens of nanometers. To allow for two-bit operation, the applied bitline voltage in reverse-read must be sufficiently large (>1.5V) to be able to "read-through" the trapped charge in the neighboring bit. Due to a thicker bottom oxide and higher read bitline voltage, some new reliability issues concerning erase-state data retentivity arise in the NROM cells. In this chapter, we will discuss two erase-state retention loss phenomena, room temperature (RT) threshold voltage drift and read-disturb. The responsible physical mechanisms will be investigated.

3.2 Room-Temperature Threshold Voltage Drift

3.2.1 Mechanism of V_t Drift

In a P/E stressed cell, the erase-state threshold is found to drift with storage time (Fig. 3.1). This retention loss exhibits logarithmic time-dependence but no temperature dependence (Fig. 3.2). This is why the drift is referred to as RT drift. Unlike a SONOS cell, the bottom oxide is sufficiently thick in the measured device and the drift cannot be explained by nitride hole back tunneling. Furthermore, we find that the V_t drift exhibits a peak around 1k P/E

cycles in Fig. 3.3. To understand this peculiar cycle number dependence, the readers should be reminded that it is well published in literature that positive trapped charge creation is dominant in tunnel oxide in the initial period of P/E stress. The appearance of the peak gives a clue that the V_t drift is related to positive charge creation in the bottom oxide. To explore the origin of the RT drift, V_t and GIDL techniques are used to monitor the charge variation in a fresh cell and in a cycled device respectively. The result is shown in Fig.3.4 (a) and Fig.3.4 (b). From the change of V_t and GIDL, it can be deduced that after P/E stress the net ONO charge above the n^+ region is positive and the net ONO charge above the channel region is negative. More exactly speaking, the ONO charge in the channel region comprises positive oxide charge (Q_{ox}) and negative nitride charge (Q_{SiN}). In storage, trapped holes in the bottom oxide (Q_{ox}) can escape to the Si substrate with time. The total ONO charge in the channel region therefore becomes more negative and thus threshold voltage increases with time. Based on the above physical picture, RT drift can be reduced by either decreasing Q_{ox} or decreasing Q_{SiN}. Fig. 3.5 shows the RT drift versus bottom oxide thickness. In Fig. 3.6, we varied the erase time to study the dependence of the RT drift on Q_{SiN}. For a prolonged erase time, Q_{SiN} is less and the RT drift is smaller.

3.2.2 Time Dependence of V_t Drift

To explain the observed time-dependence of the RT drift, the tunneling front model [18] is employed. In a P/E stressed device, the trapped hole in the bottom oxide can escape to the substrate via tunneling. Based on the tunneling front model, the threshold voltage shift caused

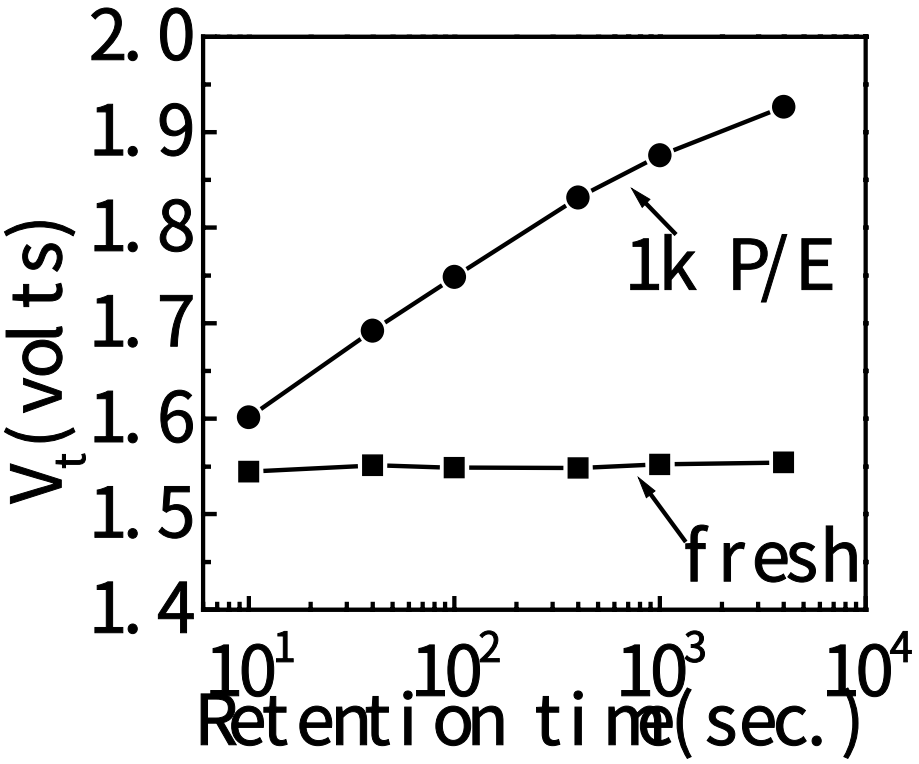


Fig.3.1 Erase-state threshold voltage drift versus retention time in a fresh device and in a 1k P/E device.

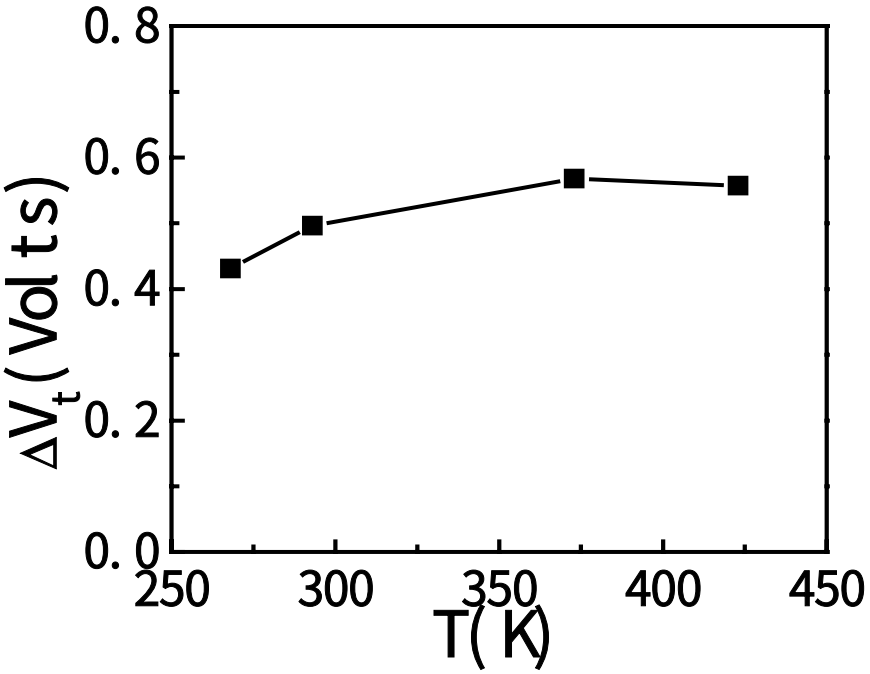


Fig.3.2 Temperature-dependence of the erase-state Vt drift. No significant change in Vt drift by varying temperature.

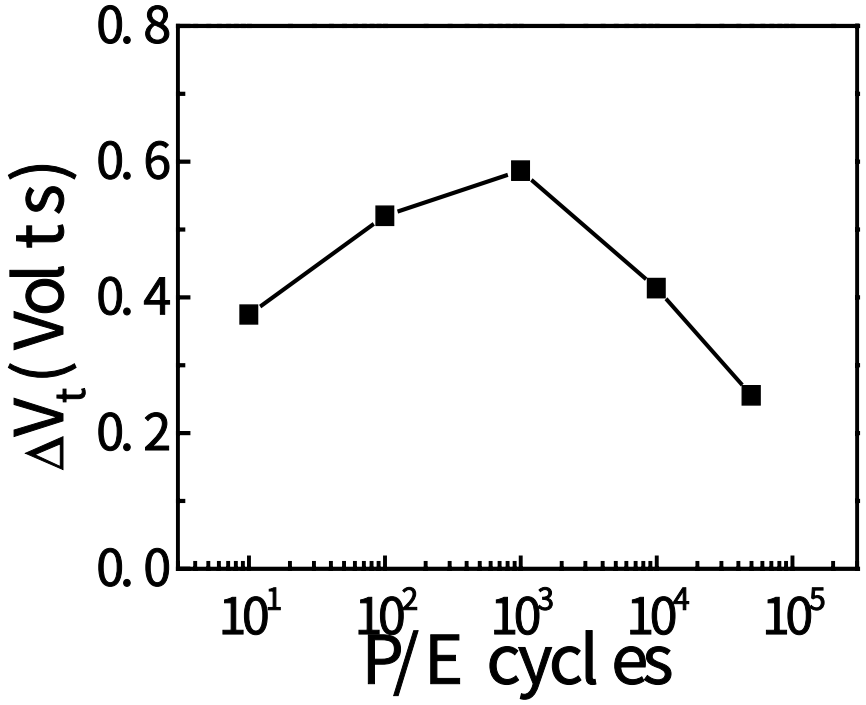
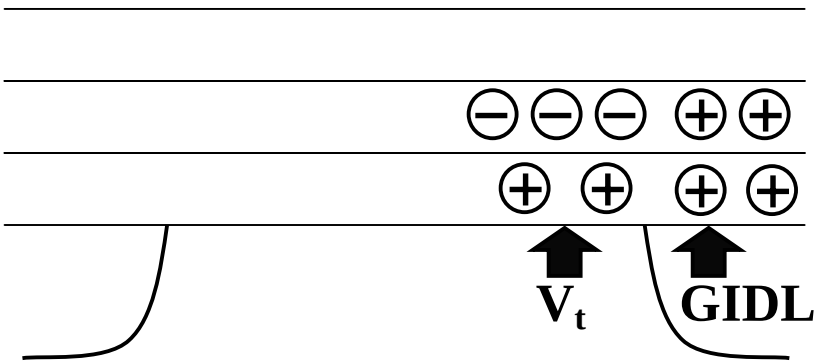


Fig.3.3 Cycling number dependence of the erase-state V_t drift. The thickness of bottom oxide is 90Å. It shows that the peak is around 1k P/E cycles.



(a)

	Fresh	1K P/E	Net charge
V_t	1.2V	1.4V	negative
GIDL	27.9pA	23pA	positive

(b)

Fig.3.4(a) Illustration of charge distribution in a 1k P/E cell.

(b) Measured V_t and GIDL in a fresh device and in a cycled device.

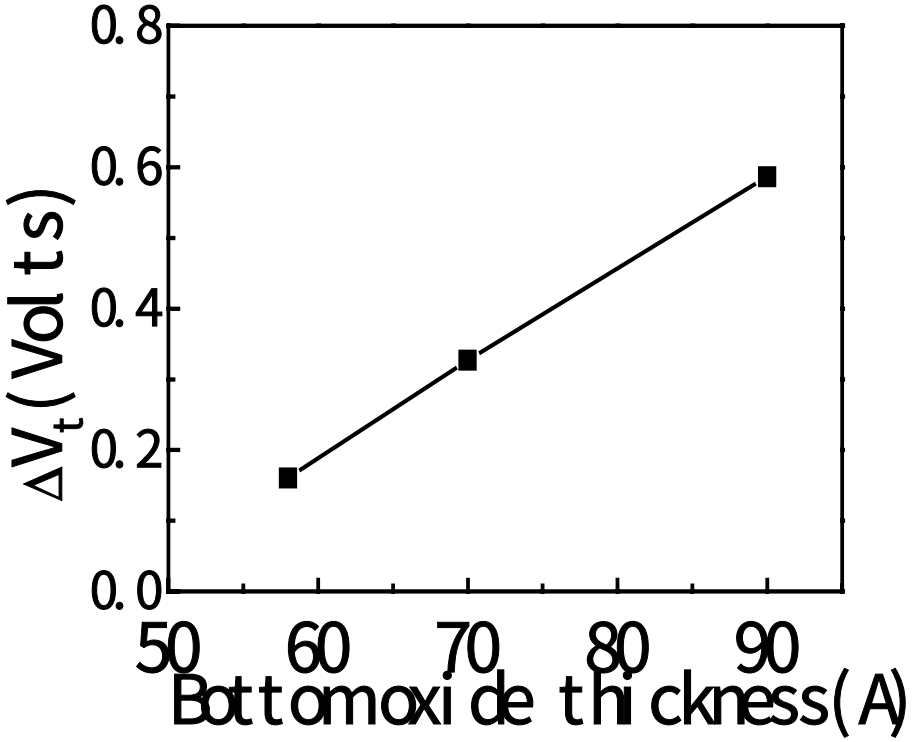


Fig.3.5 RT drift versus bottom oxide thickness in a 1k P/E cycled device. Retention time is 36 hours.

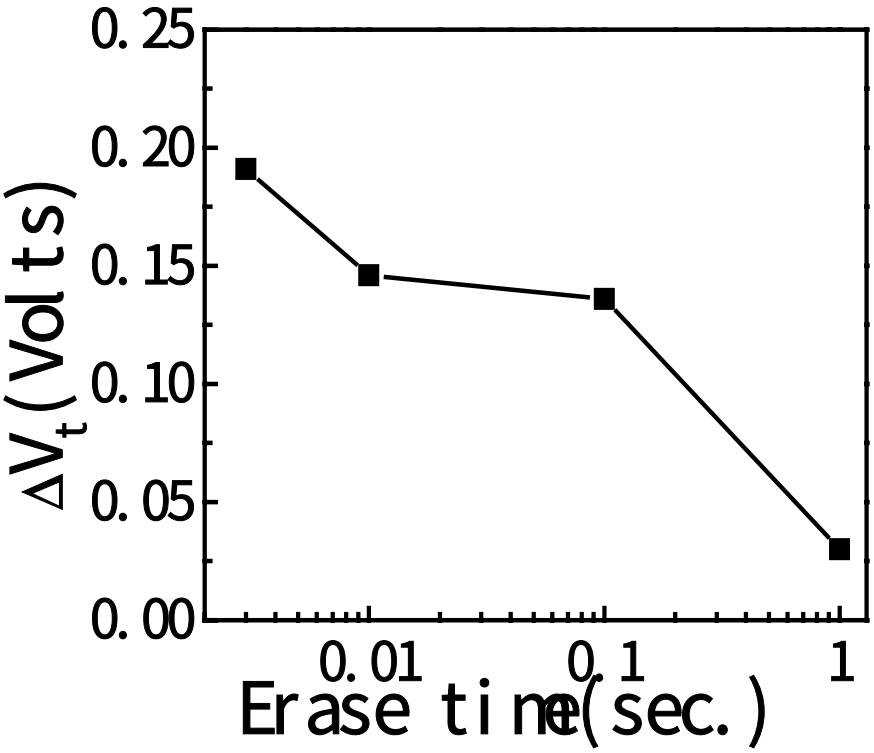


Fig.3.6 Dependence of RT drift on erase time in a 1k P/E cycled cell.

by valence band electron tunneling is illustrated by path A in Fig.3.7

$$\Delta V_{th} = -2.3 \frac{\overline{t_{ONO}}}{\varepsilon_{ONO}} \frac{q\hbar N_{ox}}{2\sqrt{2m^*(\phi_B + E_g)}} \log t \qquad (3.1)$$

and the threshold voltage shift caused by conduction band electron tunneling is illustrated by path B in Fig.3.7

$$\Delta V_{th} = -2.3 \frac{\overline{t_{ONO}}}{\varepsilon_{ONO}} \frac{q\hbar N_{ox}}{2\sqrt{2m^*(\phi_B)}} \log t \qquad (3.2)$$

3.3 Read-Disturb Effects in Erase State

Read-disturb effect is twofold in the NROM. The wordline voltage during read may enhance the RT drift in the neighboring bit. On the other side, the relatively large read bitline voltage may cause channel hot electron injection and result in a significant threshold voltage shift of the neighboring bit. The hot electron injection caused V_t shift follows either power-law time-dependence or logarithmic time-dependence. An analytical model based on positive oxide charge assisted channel hot electron injection is proposed to explain the observed power law time-dependence.

3.3.1 Commonality between V_t Drift and Read-Disturb

The RT drift and read-disturb have something in common. For example, the read-disturb

caused V_t shift is also smaller when the bottom oxide thickness is reduced (Fig. 3.8). Secondly, we performed RT drift measurement and the read-disturb measurement in the same device (1K P/E cycles) sequentially. No matter the RT drift or the read-disturb is measured first, the subsequent read-disturb or RT drift is significantly reduced (Fig. 3.9). Fig. 3.9 gives strong evidence that the mechanisms of RT drift and read-disturb should share the same physical origin. From the study in the preceding section, we believe that read-disturb is also related to positive trapped charge in the bottom oxide.

3.3.2 Drain Bias Dependence of Read-Disturb Behavior

In order to investigate the drain bias dependence of the read-disturb effect, two different read bias conditions (V_g=3.0V, V_d=2.5V and V_g=2.75V, V_d=1.6V) are applied.. We find that the read-disturb behavior changes with the read bias condition. At V_g=3.0V, V_d=2.5V, the read-disturb caused V_t shift follows a power-law time dependence (t^n) (Fig. 3.10) while at V_g=2.75V, V_d=1.6V the V_t shift follows a logarithmic time dependence (log (t)) (Fig. 3.11), respectively. The explanation is as follows; at a lower read drain bias, channel electric field is small and channel electron energy is relatively low. Such low energy electrons cannot surmount the barrier of the nitride conduction band, which is about 2eV above the Si conduction band. In this case, the read-disturb mechanism is quite similar to the RT drift process except for Vg acceleration. At a higher drain bias condition (V_g=3.0V, V_d=2.5V), channel electrons can gain sufficient energy from a large electric field to inject into the nitride

conduction band and then get trapped in the nitride. In the next section, we will develop the read-disturb model based on the channel hot electron injection into the SiN via positive charge assisted tunneling (PCAT).

3.3.3 PCAT Model in Read-Disturb

Positive oxide charges are created in the bottom oxide by P/E stress. The columbic potential of a positive oxide charge acts as a sequential tunneling center. The channel hot electron injection into nitride via PCAT is illustrated in Fig.3.12. I_{cat} is positive charge assisted electron tunneling current.

$$I_{cat} \propto t^{-P}, P = (\frac{m_e \phi_e}{m_h \phi_h})^{1/2} \tag{3.3}$$

The time dependence of the threshold voltage shift from I_{cat} injection is derived in the following.

$$\Delta V_{th} \propto \int I_{cat}(t)dt = \int t^{-P}dt = t^{1-P} = t^{n} \tag{3.4}$$

It is a general trend in literature to have $m_h \geq m_e$ [19-21] and $\phi_h \geq \phi_e$ [22, 18]. Thus the power factor P in Eq.3.3 is expected to be smaller than 1 and the extracted value of P in [23] is about 0.7. In other words, n is about 0.3, which is consistent with our measured result in Fig.3.10.

Because of two-bit per cell operation, the read-disturb effect in the following four modes should be assessed.

(A) One programmed bit and one erased bit (reading bit), as illustrated in Fig.3. 13(a)

(B) Two erased bits, as illustrated in Fig.3. 13 (b)

(C) Two programmed bits

(D) One erased bit and one programmed bit (reading bit)

The last two conditions are not our concern since the read current is low (<1μA).. The result for mode A and mode B is shown in Fig. 3.13. The worst read-disturb case is mode A due to a smaller initial read current. Read-disturb lifetime of about 3×10^4 seconds is obtained for a read failure defined as I_R<15uA.

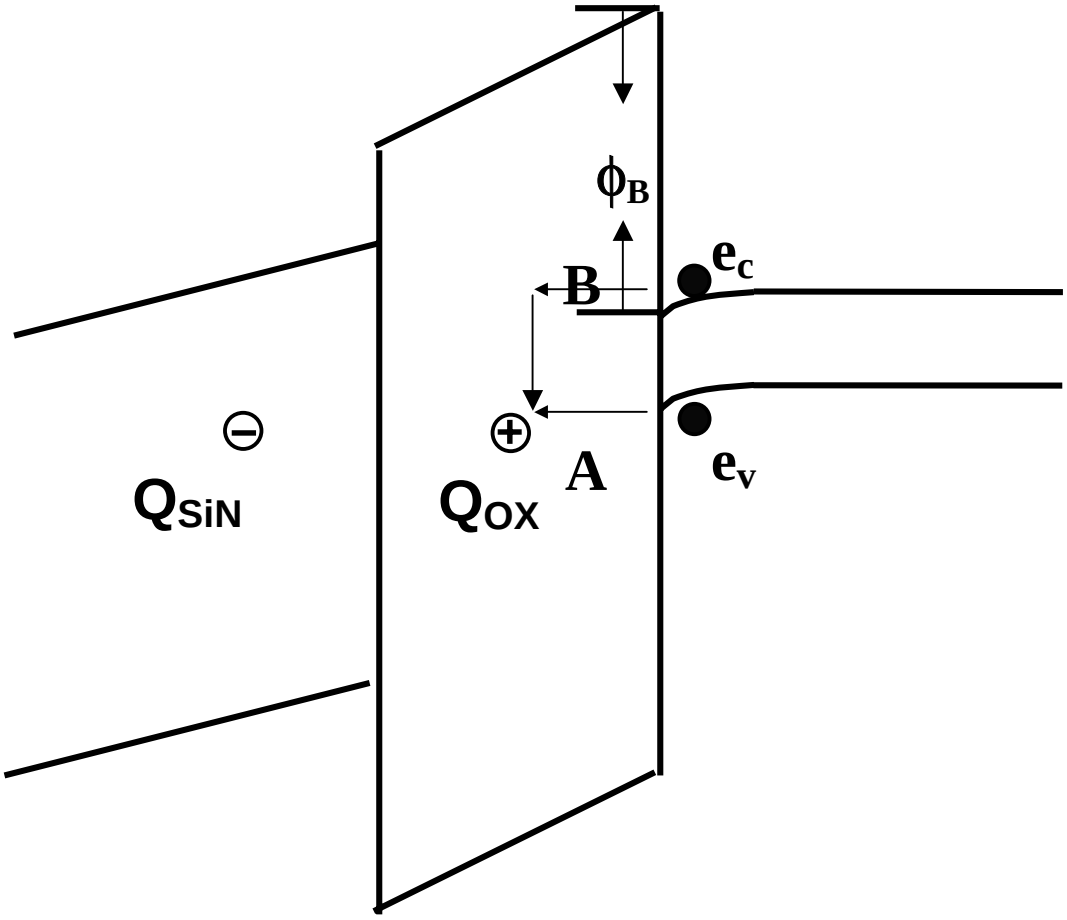


Fig.3.7 Schematic band diagram showing positive oxide charge and negative nitride charge in a 1k P/E cycled device. The electrons in valance band and conduction band can tunnel to recombine with positive oxide charge via path A and path B.

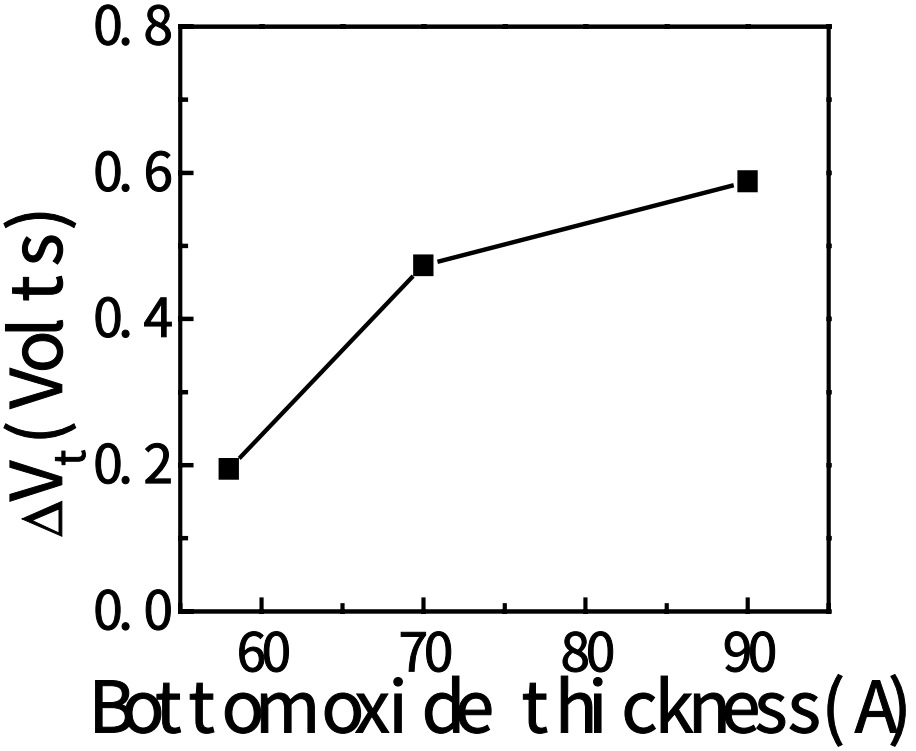


Fig.3.8 Read-disturb caused Vt shift as a function of bottom oxide thickness in a 1k P/E cycled cell. The read bias condition is V_g=2.75V, V_d=1.6V and read-disturb time is 10^4 sec.

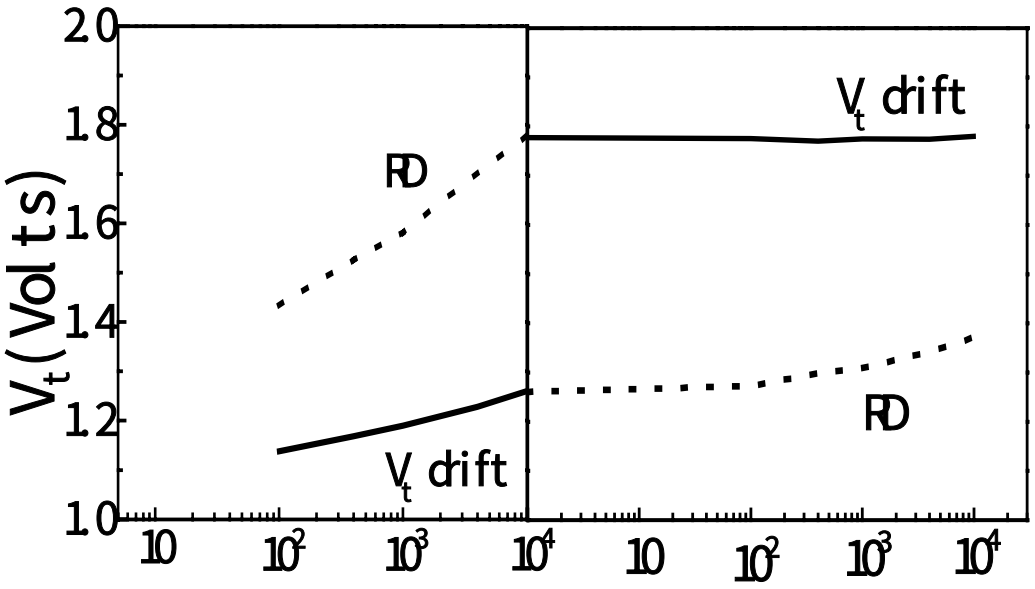


Fig.3.9 Temporal evolutions of Vt drift and read-disturb caused Vt shift. These two measurements are performed sequentially.

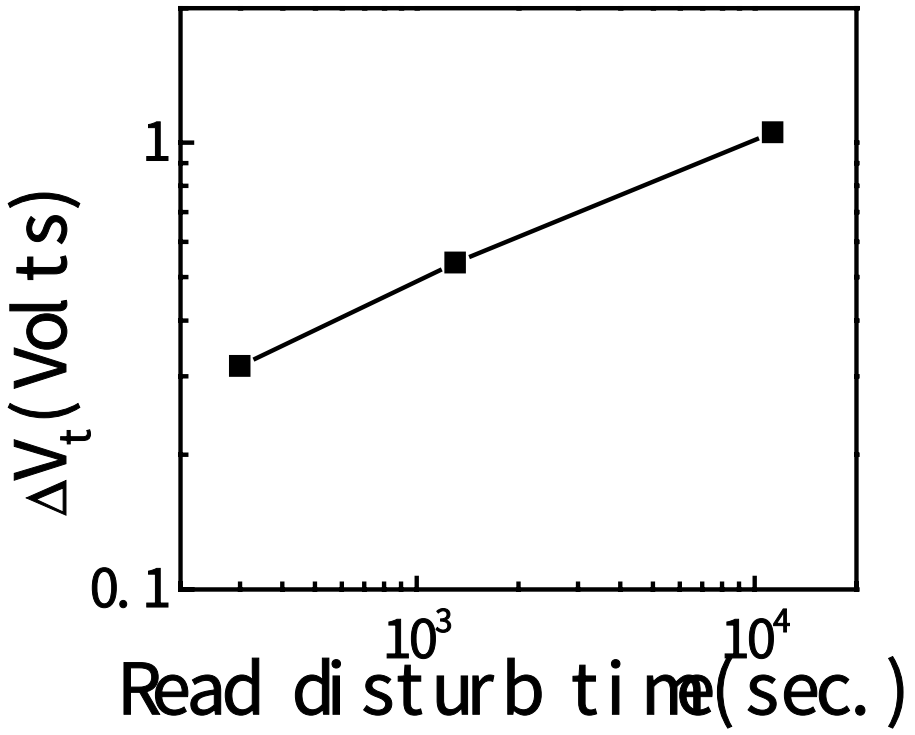


Fig.3.10 Dependence of Vt shift on read-disturb time in a 1k P/E cycled cell. Power-law time dependence (t^n) is obtained. The read bias condition is V_g=3V, V_d=2.5V.

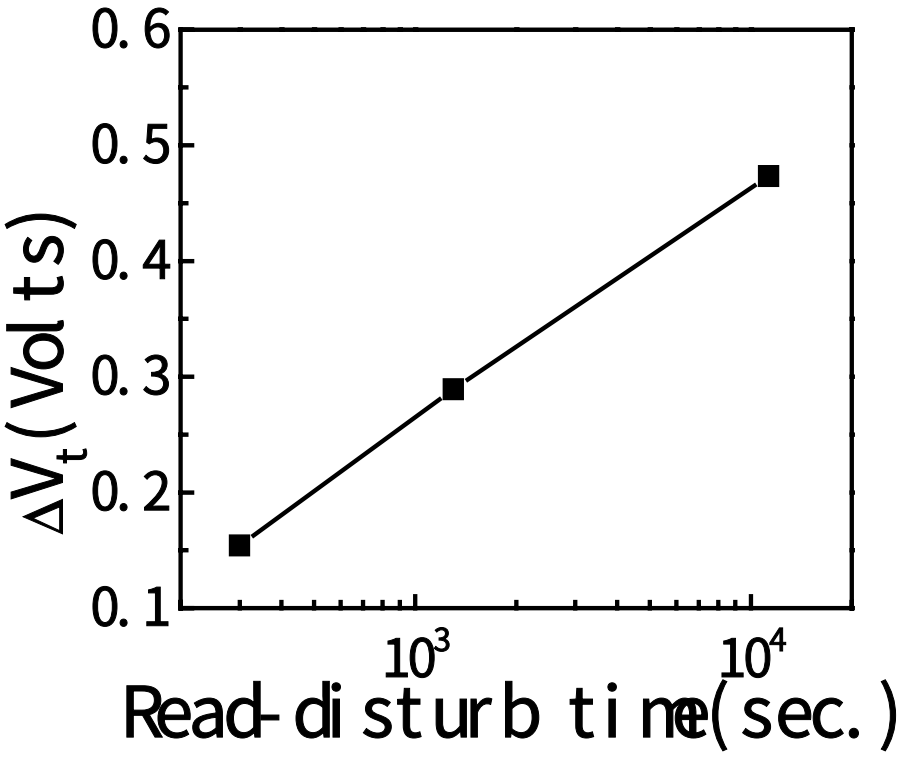


Fig.3.11 Dependence of Vt shift on read-disturb time in a 1k P/E cycled cell. Logarithmic time dependence (log(t)) is obtained. The read bias condition is V_g=2.75V, V_d=1.6V.

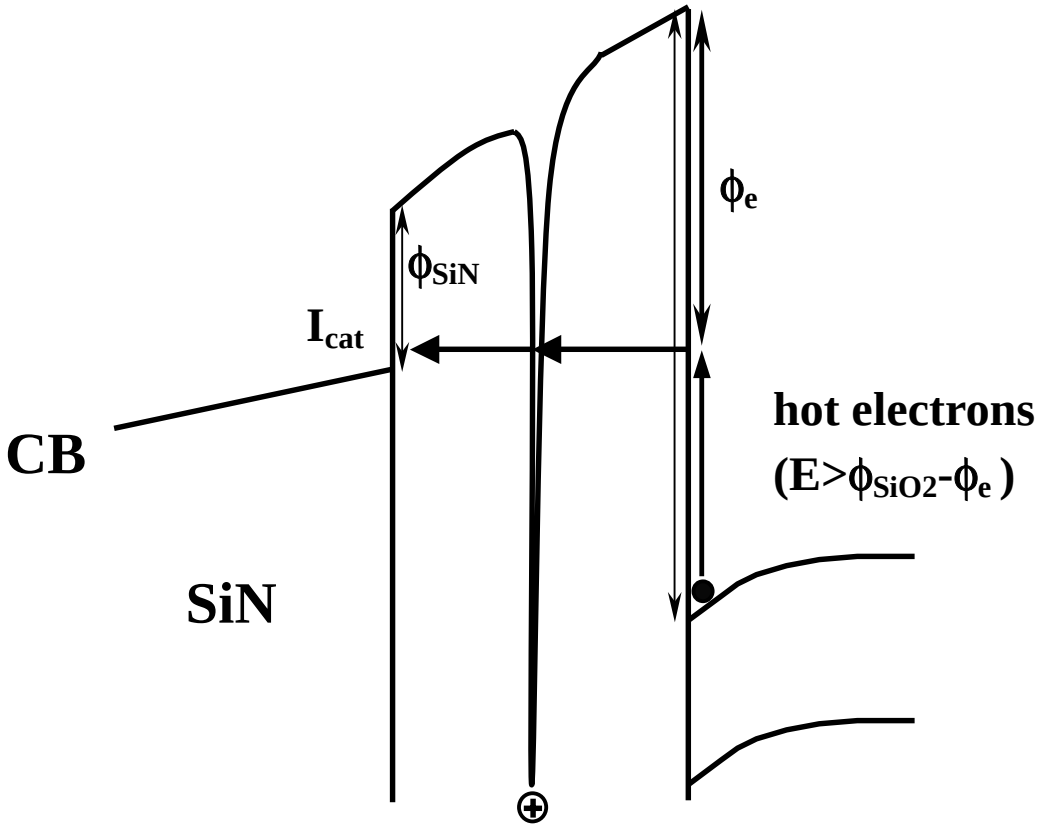
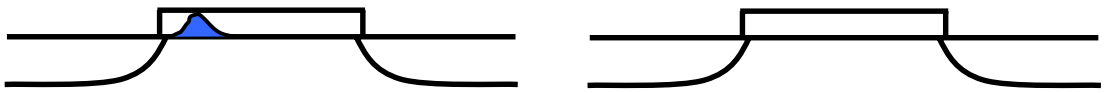


Fig.3.12 Illustration of positive charge assisted channel hot electron injection into the silicon nitride. I_{cat} denotes the positive-charge-assisted electron tunneling current.



(a) **(b)**

Fig.3.13(a) The cell has one programmed bit and one erased bit.

Fig.3.13(b) The cell has two erased bits. The read bitline voltage is applied at the source.

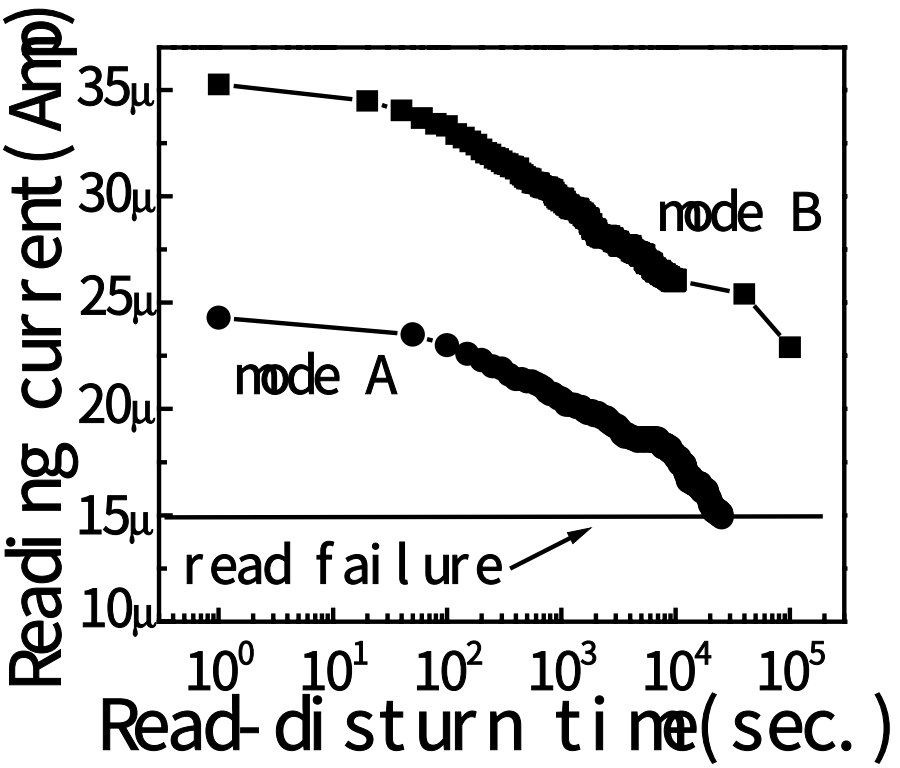


Fig.3.14 The reduction of read current versus read-disturb time for mode A and mode B disturb conditions. Read failure is defined as read current less than 15μA.

Chapter 4
Program State Charge Loss

4.1 Introduction

One of the major advantages of the NROM cell, as compared with the floating gate flash EEPROM, is the better retentivity due to localized charge trapping [24]. The retention loss characteristics of the NROM are determined by two factors. (i) oxide charge detrapping (Q_{ox}) [25], and (ii) nitride charge loss (Q_{SiN}) [26]. The amount of created oxide trapped charge is dependent on P/E stress and oxide quality. The nitride charge loss mechanism in the NROM structure is different from that in the SONOS. In a SONOS cell, nitride charge loss is through direct tunneling to Si substrate. In the NROM cell, due to a thick bottom oxide, nitride charge escape to the substrate has to go through a two-step process, i.e. electron emission from nitride traps to the nitride conduction band and subsequently escape to the substrate via oxide trap assisted tunneling. Thus, nitride charge loss is also dependent on trap creation in the bottom oxide. Fig. 4.1 shows the retention loss versus P/E number. At low P/E stress, oxide trap creation is minimal and thus charge retention loss is small.

4.2 Nitride Charge Retention Loss

4.2.1 Movement of Trapped Nitride Charge

The retention loss occurs either due to charge escape in the vertical direction (vertical

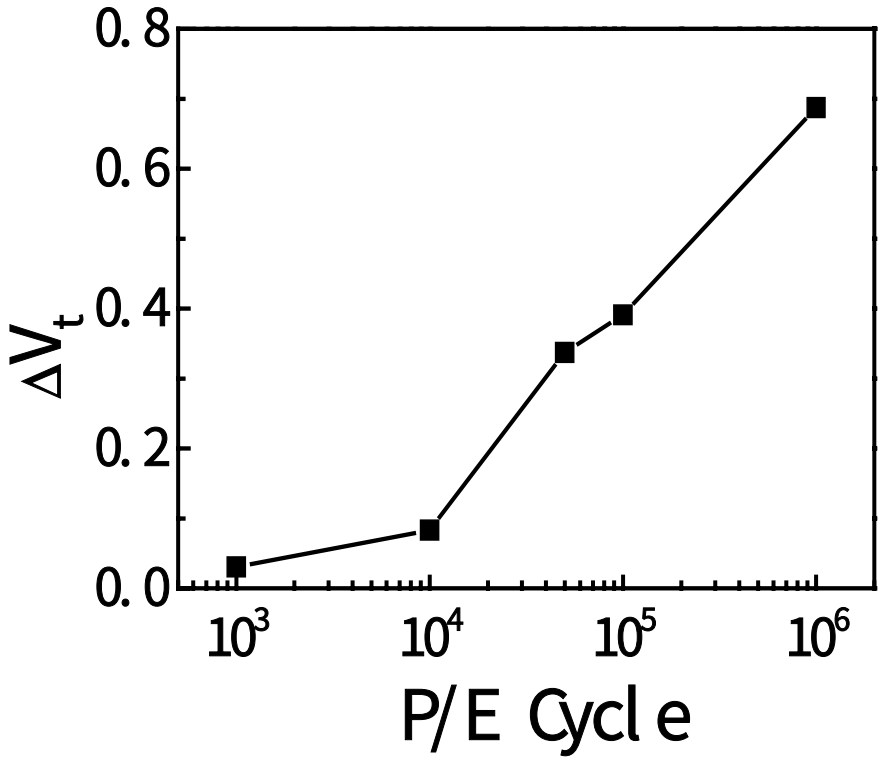


Fig. 4.1 Program-state retention loss versus P/E cycles.

retention loss [27]) or due to lateral redistribution of the trapped charge within nitride (lateral retention). Recently, Eitan's group makes efforts to investigate the cause of the charge loss in NROM cells [11]. They claimed that the root cause of the threshold voltage lowering is lateral spread of stored charges since vertical retention is guaranteed by adopting a thick bottom oxide to avoid charge direct tunneling. Their argument is definitely correct in a fresh cell. However, it's not straightforward in a cycled cell due to the presence of oxide trap assisted tunneling.

The lateral distribution of the trapped nitride charge can be deduced at least qualitatively by the dispersion of the threshold voltage versus drain bias. As drain bias increases, the junction depletion region extends further into the channel. The nitride charge above the depletion region is "masked" and does not affect the threshold voltage. Fig. 4.2 shows the measured threshold voltage versus drain bias in a fresh device. To enhance charge movement in the nitride layer, the sample was baked at 85C for 2000 sec. The V_t-Vd after the bake is shown in the figure for a comparison. No significant change is noticed. The result in Fig. 4.2 suggests that lateral movement of the nitride charge is insignificant. We also measured the V_t-Vd in a 100k P/E device (Fig. 4.3). Similarly, lateral movement of the nitride charge is not observed. However, we observe a slight threshold voltage reduction at 85C bake, an evidence of charge loss in the vertical direction. Interestingly, if we applied a negative gate bias of 3V during bake, a significant threshold voltage decrease is found in Fig. 4.3. From the above findings, we believe that the data retention loss is caused by charge escape in the vertical direction, since the application of a vertical field (Vg=-3V) apparently has a large influence

on charge retention capability.

Next, we would like to investigate the influence of vertical field on charge retention loss in program state. Three different gate biases are applied in the retention measurements. Fig.4.4 shows the threshold voltage evolution with retention time in a fresh cell. No charge loss is observed for all three gate biases. The reason is that the bottom oxide in the fresh device is clean. As pointed out earlier, nitride charge loss is improbable without oxide trap assisted tunneling. At low P/E cycles, the bottom oxide plays a blocking role for nitride charge loss. In the 100k P/E device, apparent gate bias dependence of charge retention loss is obtained in Fig.4.5. As a conclusion, vertical retention loss is a dominant mechanism in a P/E cycled cell, which exhibits strong vertical field dependence.

The following measurement provides another evidence to exclude the possibility of lateral movement in the retention loss. Here, we use uniform channel FN injection rather than hot electron injection for programming. In this way, the injected nitride charge has a uniform distribution. The possibility of lateral movement can be ruled out completely in this case. Again, we use GIDL and GISL [28] to monitor the variation of charge in the two ends of the channel during retention measurement. Fig. 4.6 shows the measured result in a fresh cell. The GIDL/GISL are constant in the entire measurement period. In a P/E stressed device (stressed at the drain side), the threshold voltage and GISL still keep unchanged during the measurement, but GIDL decreases with time, as shown in Fig.4.7. The threshold voltage does not change because only the drain side is damaged and charge loss takes place in the drain side. The potential barrier in the channel region is mostly unaffected. Similarly, GISL does not

change with time since GISL is affected only by the charge at the source end. This distinctly different feature of GISL and GIDL in Fig. 4.7 implies that the retention loss is correlated with oxide defects created by P/E stress. In summary, there are three factors affecting the nitride charge loss; (1) temperature, (2) vertical field, and (3) the damage due to cycling stress. Temperature will accelerate trapped charge emission rate but on the other side may cause oxide trap annealing and reduce the retention loss [29]. To improve data retention lifetime, the nitride internal electric field in program state should be lowered. The approach is to increase the thickness of top oxide or to reduce device initial threshold voltage.

4.2.2 Data Retention Model

In this section, we will focus on the modeling of nitride charge detrapping processes in a NROM device. In our discussion, it's assumed that blocking oxide is thick enough to prevent any charge loss. All four device terminals are grounded when devices are in the retention mode. The nitride film is initially filled with injected electrons.

Fig.4.8 shows the retention characteristics at different P/E cycles. The cycling number and temperature dependence in Fig.4.8 implies that the stored nitride charge loss is through thermionic-field emission (Frenkel-Poole model [30]) and subsequently oxide trap assisted tunneling [31]. These processes are illustrated in Fig.4.9. To confirm the field effect on the nitride charge detrapping, we monitor the V_t evolution with time for different applied gate bias (Fig.4.10). Here, the P/E number is 100k and oxide trap assisted tunneling is assumed to

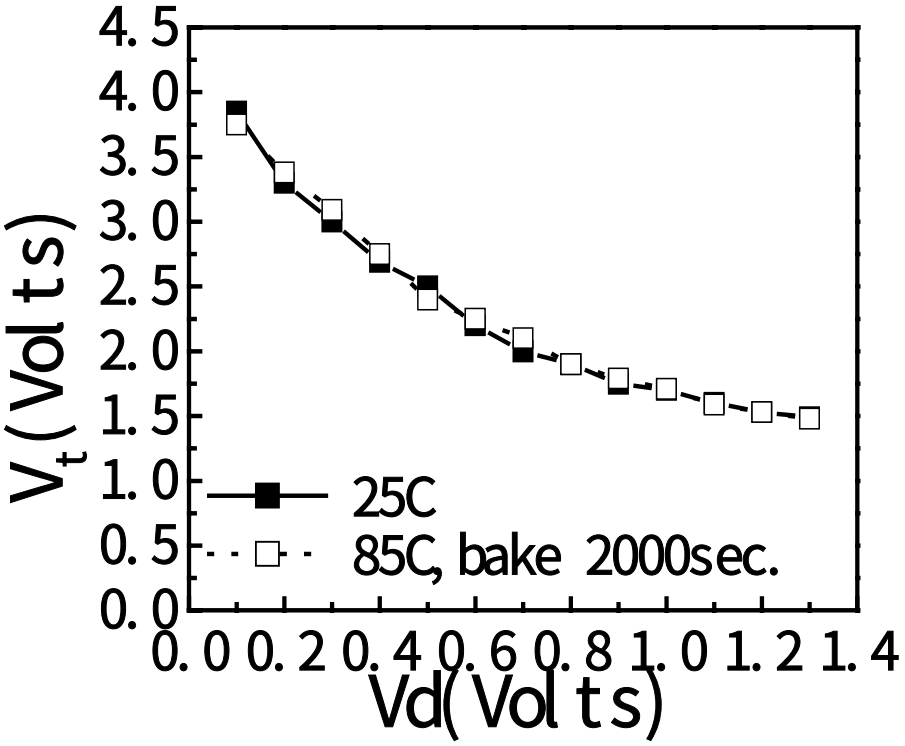


Fig. 4.2 Threshold voltage plotted against drain bias in a fresh device. T=25C and 85C.

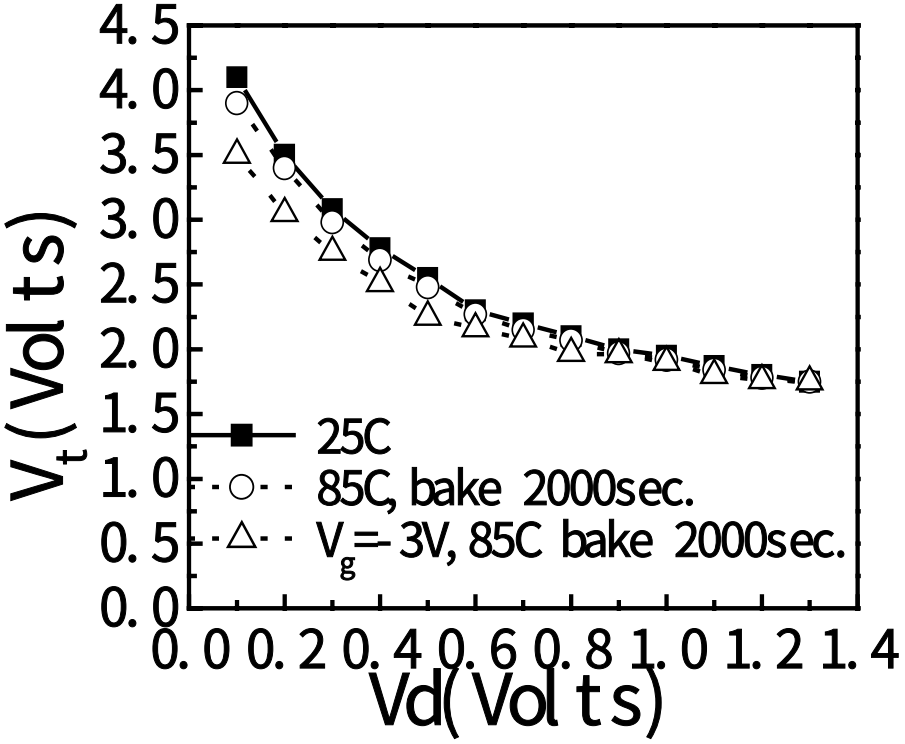


Fig. 4.3 Threshold voltage versus drain bias in a 100k P/E cell..

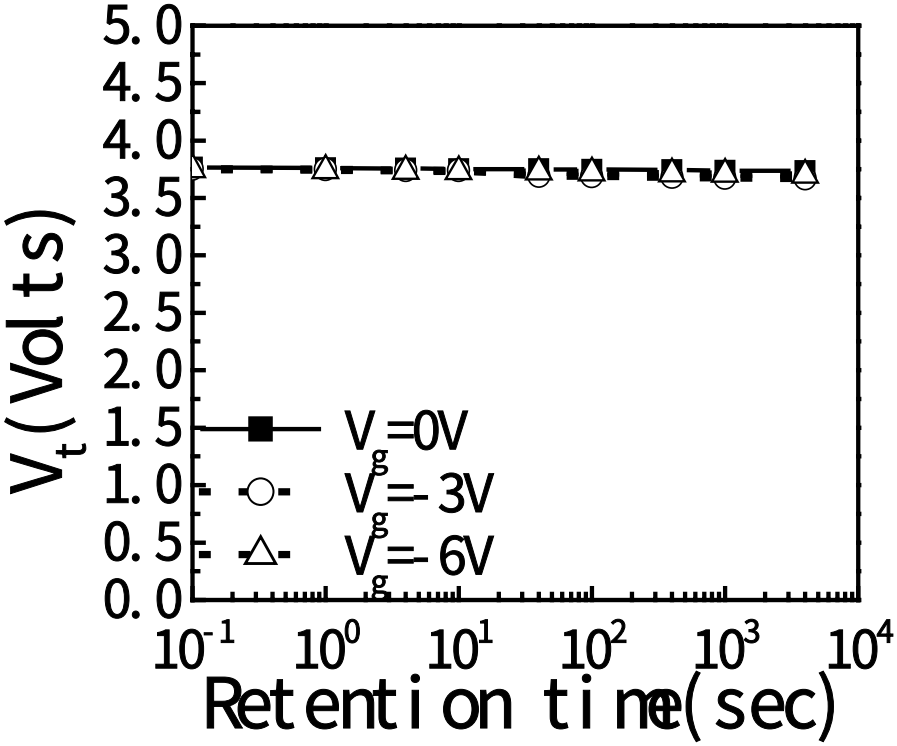


Fig. 4.4 Dependence of threshold voltage on retention time in a fresh cell. Gate bias is 0V, -3V and –6V in retention measurement state.

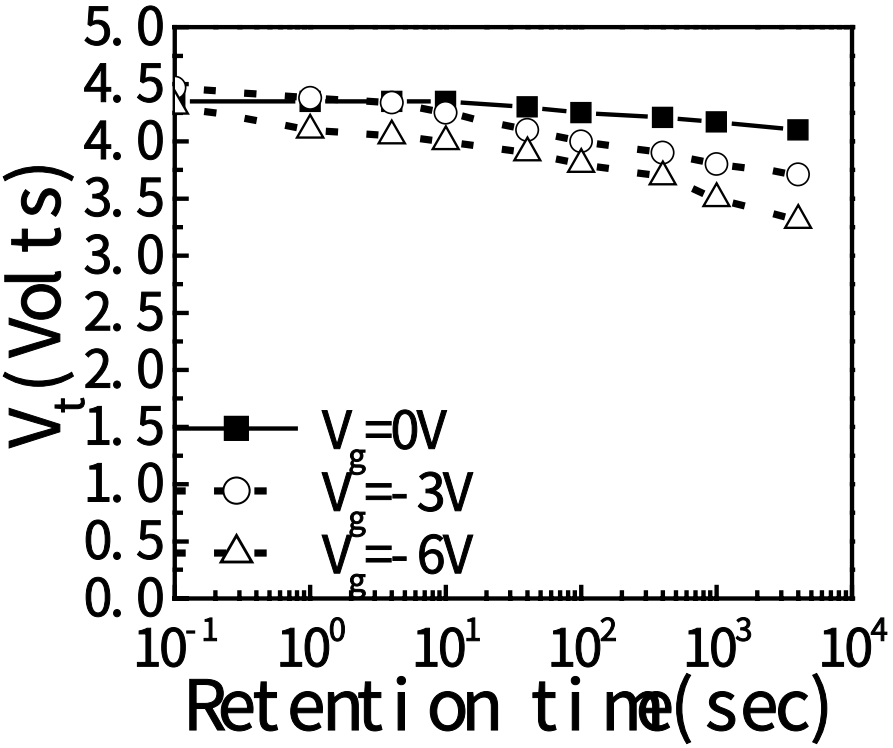


Fig. 4.5 Dependence of threshold voltage on retention time in a 100k P/E device. Retention gate bias is 0V, -3V and -6V.

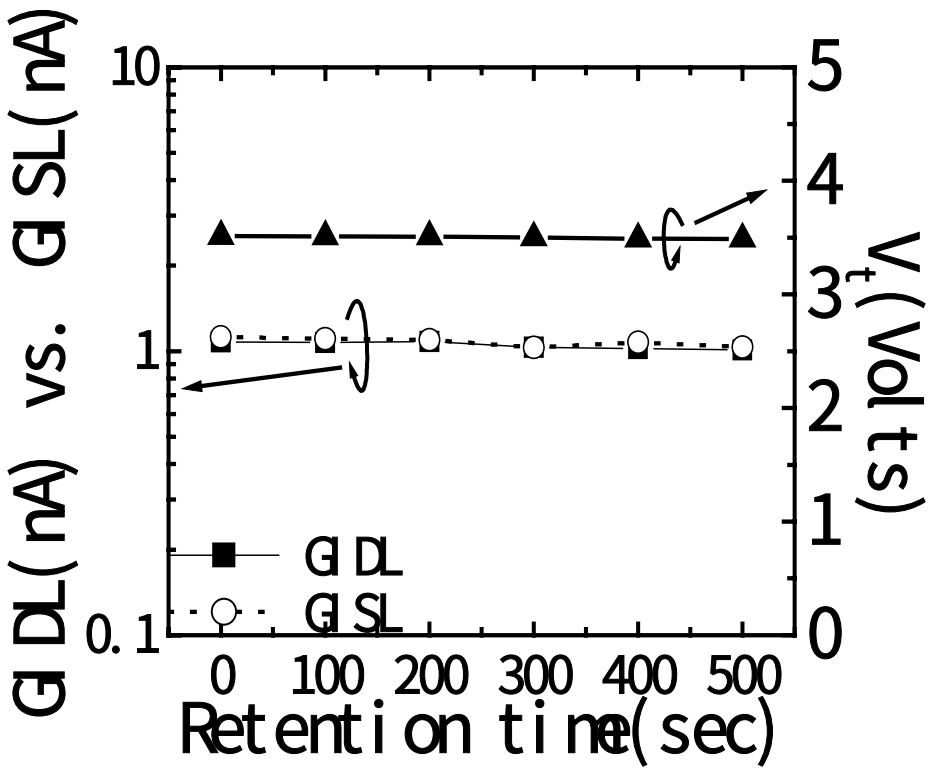


Fig. 4.6 Dependence of GIDL/GISL and threshold voltage on retention time in a fresh device.

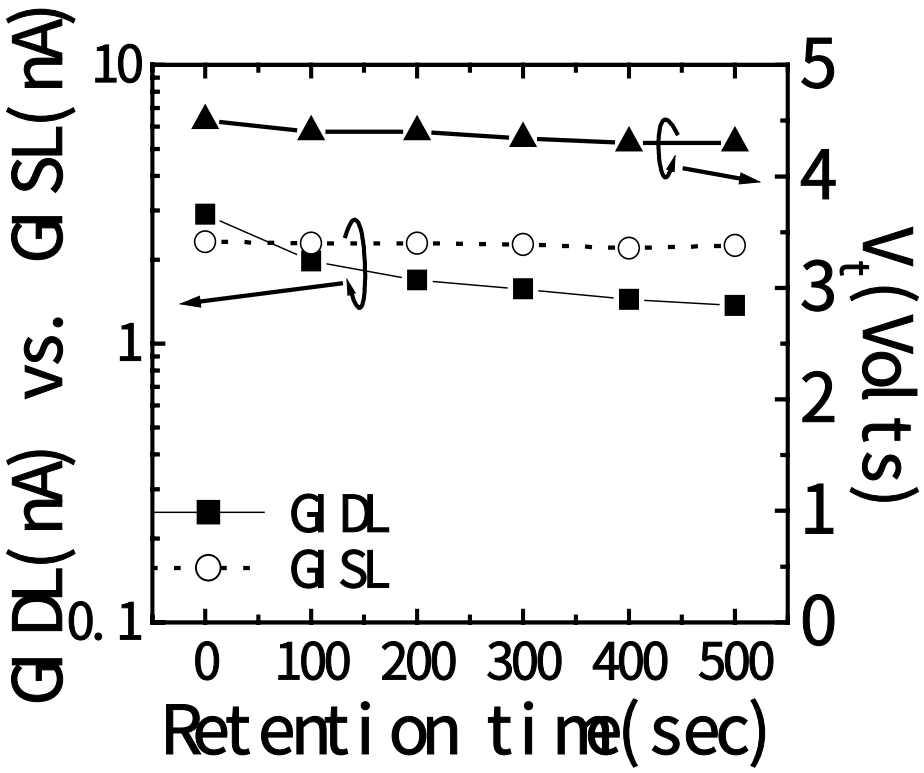


Fig. 4.7 Dependence of GIDL/GISL and threshold voltage on retention time in a 100k P/E device.

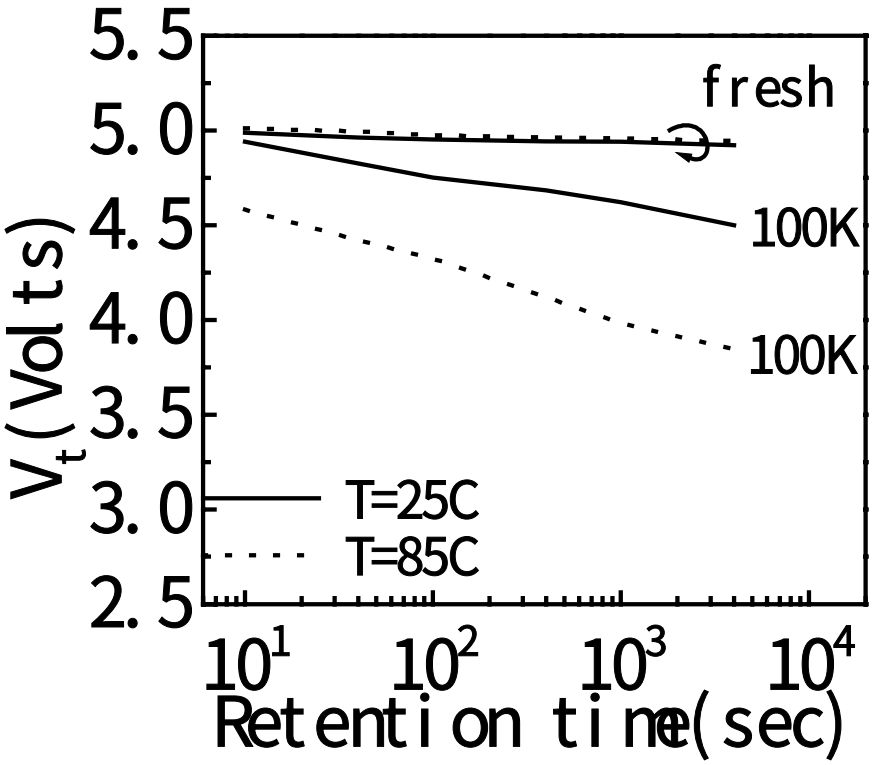


Fig. 4.8 Program-state charge loss characteristics in a fresh and a 100k P/E NROM cells. T=25 and 85.

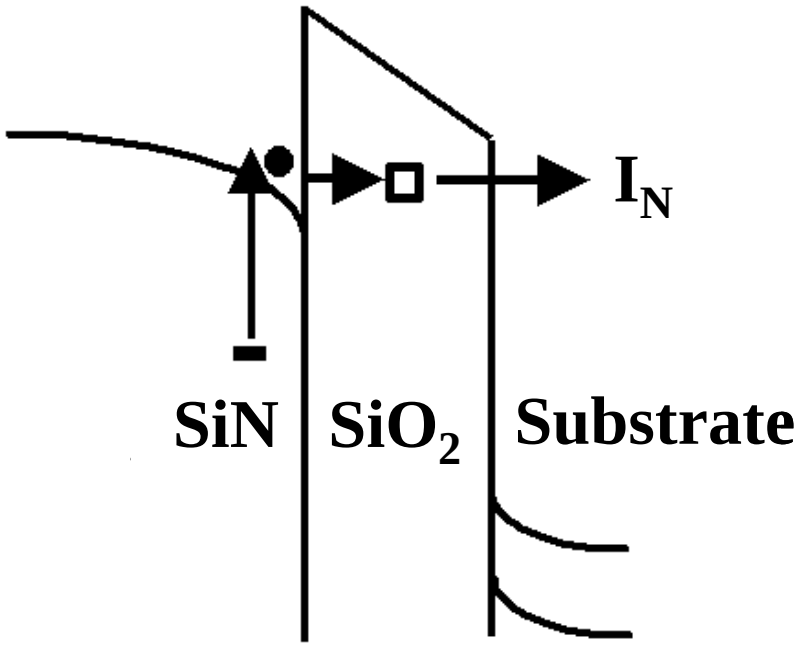


Fig. 4.9 Illustration of stored charge loss by Frenkel -Poole-emission and subsequently oxide trap assisted tunneling.

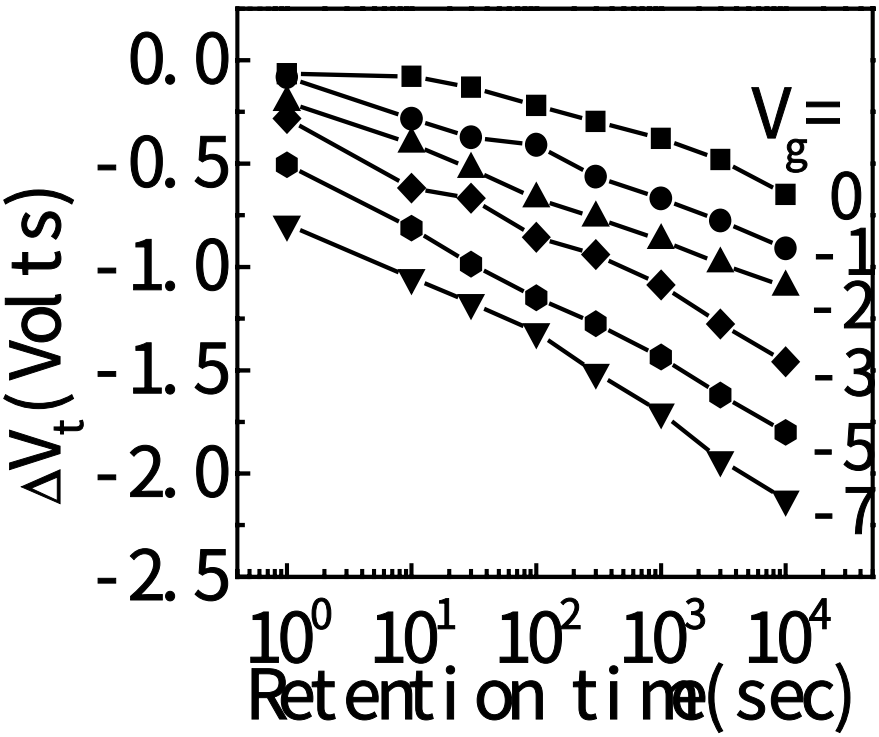


Fig. 4.10 Program-state charge loss characteristics at different applied gate bias in a 100k P/E device.

be sufficiently fast. A square-root dependence of the V_t loss on electric field is obtained (Fig.4.11). This square-root dependence is consistent with the Frenkel-Poole emission.

One of the reasons to study the field dependence of nitride charge detrapping is to establish an acceleration test method to predict long memory retention time. From Fig.4.11, V_g is apparently an effective acceleration factor for lifetime measurement. If we assume that during the discharge time, t, all traps with time constants less than t will be completely emptied while all other traps are unaffected, the memory retention time will be equal to the nitride charge emission time. The nitride charge emission time can be expressed by Eq. (4.1).

$$\tau_N = \tau_0 \exp((\phi_N - q(qE/\pi\varepsilon)^{1/2}/kT) \qquad (4.1)$$

The retention lifetime versus the square-root of electric field is plotted in Fig. 4.12. The symbols represent measured result and the fitting straight lines are derived from Eq. (4.1). The extrapolated memory retention time (i.e. at V_g=0V) is about 5×10^6 sec. for ΔV_t=1.5V and is above 10 years for a reliability margin of ΔV_t=2V. Finally, the feasibility of temperature acceleration is studied. Due to the significant oxide trap annealing at an elevated temperature (=150C), temperature acceleration is not appropriate for lifetime measurement of the NROM cell.

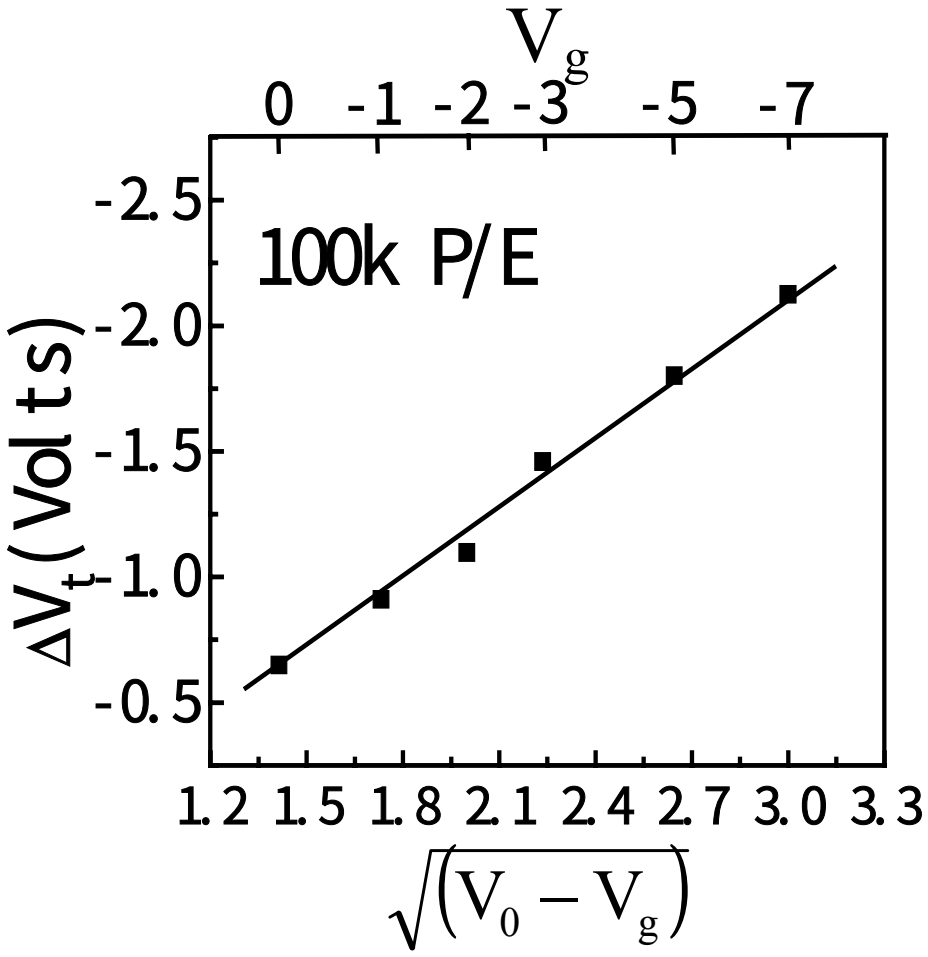


Fig. 4.11 Program-state retention loss plotted against applied gate bias. Retention time is $1x10^4$ sec.. In this figure, V_0 is the built-in potential and the x-axis corresponds to the square root of electric field. In the measured device, program state Vt is 5.0V and V_0 is about 2V.

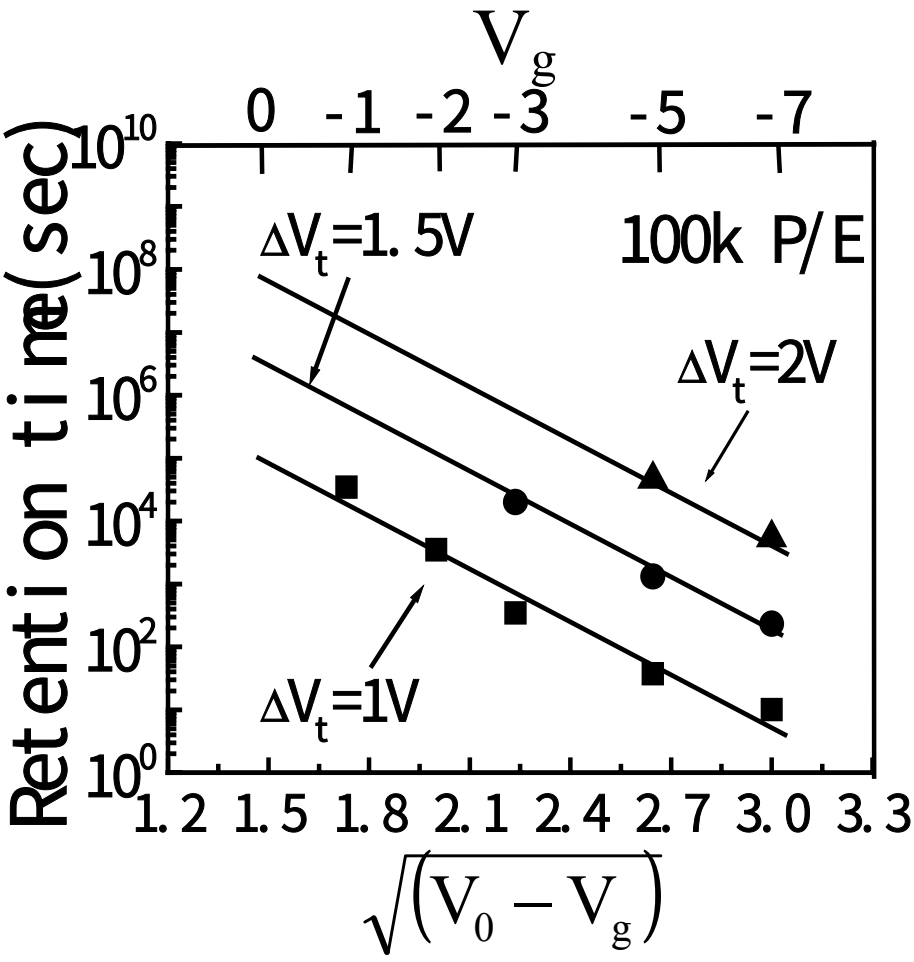


Fig. 4.12 The charge storage lifetime versus applied gate bias. Retention lifetime is defined as ΔV_t=1V, ΔV_t=1.5V and 2.0V, respectively. V_0 is defined in Fig. 3.11.

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Appendix

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Data Retention Behavior of a SONOS Type Two-Bit Storage Flash Memory Cell

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Abstract

Data retention loss mechanisms in a 2-bit SONOS type flash EEPROM cell with hot electron programming and hot hole erase are investigated. In erase (low-V_t) state, a threshold voltage drift with storage time is observed after P/E cycling stress. Positive trapped charge creation in the bottom oxide is found to be responsible for the drift. In program (high-V_t) state, data retention loss is attributed mostly to nitride charge escape by Frenkel-Poole emission and oxide trap assisted tunneling. A square-root dependence of the nitride charge loss on electric field is obtained. A V_g-acceleration method for retention lifetime measurement is proposed.

Introduction

Recently, nitride-based trapping storage flash memory cells have received much interest for smaller cell size, less fabrication complexity, no drain induced turn-on and better cycling endurance [1-4]. In a conventional SONOS structure, charges are stored uniformly in the nitride layer. This SONOS concept has recently evolved into a localized trapping [2] and two-bit storage [3] technology. This special type SONOS cell (referred as Multiplex Virtual Ground **AND** (MXVAND) flash in this work) is made of a n-channel MOSFET with an oxide-nitride-oxide gate dielectric structure, as illustrated in Fig.1. The charges are stored *locally* in the nitride layer above the n^+ source/drain junctions. Unlike a conventional SONOS cell, the bottom oxide of this cell is sufficiently thick to avoid charge direct tunneling. Channel hot electron injection and band-to-band hot hole injection [2,3] are utilized for programming and erasing respectively (Table 1). Two-bit operation is achievable with a reverse read scheme [3]. The endurance of the operation window is shown in Fig. 2. In this paper, we will investigate reliability issues and accelerated test methods for this cell.

Erase-State Threshold Voltage Drift

In a P/E stressed MXVAND cell, erase-state threshold voltage (V_t) is found to increase with retention time (Fig.3). This V_t drift cannot be simply explained by nitride hole back tunneling [5] as in a conventional SONOS cell due to a large bottom oxide thickness (7nm). To explore the origin of this drift, we measure the erase-state GIDL current and V_t in a fresh cell and in a P/E stressed cell (Table 2). From the change of GIDL and V_t, it can be deduced that after P/E stress the ONO layers above the n^+ drain region should possess net positive charge while the ONO above the channel has net negative charge. Moreover, we notice that the V_t drift exhibits a peak around 1k P/E cycles in Fig. 4. Since positive oxide charge creation is dominant in the initial period of P/E stress [6], the appearance of the peak strongly implies that the V_t drift is related to positive trapped charge generation in the bottom oxide. The proposed mechanism for the erase-state V_t drift is shown in Fig.5. The stress created positive trapped charge can escape from the bottom oxide to the substrate via tunneling, thus resulting in a substrate current I_h. The total ONO charge in the channel region therefore becomes more negative as time increases. Based on the tunneling front model [7], the V_t drift due to I_h has a logarithmic time-dependence as follows.

$$\Delta V_t(t) = 2.3\frac{1}{C_{ono}}\frac{qhN_{ox}}{2\sqrt{2m\phi_{ox}}}\log(t) \qquad (1)$$

where ϕ_{ox} denotes the energy level of the positive trapped charge and N_{ox} is the charge density. The *log(t)* dependence is in agreement with the measured result in Fig. 3.

At a positive gate bias (for example, a read condition), another component I_{est} in Fig.5 occurs, representing positive oxide charge assisted electron tunneling current [8] from the substrate to the SiN conduction band. Here, we use a charge separation technique (Fig. 6) to monitor I_h and I_{est} in erase-state separately. The measured I_g(=I_{est}+I_h) and I_t(=I_h) are plotted in Fig.7. Note that the positive oxide charge detrapping current (I_h) follows a 1/t time-dependence and is nearly independent of an oxide field (Fig.8).

As V_g increases, the I_{est} may arise drastically (Fig. 8) and results in a large V_t shift. Fig. 9 shows the wordline disturb caused Vt shift. In addition, the large bitline voltage in reverse read may also enhance I_{est} due to hot electron effects. The I_{est} thus imposes a limitation on read voltage in two-bit operation.

Program-State Charge Retention Loss

One of the advantages of trapping storage cells, as compared to floating gate flash cells, is the better charge retentivity. Fig.10 shows the program-state retention characteristics in our MXVAND cell. The cycle number and

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temperature dependence suggests that the nitride charge escape is through thermionic-field emission and subsequently oxide trap assisted tunneling (Fig.11). To study the field effect on nitride charge detrapping, we measure the V_t evolution with time at different gate biases (Fig.12). It was found that the V_t loss is proportional to the square root of an electric field (Fig. 13). In Fig. 13, V_o is the built-in potential in program state. From a 2D device simulation, V_o is around 2V. The square-root dependence of the charge loss on electric field can be well explained by the Frenkel–Poole model [9], i.e.

$$\tau_N = \tau_o \exp((\phi_N - q(qE/\pi\varepsilon)^{1/2})/kT) \qquad (2)$$

where τ_N is nitride charge detrapping time and ϕ_N is the corresponding nitride trap energy. Other variables have their usual definitions.

From Fig.13, it is apparent that V_g is an effective acceleration factor for lifetime measurement. If we assume that during the discharge time, t, all nitride traps with time constants less than t will be completely emptied and all other traps will be unaffected, the memory retention time will be equal to the nitride charge detrapping time. (We assume oxide trap assisted tunneling is sufficiently fast.)

In Fig.14, we plot the retention lifetime versus applied gate bias. The symbols represent measured result and the straight lines are from the Frenkel-Poole emission model. The measured slope in Fig.14 is about 2.75 decade/$V^{0.5}$, which is close to a theoretical value of 2.6 decade/$V^{0.5}$. The extrapolated memory retention time at V_g=0V is about 10^7 sec. for ΔV_t=1.5V and is above 10 years for ΔV_t=2.0V. The temperature acceleration for the retention loss is also investigated. Fig. 15(a) shows the charge loss versus time at T=25C, 85C and 150C, respectively. The retention loss at 150C shows saturation behavior. Further study by using a charge pumping technique reveals that the saturation is possibly caused by trap annealing. Fig. 15(b) shows the measured charge pumping current for different bake times.

Finally, we compare the data retention capability of the MXVAND cell and a SONOS cell [10] in Fig. 16. Better retentivity is achieved in the MXVAND due to a thicker bottom oxide and localized charge trapping.

Conclusion

The oxide-nitride-oxide trapping storage cell with hot electron programming and hot hole erasing is a promising candidate for the flash memory technology. The data retention issues of this cell are studied and reported for the first time. Frenkel-Poole emission rather than nitride charge direct tunneling is identified to be a dominant charge loss mechanism in program-state while positive trapped charge creation in the bottom oxide is the cause of the reliability issues in erase-state.

Acknowledgements

The authors would like to acknowledge Tom Yiu, Simon Wang, Fuja Shone and Ho-Chun Liou of MXIC for encouragement and support. The authors also would like to thank Reliability Engineering and Product Engineering of MXIC for many useful discussions.

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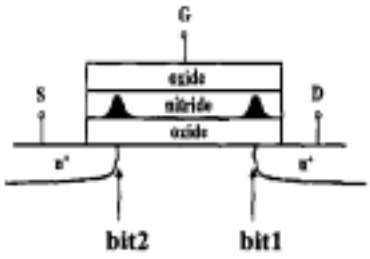


Fig.1 Schematic representation of a MXVAND cell with two-bit storage. The shaded area in the nitride layer represents stored charges.

Table.1 Suggested bias conditions for MXVAND cell operation.

		Program	Erase	Read
Bit 1	Vg	11V	-3V	2.5V
	Vd	5V	8V	0V
	Vs	0V	0V	>1.5V
Bit 2	Vg	11V	-3V	2.5V
	Vd	0V	0V	>1.5V
	Vs	5V	8V	0V

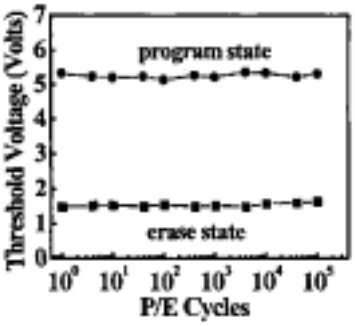


Fig.2 Endurance of a MXVAND flash cell operation window. The thickness of each ONO layer is 9nm, 6nm and 7nm. L_g=0.5μm.

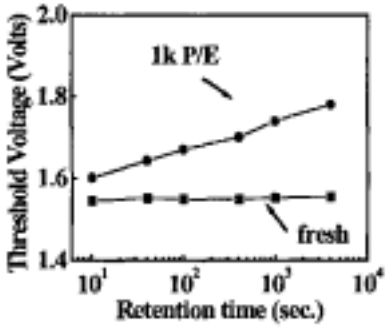


Fig.3 Erase-state threshold voltage drift versus retention time in fresh and 1k P/E cycled devices.

Table.2 Measured Vt and GIDL in a fresh device and a cycled device.

	Fresh	1K P/E	Net charge
V_t	1.2V	1.4V	negative
GIDL	27.9pA	23.5pA	positive

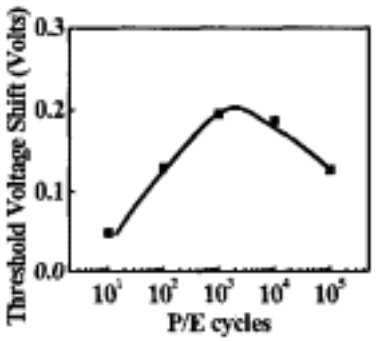


Fig.4 P/E cycle dependence of erase-state Vt drift after 10^4 sec. storage.

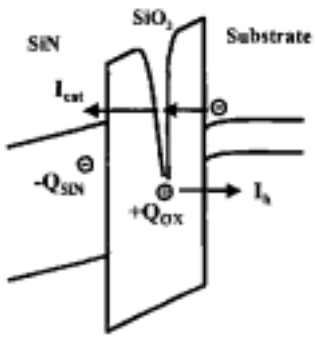


Fig.5 Schematic band diagram illustrating positive oxide charge detrapping current (I_h) and +Qox assisted electron tunneling current from substrate to the SiN conduction band (I_{cat}).

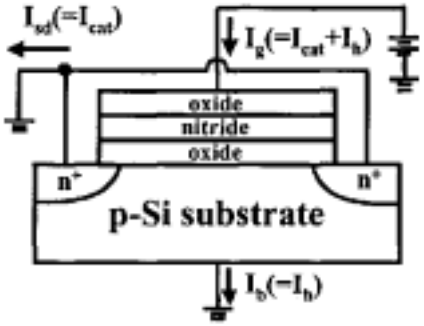


Fig.6 Illustration of a charge separation technique. I_{sd} is an electron current and I_b is a hole current.

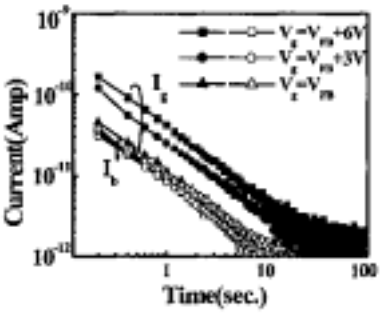


Fig.7 Measured I_g and I_b transients in erase state. The device has a large gate area ($2.5x10^5$μm^2). V_g is equal to V_{FB}, V_{FB}+3V, V_{FB}+6V respectively.

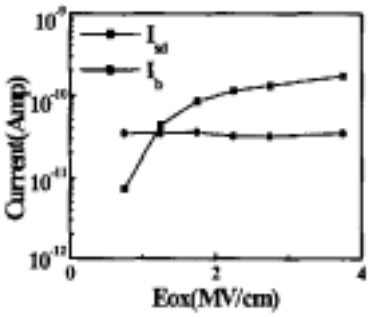


Fig.8 Field dependence of positive oxide charge detrapping current (I_h) and electron tunneling current (I_{sd}) at t=0.2 sec.. The gate area is $2.5x10^5$ μm^2.

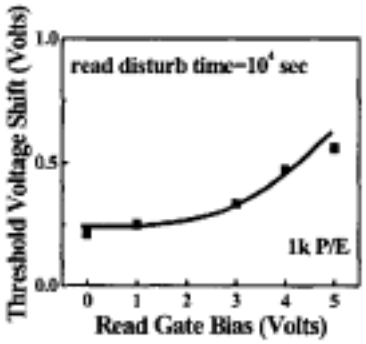


Fig.9 Wordline distuib caused threshold voltage shift.

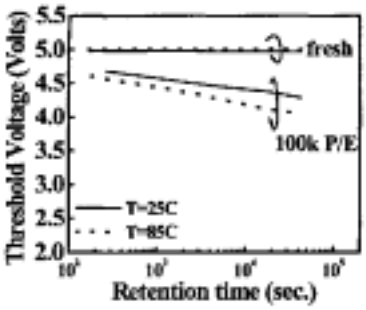


Fig.10 Program-state charge loss in fresh and 100k P/E cycled cells. T=25℃ and 85℃.

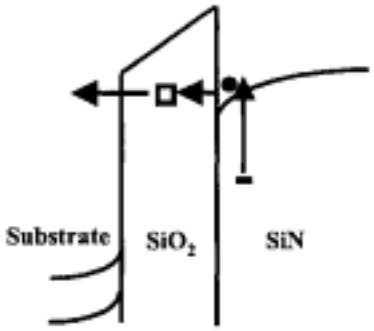


Fig.11 Illustration of nitride trapped charge escape by Frenkel -Poole emission and subsequently oxide trap assisted tunneling.

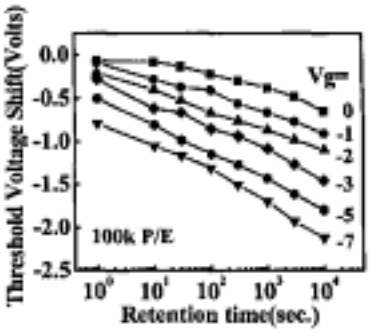


Fig.12 Program-state charge loss at different applied gate bias. T=25℃.

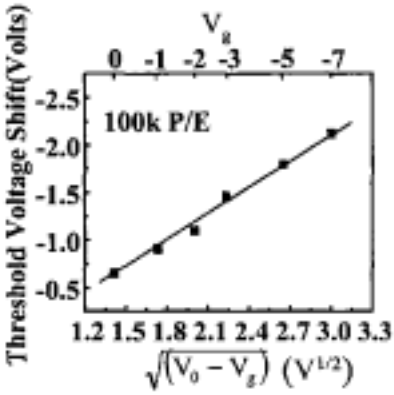


Fig.13 Program-state retention loss plotted against applied gate bias (top x-axis). Retention time is $1x10^4$ sec.. In this figure, V_0 is the built-in potential and the bottom x-axis corresponds to the square root of electric field. In the measured device, program-state V_t is 5.0V and V_0 is about 2V from a 2D device simulation.

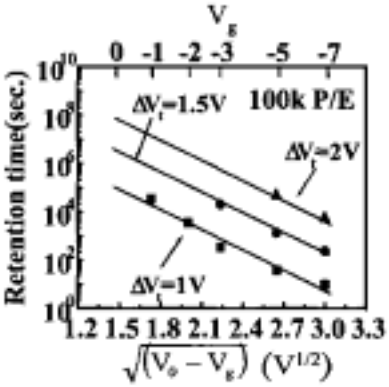
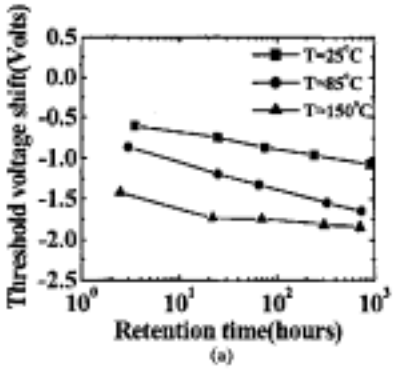


Fig.14 The charge storage lifetime versus applied gate bias. Retention lifetime is defined as ΔV_t=1V, 1.5V and 2.0V, respectively. V_g is defined in Fig. 13.



(a)

	fresh cell	1k P/E	5hr bake	20hr bake	60hr bake
I_{cp}(pA)	63	425	240	195	173

(b)

Fig.15 (a) Program-state retention loss versus time at different temperatures. (b) Charge pumping current in fresh and 1k P/E cycled cells. The bake temperature is 150 ℃.

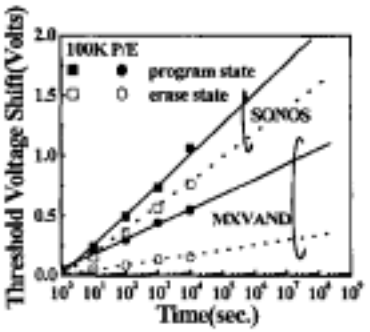


Fig.16 Comparison of data retention behavior between SONOS and MXVAND in program state and erase state.

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Cause of Data Retention Loss in a Nitride-Based Localized Trapping Storage Flash Memory Cell

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ABSTRACT

Data retention loss in a localized trapping storage flash memory cell with a SONOS type structure is investigated. Both charge loss through the bottom oxide and lateral migration of trapped charges in the nitride layer are considered for the data retention loss. Charge pumping and charge separation methods are used in this study. Our results reveal that in normal operation condition the retention loss is mainly caused by charge leakage via P/E stress created oxide traps.

INTRODUCTION

Interest in nitride-based trapping storage flash memory cells has revived recently for smaller cell size, simpler fabrication process, no drain induced turn-on and better cycling endurance [1-3]. Among these cells, attention is particularly paid to two-bit storage flash memory technology (NROM [3] and MXVAND [4]). Its cell structure is depicted in Fig.1 and its operation conditions are summarized in Table.1. Channel hot electron injection and band-to-band hot hole injection are used for programming and erasing, respectively. This storage method enables two bits per cell operation and exhibits better data retentivity than a conventional SONOS cell with uniform charge storage. Though the cell demonstrates excellent intrinsic charge retentivity [5], data retention loss is still a reliability concern after P/E cycling. Fig.2 shows the typical Vt retention characteristics in a fresh and a P/E cycled cell. After P/E cycling, the program state Vt drops with time and the erase state Vt has a positive shift. Data retention loss mechanisms in these localized storage cells are still controversial. Various theories have been proposed to explain the data retention loss. Lateral migration of trapped charges [6, 7] and oxide trap-assisted charge escape through the bottom oxide [4] have been proposed to explain the program state charge loss. Tunnel detrapping of positive oxide charges created during P/E cycling has been considered to be the cause of erase state Vt drift [4]. The purposes of this work are to clarify these issues and to provide more experimental evidence. In addition, a new reliability concern, negative Vt drift in a strongly erased cell, is reported and its mechanism is explained.

DEVICE CHARACTERIZATION

The samples used in this work are made of a n-channel MOSFET with an oxide-nitride-oxide (ONO) gate dielectric structure (Fig.1). The thickness of each ONO layer is 9nm (top oxide), 6nm and 7nm. Unlike a conventional SONOS cell, the bottom oxide is sufficiently thick to avoid charge direct tunneling.

Two methods are utilized to study the lateral spread of injected carriers. Assuming that electrons are trapped in the nitride layer above the channel near the n^+ drain junction, a Vt versus Vd measurement is used to investigate the lateral extent of the trapped electrons. Here, Vt is defined as the applied gate voltage at which the drain current is 1μA. These trapped electrons will raise the potential

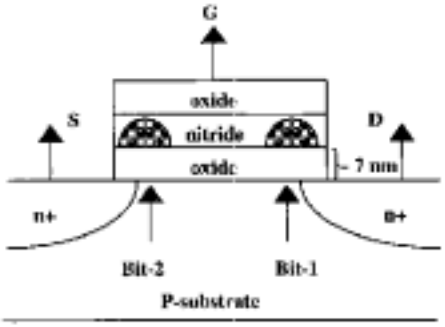

Fig.1 Schematic representation of the cell structure and localized charge storage.

Table 1. Operation conditions of MXVAND cells [4].

		Program (CHE)	Erase (BTBT HH)	Read (reverse)
Bit-1	Vg	11V	-3V	2.5V
	Vd	5V	8V	0V
	Vs	0V	0V	>1.5V
Bit-2	Vg	11V	-3V	2.5V
	Vd	0V	0V	>1.5V
	Vs	5V	8V	0V

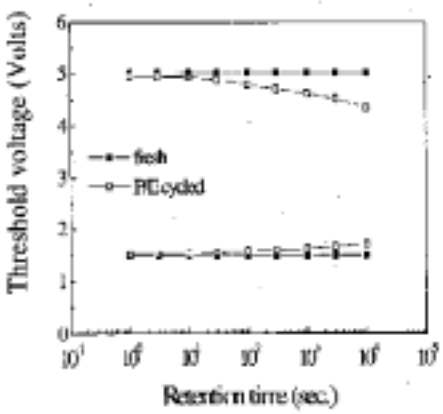

Fig.2 The typical Vt retention characteristics in a fresh and a P/E cycled cell. The storage temperature is 25C.

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barrier near the drain side. An increased Vt, which is proportional to the trapped electron density, will be measured at a low drain bias (e.g. Vd=0.1V). As a sufficiently high drain bias (e.g. Vd=1.5V) is applied, however, the drain depletion region will extend toward the channel. The trapped electrons will have little effect on the measured I-V characteristics when they are located within the depletion region at the drain [8]. The trapped electron density and its lateral extent can be estimated by this measurement.

A charge pumping method [9], which is able to probe the lateral distribution of trapped charges, is also used. A trapezoidal pulse train with a fixed high level (Vgh) and successively decreasing low levels (Vgl) is applied to the gate of the device. The substrate and the drain are grounded and the source is floating. The charge pumping current Icp (=Id=Ib) versus Vgl is measured. The fixed Vgh is sufficiently high to ensure that the entire channel is inverted. By varying Vgl, only the part of channel that undergoes inversion-accumulation-inversion over a pulse cycle contributes to Icp. Since the trapped electrons (near the drain side) cause an increase of the local flatband voltage, an Icp shift along the Vgl axis will be observed in a programmed cell. Based on the measured Icp versus Vgl curves of an un-programmed and a programmed cell, the trapped electron density can be extracted [9]. The trapped hole density can be profiled in a similar manner by a pulse train with a fixed base level and successively increasing high levels applied to the gate. The lateral migration of trapped charges in both the program and the erase state can be characterized by this technique.

With respect to charge loss through the bottom oxide, an ONO capacitor (2.5×10^5 μm^2) with uniform stress and charge storage is used. Thus, the effect of lateral charge migration can be excluded in this device. The evolution of the flatband voltage in the ONO capacitor with time is monitored to study the charge retention behavior. Furthermore, a charge separation technique is employed to explore the role of hole traps (positive trapped charges) in the bottom oxide during the retention loss process of an erase state cell. As shown in Fig.3, the hole detrapping current can be collected from the substrate.

Results and Discussions

Program state charge loss via vertical leakage path

As we mentioned in the previous section, the Vt versus Vd characteristics give an indication of the trapped electron density and the lateral extent of the trapped electrons in a programmed cell. Fig.4 shows the Vt versus Vd characteristics of a 100K P/E cycled cell in the program state before and after 24 hours storage. The storage temperature is 85C. It can be seen that the Vt has dropped due to charge loss, however, the shape of Vt versus Vd curves is essentially unchanged and there is no crossover in the Vt versus Vd characteristics before and after 85C, 24 hours storage. This indicates that lateral migration of electrons has not occurred. We have also applied the charge pumping technique to probe the lateral electron extent (Fig.5). If the trapped electrons spread laterally during the storage period, an increased Icp will be observed due to the extended trapped electron area. As indicated in Fig.5, the leftward shift of the Icp implies a decrease of the trapped electron density, however, no clear evidence of lateral electron movement is shown in the charge pumping characteristics.

In order to correlate the Vt loss with charge escape through the bottom oxide, the temporal evolution of the flatband voltage in an ONO capacitor was measured (Fig.6). The ONO capacitor had undergone a negative gate stress (-100nA for 1000sec) and then was programmed to a high Vt state by +FN injection. Since the structure has uniform charge storage, charge loss through the bottom oxide should be the only cause for the flatband voltage shift. The gate bias

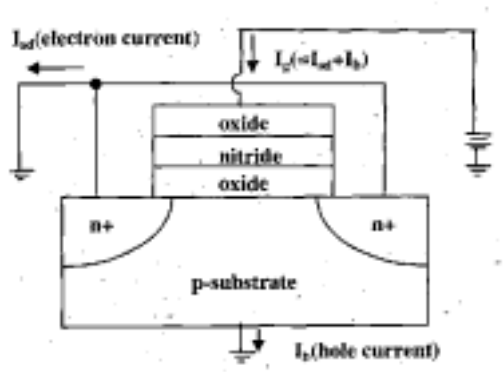

Fig.3 Illustration of a charge separation technique. Isd is an electron leakage current and Ib is a hole leakage current.

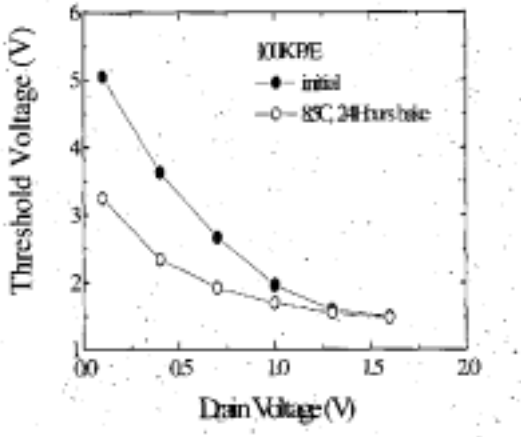

Fig.4 The measured Vt versus Vd characteristics of a 100K P/E cycled cell before and after 24 hours, 85C storage. The cell is in program state.

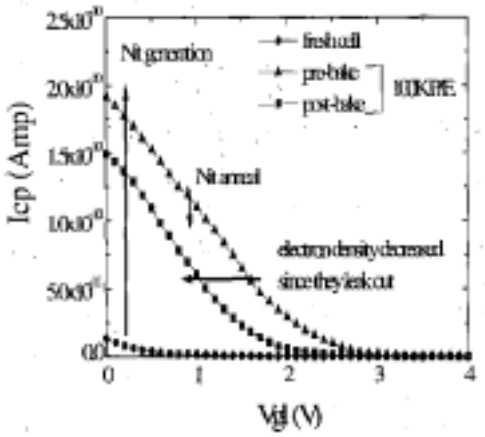

Fig.5 The measured charge pumping current (Icp) versus the low level of gate pulse (Vgl) in the CP measurement. The 100K cycled cell is in program state. The bake time is 24 hours and the bake temperature is 85C.

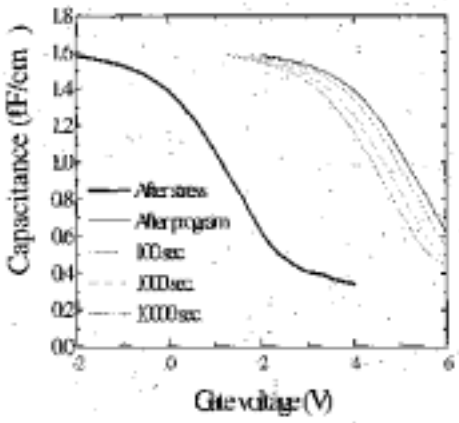

Fig.6 The CV temporal evolution of an ONO capacitor.

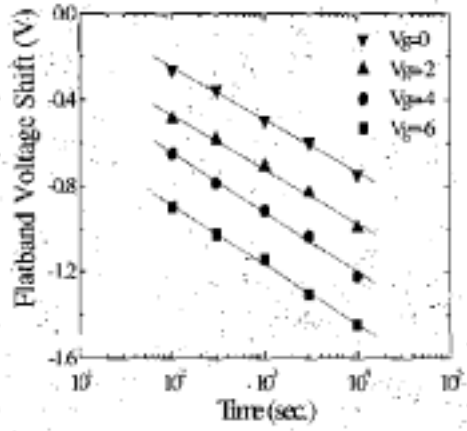

Fig.7 Evolution of the flatband voltage shift with the retention time in an ONO capacitor. The gate biases in measurement are 0, -2V, -4V, and -6V.

in the measurement is from Vg=0V to Vg=-6V. The measured results are shown in Fig.7. The flatband voltage shift exhibits vertical field dependence. Fig.8 shows that the Vt loss is proportional to the square root of the applied voltage, which is proportional to the nitride electric field. The square-root field dependence and the observed temperature dependence [4] imply that nitride charge escape is through the Frenkel-Poole emission [10]. Meanwhile, the dramatically increased Vt loss in a P/E cycled cell and in a negative gate stressed ONO capacitor, compared to fresh ones, suggests that oxide trap-assisted tunneling also participates in the charge loss process. In other words, trapped electrons leak out of the ONO stack via Frenkel-Poole emission and subsequent oxide trap-assisted tunneling. However, the oxide trap-assisted tunneling is a relatively fast process. The square-root field dependence is then determined by the Frenkel-Poole emission.

We have also plotted the retention lifetime versus the square root of the applied voltage, which is proportional to the nitride electric field, as shown in Fig.9. The slope of this curve is 2.49 dec/$V^{0.5}$ which is consistent with the theoretical value (2.6 dec/$V^{0.5}$). This

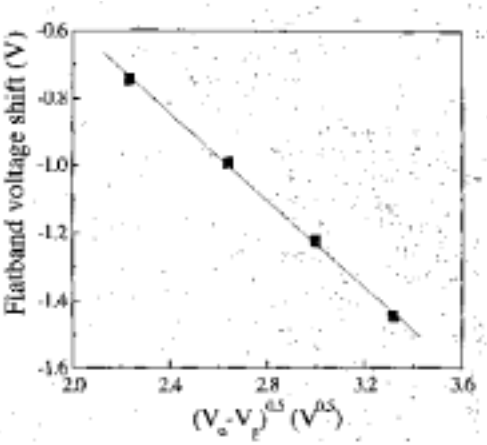

Fig.8 The measured flatband voltage shift versus the square root of the nitride electric field which is proportional to (V_0-V_g). V_0 represents the internal built-in field and is due to the flatband voltage and the trapped charges. It is 5V in our example. The storage time is 10000 sec.

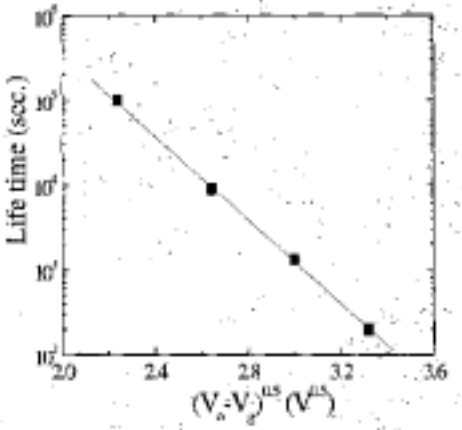

Fig.9 The retention lifetime versus the nitride electric field. V_g is the same as that in Fig.8. The lifetime is defined as the storage time sustained for a 1V shift of the flatband voltage.

field dependence is the same as that we observe in a memory cell [4]. It implies that the vertical charge loss occurs in an ONO capacitor with uniform charge storage and also in a memory cell with localized charge storage.

Positively trapped oxide charges in an erase state cell

In the erase state, a positive Vt drift is observed after P/E stress (Fig.2). Since the Vt drift does not show temperature dependence (Fig.10), we believe that lateral migration of trapped charges in the nitride layer is unlikely. The charge pumping result of an erase state cell also supports this argument (Fig.11). As shown in Fig.11, we do not observe any obvious distortion of the Icp characteristic after an 85C, 4 hours bake except for a little interface state annealing effect.

The positive Vt drift implies a net increase of negative charges. Since the nitride charge direct back tunneling is prevented by the 7nm bottom oxide, and the insignificant temperature dependence of the Vt drift excludes the charges transport in nitride, funnel

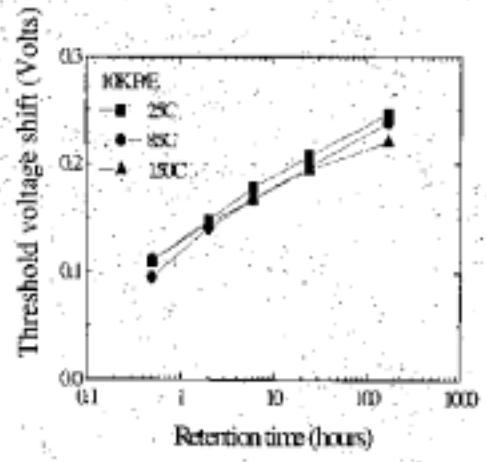

Fig.10 The Vt shift versus the retention time of a 10K P/E cycled cell in erase state. The bake temperatures are 25C, 85C and 150C.

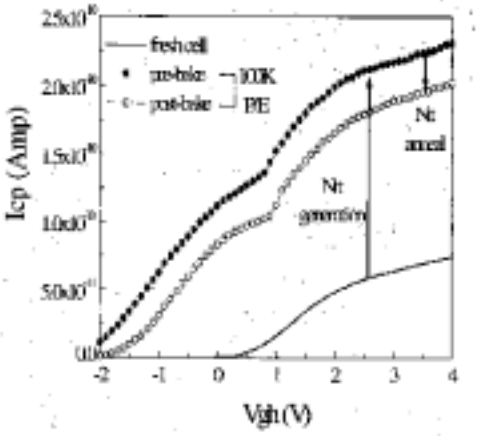

Fig.11 The measured Icp versus Vgh of a 100K P/E cycled cell in erase state. The bake time is 4 hours and the bake temperature is 85C.

detrapping of positive oxide charges created during P/E cycling is suspected to be the cause. The results obtained by the charge separation method confirm the existence of a transient hole leakage current (Ib) in an erased cell (Fig.12). The I/t transient characteristic of Ib can be well explained by the tunnel front model [11]. This finding provides additional evidence that the erase state Vt drift is related to positive oxide charge tunnel detrapping.

Lateral migration of trapped holes in strongly erased cell

We would like to investigate the lateral hole transport in a fresh cell with an extremely strong erase condition. The erase (hot hole injection) time is 100 seconds (10 ms × 10K erase-only cycles). This strongly erased cell shows a negative Vt shift (Fig.13). As opposed to the positive Vt shift after P/E stress (Fig.10), this negative Vt shift shows strong temperature dependence.

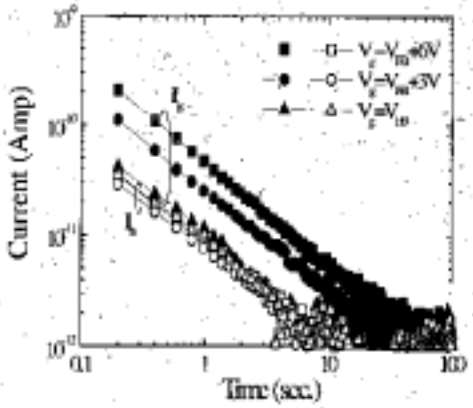

Fig.12 The measured Ig and Ib transients in erase state. The cell has a large gate area (2.5×10^5 μm^2).

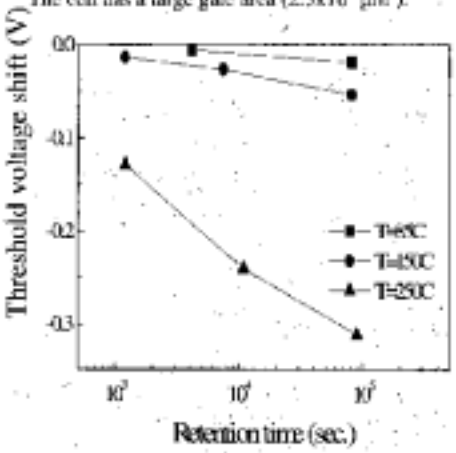

Fig.13 The evolution of Vt with the storage time in a strongly erased cell. The bake temperatures are 85C, 150C, and 250C. A negative Vt shift is observed.

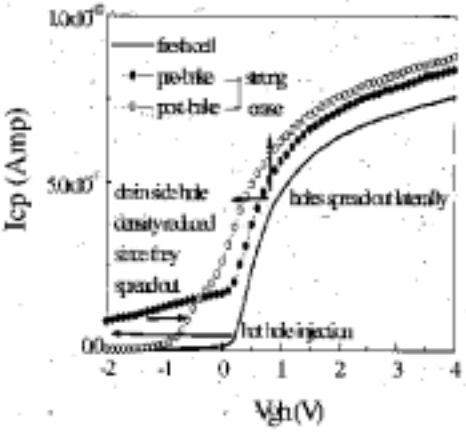

Fig.14 The measured Icp versus Vgh in a strong hot hole erase condition. The BTBT hot hole erase time is 100 sec. The bake time is 3 hours and the bake temperature is 250C. The evidences of considerable hole pile-up and lateral hole movement are indicated in the figure.

Fig.14 shows the charge pumping characteristics. As indicated in this figure, a considerable amount of holes is trapped in the nitride layer above the channel close to the drain junction after strong erase. It causes a leftward shift of the low Vgh portion (for Vgh<0V) of the Icp characteristic [9]. The cell is then baked at 250C for 3 hours. A crossover of the Icp characteristics before and after bake is observed. We can see that the low Vgh portion (for Vgh<-1V) of the Icp curve shifts rightward. This indicates that the trapped hole density near the drain side decreases. In addition, Icp increases for Vgh>0V. This increased Icp is conflict with interface annealing effect, if any. We believe that the leftward shift of Icp (for Vgh>0V) is caused by the lateral spread of the trapped holes. It results in channel shortening and serious short channel effect. This causes the observed negative Vt shift. Meanwhile, the lateral spread of holes also explains the strong temperature dependence of this negative Vt shift. Finally, we want to point out that this negative Vt shift will result in an increased leakage current in the memory array. This will be a potential reliability concern.

CONCLUSIONS

The effects of lateral charge migration and charge loss through the bottom oxide in a localized trapping storage cell have been assessed. In a P/E cycled cell, charge leakage through the bottom oxide is found to be the dominant data loss mechanism in the program state. Positive oxide charge tunnel detrapping is responsible for the positive Vt drift in the erase state after P/E cycling. In the extreme conditions of considerable hole pile-up and high temperature storage (250C), lateral hole transport in the nitride is observed and it results in an increased leakage current in the memory array.

ACKNOWLEDGEMENTS

The authors would like to acknowledge Tom Yiu, Simon Wang, Fuja Shone and Ho-Chun Liou of MXIC for encouragement and support. The authors would also like to thank Reliability Engineering and Product Engineering of MXIC for many useful discussions.

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