行政院國家科學委員會專題研究計畫　成果報告

晶圓製造廠爐管區控檔片之多迴圈網路模式

計畫主持人： 彭文理
共同主持人： 鍾淑馨
計畫參與人員： 李欣怡、康鶴耀

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※　　　　晶圓製造廠爐管區控擋片之多迴圈網路模式

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※　　　A Multi-loop Network Model for Control/Dummy Wafers in

the　※

※　　　　　　Furnace Area of Wafer Fabrication

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計畫主持人：　彭文理

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共同主持人： 鍾淑馨

計畫參與人員： 李欣怡、康鶴耀

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行政院國家科學委員會專題研究計畫成果報告

主持人：彭文理　　　　　　國立交通大學工業工程與

管理系

共同主持人：鍾淑馨　　　　　　國立交通大學工業工程與

管理系

計畫參與人員：李欣怡、康鶴耀　國立交通大學工業工程與

管理系

中文摘要：本計劃主要考慮晶圓廠爐管區之控片擋的降級交互作用特性，首先分析爐管區控擋片之降級特性與重複使用情況，並以多迴圈網路模式，解決控擋片水準的問題。對於多迴圈網路模式，我們是在考慮等級調降的情況下，以拉式生產系統之存貨概念，決定各等級間迴圈內之控擋片水準與重複使用之比例。經由實例驗證，得知本模式所設定之等級控擋片水準與等級重複之比例，能滿足生產系統控擋片消耗之需求。因此在不影響系統產出條件下，本計劃所構建之控擋片多迴圈網路管理模式，確實能提供最低之控檔片水準。

關鍵詞：爐管區、控檔片、存貨、多迴圈、再回流

Abstract: In this research project, we establish a multi-loop network model for control/dummy (C/D) wafers in wafer fabrication furnace area by considering the re-entrant of control wafers within the same grade and the downgrading of control wafers among different grades. Under pulling control production environment, a multi-loop algorithm is developed for estimating the WIP control wafers for each grade. We conduct some simulation experiments based on a real-world factory production environment to demonstrate the effectiveness of the proposed algorithm. The results show that the algorithm is an efficient tool for estimating the cycle time and WIP level for each grade of control wafers.

Keywords: Furnace area, control/dummy wafers, inventory, multi-loop, re-entrant.

1. Introduction

The purpose of using C/D wafers is to assure that manufacturing process in a wafer fab can satisfy the required specifications. C/D wafers are repeatedly used until their immaculacy and thickness no longer conform to the process requirement. For C/D wafers that do not conform to the process requirements, they are either downgraded or discarded.   To avoid pollution to factory machines due to the misuse of C/D wafers, managers often apply grade concepts of C/D wafers for diverse machine types according to the requests of processing circumstances, such as immaculacy degree. Any shortage of C/D wafers may result in a halt of machine operations and as a consequence, may seriously affect the process yield and production planning. To avoid such situations occur, a large number of C/D wafers are usually prepared and stored for use. This, however, unnecessarily increases the WIP level of

C/D wafers.   For most factories, the WIP level of C/D wafers is 30%-50% of that for normal products, with 30% being the benchmark as indicated by Lin (2000).

Existing methods for estimating cycle time include the simulation approach, statistical regression approach, analytical method, and the hybrid method. The pros and cons of those existing methods have been examined by several researchers (Lawrance (1995), Glynn (1997), Raddon & Grigsby (1997)).   Discrete event simulations are used to create shop floor condition, which is a useful tool for performance prediction. The use of statistical regression approach with variance analysis explores the relationship between the cycle time and the system variables to construct a cycle time forecasting model.   Wang *et al.* (1997) combined Little's formula (Hiller (1995)) with Kingman's equation (Kleinrock (1975)) to develop a regression function for estimating the cycle time at each workstation. Analytical method uses the queuing systems theory as a base to develop formulas for flow time estimation according to the distribution hypothesis on parameter setting. The hybrid method combines various methods to provide the cycle time estimation. Chung *et al.* (1999) studied analytical methods incorporating simulation techniques to develop a cycle time estimation method.

Although those studies have provided some important information regarding the cycle time and WIP level estimation, there has been little research done on C/D wafers inventory management.   The purpose of this paper is to present an algorithm for estimating the C/D wafers cycle time and the WIP level for each C/D wafer grade. Under the production C/D environment with pulling system, a multi-loop C/D wafers (MCW) algorithm is developed, which considers the re-entrant and downgrade manufacturing factors to set the WIP level of C/D wafers for each grade.   This investigation provides a useful reference to the management level for setting the WIP level for each grade and to increase inventory management performance.

2. Problem Description and Assumptions

In general, the re-use status of C/D wafers can be divided into (1) pre-disposition, (2) in-use, and (3) recycle (see Chen and Lee (2000)), termed the PUR process. The in-use C/D wafers in the furnace area provide functions for product monitoring, equipment monitoring, breakdown and recovery monitoring, and preventive maintenance (Lin (2000)).   In this paper, multi-loop system concept is applied to the establishment of the downgrade and PUR process.

A diagram of multi-loop C/D wafers system is depicted in Figure 1.   In Figure 1, node *Start* contains new C/D wafers, node *Finish* is the discard wafers collection, and a_{01} is the new wafers depletion rate to loop I.   Each loop can be considered as a neuron, and the jth loop can be considered as the jth grade of C/D wafers process.   The depletion rate of jth grade C/D wafers is d_j, re-entrant ratio is P_{ij} (for $i=j$) , downgrade ratio is P_{ij} (for $i<j$) , discard ratio is P_{ij} (for $j=D$) , and arrival rate is λ_j.
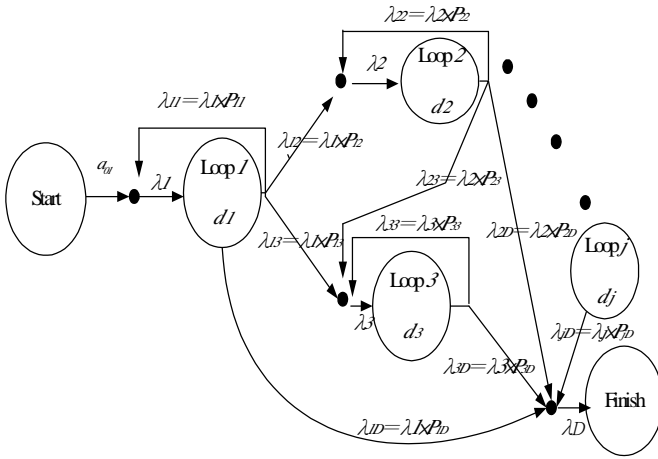
Figure 1. The multi-loop C/D wafers system

3. C/D Wafers Inventory Management System

This paper develops MCW algorithm to estimate the most appropriate WIP level of C/D wafers for each grade. The proposed algorithm can be divided into two phases: (1) calculating new C/D wafers arrival rate, downgrade ratio and re-entrant ratio, and (2) estimating C/D wafers cycle time and WIP level for each grade.

The multi-loop system presented here can supply new C/D wafers in the 1st loop and downgrade C/D wafers to the jth loop ($1 < j$). When supply and demand are in balance, we can calculate the new C/D wafers supply rate, the re-entrant C/D wafers arrival rate and the downgrade C/D wafers arrival rate. The cycle time for each grade of C/D wafers is calculated by adding up the downgrade waiting time, the re-entrant waiting time and the PUR process time for each grade of C/D wafers. The WIP level for each grade of C/D wafers is obtained by multiplying the arrival rate（consisting of new C/D wafers arrival and downgrade arrival） and cycle time of C/D wafers.

3.1.Calculation of Downgrade and Re-entrant Ratios

The multi-loop system must supply enough C/D wafers for use in time, and shortage is not allowed. The operative constraints are as follows. By Equation (1), the demand rate of C/D wafers is equal to the supply rate of C/D wafers for each loop. In the first loop, the supply rate of C/D wafers is equal to the new arrival rate of C/D wafers and the re-entrant rate, and this relationship is shown in Equation (2). For other loops, the supply rate of C/D wafers equals to the C/D wafers re-entrant rate and downgrade rates from up-stream loops, as shown in Equation (3). The constraints are as follows:

$$d_j = \lambda_j \qquad\qquad j = 1, 2, \dots c. \qquad (1)$$

$$\lambda_j = a_{01} + \lambda_1 p_{11} \qquad\qquad j = 1 \qquad\qquad (2)$$

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$$\lambda_j = \sum_{i=1}^{j} \lambda_i P_{ij} \qquad\qquad j = 2, \ldots c. \qquad\qquad (3)$$

where d_j is the demand rate of C/D wafers per day, λ_j is the supply（arrival）rate of C/D wafers per day, a_{01} is the supply rate of new C/D wafers per day, P_{ij}（$i=j$）is the re-entrant ratio and P_{ij}（$i<j$）is the downgrading ratio.

3.2. Estimation of Cycle Time and WIP Level

The cycle time of C/D wafers is defined to be the time interval from C/D wafers entering the jth loop system to leaving the jth loop system. Cycle time consists of downgrading waiting time, re-entrant waiting time and process time. They are defined as follows:

(1) The downgrading waiting time: DWT_j. The downgrading waiting time is the time interval between downgrade arriving of C/D wafers and the pre-disposition of PUR process in loop j.

$$DWT_j = \begin{cases} 0 & j=1 \\ \dfrac{1}{\lambda_j \times (1-P_{jj})} - \dfrac{1}{\lambda_j} & j=2,\ldots c. \end{cases} \qquad (4)$$

where $\lambda_j \times (1-P_{jj})$ is equal to the sum of downgrading arrival rate $\left(\sum_i^j \lambda_{ij} \right)$.

(2) The re-entrant waiting time: RWT_j. The re-entrant waiting time is caused from C/D wafers re-entrant arriving to in-use in the PUR process in loop j. The difference between re-entrant arrival time and in-use time is multiplied by the number of repeat times to estimate the re-entrant waiting time.

$$RWT_j = \left(\frac{k}{\lambda_j} - \frac{1}{\lambda_{j1}} - \frac{1}{\lambda_{j2}} - \frac{1}{\lambda_{j3}} \right) \times \frac{P_{jj}}{1-P_{jj}} \qquad j=1,2,\ldots c. \qquad (5)$$

where

$$0 \leq \frac{1}{\lambda_{j1}} + \frac{1}{\lambda_{j2}} + \frac{1}{\lambda_{j3}} \leq \frac{1}{\lambda_j} \qquad k=1$$

$$\frac{1}{\lambda_j} \leq \frac{1}{\lambda_{j1}} + \frac{1}{\lambda_{j2}} + \frac{1}{\lambda_{j3}} \leq \frac{2}{\lambda_j} \qquad k=2$$

$$\cdot$$
$$\cdot$$
$$\cdot$$

$$\frac{n-1}{\lambda_j} \leq \frac{1}{\lambda_{j1}} + \frac{1}{\lambda_{j2}} + \frac{1}{\lambda_{j3}} \leq \frac{n}{\lambda_j} \qquad k=n.$$

(3) Theoretical process time: PUR_j. The theoretical process time includes the PUR process time, loading and unloading time of C/D wafers in loop j. Process time is obtained by multiplying

process service time by the number of repeat times.

$$PUR_j = \frac{1}{\sim_{j1}} \times \frac{1}{1-p_{jj}} + \frac{1}{\sim_{j2}} \times \frac{1}{1-p_{jj}} + \frac{1}{\sim_{j3}} \times \frac{p_{jj}}{1-p_{jj}} \quad j=1,2,..c. \quad (6)$$

Cycle time for each loop j, CT_j, equals the sum of DWT_j, RWT_j and PUR_j

($CT_j = DWT_j + RWT_j + PUR_j$) and is calculated by Equation (11).

$$CT_j = \begin{cases} \frac{1}{\sim_{j1}} \times \frac{1}{1-p_{jj}} + \frac{1}{\sim_{j2}} \times \frac{1}{1-p_{jj}} + \frac{1}{\sim_{j3}} \times \frac{p_{jj}}{1-p_{jj}} + \left(\frac{k}{\lambda_j} - \frac{1}{\sim_{j1}} - \frac{1}{\sim_{j2}} - \frac{1}{\sim_{j3}} \right) \times \frac{P_{jj}}{1-p_{jj}} & j=1 \\ \frac{1}{\sim_{j1}} \times \frac{1}{1-p_{jj}} + \frac{1}{\sim_{j2}} \times \frac{1}{1-p_{jj}} + \frac{1}{\sim_{j3}} \times \frac{p_{jj}}{1-p_{jj}} + \left(\frac{k}{\lambda_j} - \frac{1}{\sim_{j1}} - \frac{1}{\sim_{j2}} - \frac{1}{\sim_{j3}} \right) \times \frac{P_{jj}}{1-p_{jj}} \\ + \left(\frac{1}{\lambda_j \times (1-P_{jj})} - \frac{1}{\lambda_j} \right) & j=2..c. \end{cases} \quad (7)$$

where $\sim_{jj}$ is the service rate of the jth loop, p_{jj} is re-entrant ratio of the jth loop, λ_j is the total

arrival rate of the jth loop, λ_{ij} is the arrival rate from the ith loop to the jth loop and

$\lambda_j \times (1-P_{jj})$ is the sum of downgrade arrival rate. The WIP level of a loop can be estimated by
Equation (8) and (9). The WIP level of loop j is:

$$WIP_j = \lambda_j \times (1-P_{jj}) \times CT_j, \quad j=1,2,...c \quad (8)$$

$$\lambda_j \times (1-P_{jj}) = \begin{cases} a_{01} & j=1 \\ \sum_2^j \lambda_{ij} & j=2,...c. \end{cases} \quad (9)$$

where WIP_j is the work-in-process in the jth loop and CT_j is the cycle time of the jth loop. The system
WIP level, WIP_s, of C/D wafers is as follows:

$$WIP_s = \sum_{j=1}^{c} WIP_j \quad (10)$$

4. Numerical Example and Simulation Results

In order to justify the applicability of the proposed MCW algorithm, we consider some cases to
investigate the effects of different demand rate on the system. We compare our estimated parameter
values with the results obtained from simulations by eM-Plant simulation programming software
(TECONMATIX TECHNOLOIES Ltd. (2000)). The simulation horizon is set to 110 days, in which
the first 10 days are warm up period. In order to eliminate simulation errors, 10 times of simulation
with different seeds are run, and the average value of simulation results is used as the comparison
object.

The results of MCW algorithm are compared with those of simulation.   As shown in Figure 2-13, the absolute percentage of discrepancy in cycle time estimation is between 0.008% and 4.324% among all cases in loop 1, between 0.005% and 1.227% in loop 2, and between 0.002% and 1.489% in loop 3. The absolute percentage of discrepancy in WIP level for MCW and simulation is between 0.048% and 0.867% among all cases for loop 1, between 0.040% and 4.810% in loop 2, and between 0 and 0.317% in loop 3. The system WIP level is the sum of WIP level for each loop, and the WIP level for a single loop can be obtained with the given demand rate and re-entrant ratio. The absolute percentage of discrepancy in system WIP level under MCW and simulation is less than 5%.   Based on the above analysis, we can see that the proposed MCW algorithm performs quite well in estimating cycle time and WIP level for each C/D wafers grade.
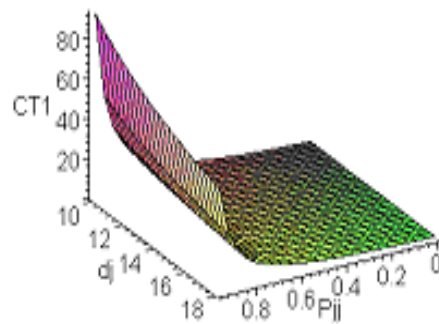
Figure 2. The cycle time of I^{st} loop under MCW with demand rate=10(1)18 and re-entrant ratio=0.0(0.1)0.9.
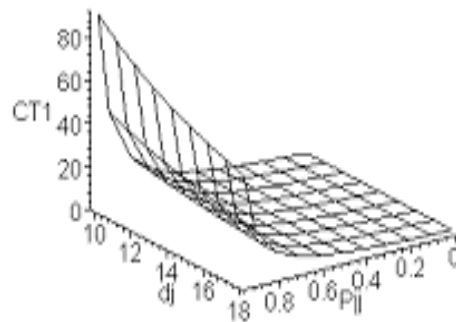
Figure 3. The cycle time of I^{st} loop under simulation with demand rate=10(1)18 and re-entrant ratio=0.0(0.1)0.9.
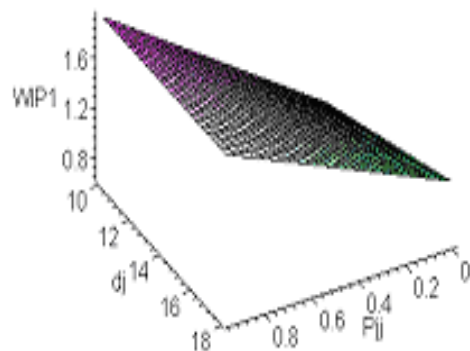
Figure 4. The WIP level of I^{st} loop under MCW with demand rate=10(1)18 and re-entrant ratio=0.0(0.1)0.9.
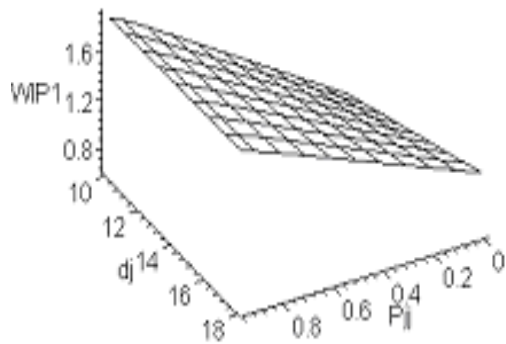

Figure 5. The WIP level of I^{st} loop under simulation with demand rate=10(1)18 and re-entrant ratio=0.0(0.1)0.9.
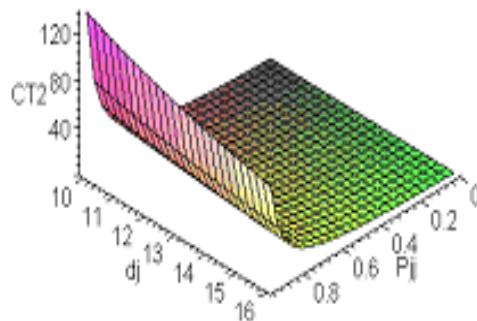

Figure 6. The cycle time of loop 2 under MCW with demand rate=10(1)16 and re-entrant ratio=0.0(0.1)0.9.
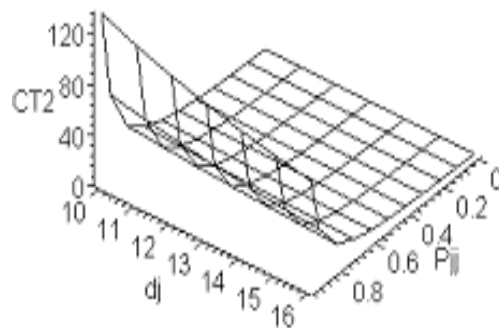

Figure 7. The cycle time of loop 2 under simulation with demand rate=10(1)16 and re-entrant ratio=0.0(0.1)0.9
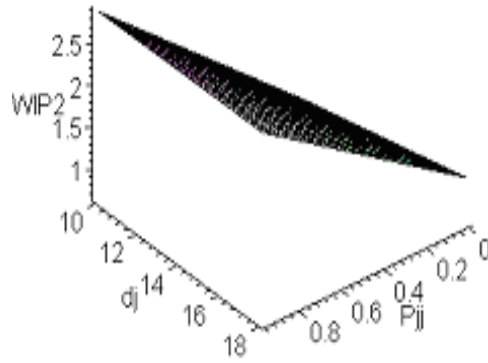
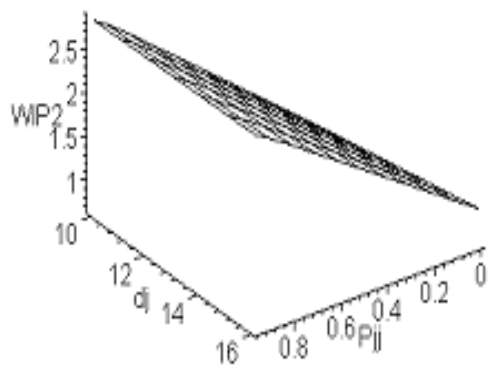Figure 8. The WIP level of loop 2 under MCW with demand rate=10(1)16 and re-entrant ratio=0.0(0.1)0.9.

Figure 9. The WIP level of loop 2 under simulation with demand rate=10(1)16 and re-entrant ratio=0.0(0.1)0.9.
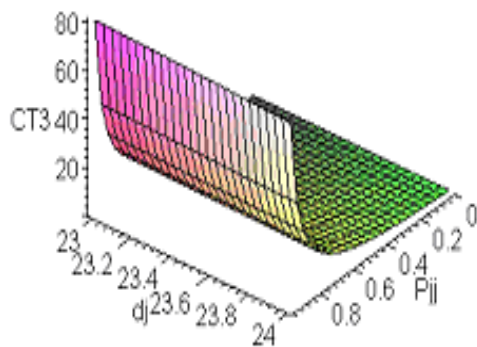

Figure 10. The cycle time of loop 3 under MCW with demand rate=23(1)24 and re-entrant ratio=0.0(0.1)0.9.
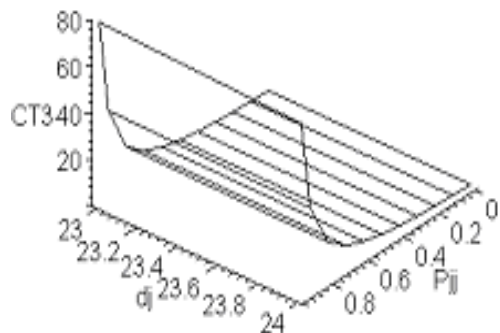

Figure 11. The cycle time of loop 3 under simulation with demand rate=23(1)24 and re-entrant
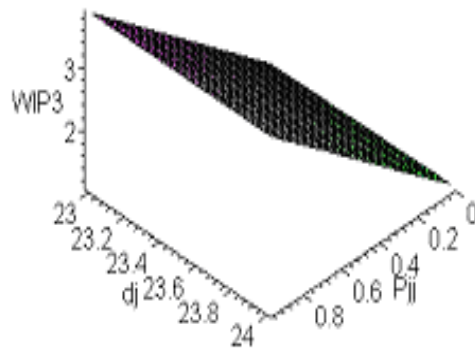
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ratio=0.0(0.1)0.9.

Figure 12. The WIP level of loop 3 under MCW with demand rate=10(1)16 and re-entrant ratio=0.0(0.1)0.9.
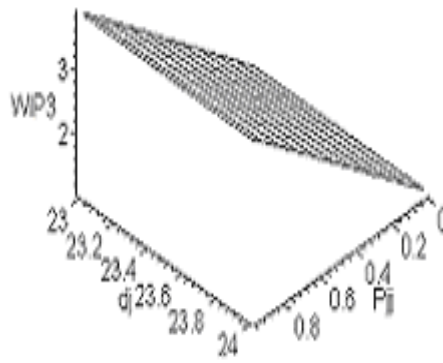

Figure 13. The WIP level of loop 3 under simulation with demand rate=23(1)24 and re-entrant ratio=0.0(0.1)0.9.

5. Conclusions

C/D wafers inventory management is a challenge to wafer fab, and estimating depletion rate correctly for each grade becomes an important task. Demand rate and WIP level of C/D wafers are closely related to many factors such as throughput target, product mix and priority mix. In this paper, the MCW algorithm is proposed to estimate the C/D wafers WIP level for each grade. By estimating processing time, downgrading waiting time, and re-entrant waiting time for each PUR process, cycle time and WIP level for each grade can be determined. From the results obtained in the example, the MCW algorithm performed quite promising on estimating the depletion rate and WIP level. The percentage of discrepancy in system WIP level between the MCW algorithm and simulation result is less than 5%. The results showed that the proposed methodology has rather good accuracy. Future research could focus on different depletion cost for each grade of C/D wafers, to find the minimum cost curve as well as to achieve manufacturer's planning target.

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