# 行政院國家科學委員會研究計畫成果報告

## 計畫題目：深次微米射頻元件

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### 中文摘要

為了達到高效能及極佳的高頻特性，在製作0.5、0.25以及0.18微米之高頻電晶體中，利用raised source/drain的方法來實現，並且，於接點處成長低阻值的矽化鈷，不僅減小閘極阻抗和產生最大功率增益，進而，避免其在最高工作頻率之不良影響，另則，使用多指的閘極結構來增大其電流值並同有降低閘極阻抗之功用，在完成對射頻元件之設計及製程後，即對三種不同尺寸的電晶體分別做了直流與高頻的電性量測，並針對所得的量測數據使用模擬工具進行分析與比較。

而數值分析之結果顯示，其高頻效能改善的幅度逐漸趨和緩而達到飽和，是隨著電晶尺寸的微縮化。再進一步，利用簡單但有效的高頻電晶體等效電路模型加以分析，發現造成這趨勢特性，主要之因素為其電晶體閘極與汲極間的寄生電容$C_{gd}$之影響以及高頻的非穩態效應（non-quasi static effect）所造成，因為這些效應並未隨著閘極長度的微縮化而減小，而影響了深次微米射頻元件之高頻特性。

關鍵詞: 高頻電晶體，電晶體微縮化，非穩態效應

### *Abstract*

For achieving the optimum characteristics of RF performance, taking the methods of raised source/drain to fabricate at the Deep sub-µm RF Devices of 0.5µm 0.25µm 0.18µm Furthermore, the growth of $CoSi_2$ can help producing the higher power gain by lower resistance and using the technique of the multiple gate fingers due to enhance the current . After the device process, the measured numeric of DC and RF is to be compared and analyzed with simulation.

Obviously, it is found the measured RF performance of 0.5, 0.25, and 0.18 µm MOSFETs gradually saturates as scaling down, which can be explained by the derived analytical equation and simulation. It is reasonable that the overlap $C_{gd}$ and non-quasi-static effect are the main factors but scales much slower than $L_g$.

**This paper has been submitted to IEEE MTT-S 2000.**

Keywords: RF MOSFET, scaling down, RF performance

### 一、簡介

Although Si RF MOSFETs has the advantages of rapid technology evolution and low production cost, it is still not clear where is the limitation of MOSFETs [1], and whether Si BJT [2] or even III-V technology should be used at higher frequencies. In this paper, we have analyzed the fabricated 0.5, 0.25, and 0.18 µm MOSFETs, and discuss performance limiting factors as scaling down using our derived analytical equation and numerical device simulation. We have found that the RF performance improvement gradually saturates as scaling down, which is observed by both experimental data and our analysis. The gate-drain overlap capacitance ($C_{gdo}$) is the key factor for $G_{max}$ and $f_{max}$; unfortunately, it is difficult to proportionally scale down as $L_g$ due to lateral diffusion of source-drain implants. The non-quasi-static (NQS) effect will also reduce the $H_{21}$, $f_t$, and maximum available gain (MAG). Our work can help to understand the performance limitation of MOSFET scaling and further choose of device operated at high frequencies.

### 二、實驗方法

Multiple fingered 0.5, 0.25, and 0.18 µm MOSFETs are fabricated on standard ~10 Ω-cm Si substrate with gate width of 200-250 µm and on-wafer probe layout. The multiple gate fingers with low resistivity $CoSi_2$ [3] can achieve a reasonable power level and reduce the extrinsic gate resistance that is important for $G_{max}$ and $f_{max}$. Then, S-parameters were measured up to 18 GHz using a CASCADE on-wafer probe, a network analyzer, and de-embedded from dummy devices. A matrix of different size of transistors and capacitors is used to extract device parameters for further analysis using modified BSIM3v3 MOSFETs model in SPICE..

## 三、結論與討論

The measured frequency response of $H_{21}$ and $G_{max}$ according to the equations (1) to (4) is plotted in Fig. 1 and summarized in Table 1.

$$f_t=\frac{g_m}{2\pi(C_{gs}+C_{gd})}\frac{1}{\sqrt{1-\left(g_m R_{nqs}\frac{C_{gd}}{C_{gs}+C_{gd}}\right)^2}}=\frac{v_{sat}}{2\pi(L_g+L_{ov})}\frac{1}{\sqrt{1-\left(g_m R_{nqs}\frac{L_{ov}}{L_s+L_{ov}}\right)^2}} \tag{1}$$

$$G_{max}=\left|\frac{S_{21}}{S_{12}}\left(K-\sqrt{K^2-1}\right)\right|=\left|\frac{jwC_{gd}-g_m[1+jwR_{nqs}(C_{gd}+C_{gs})]}{jwC_{gd}}\right|\left|\left(K-\sqrt{K^2-1}\right)\right| \tag{2}$$

$$f_{\max,MSG=1}=\frac{1}{2\pi}\frac{g_m}{C_{gd}}\frac{1}{\sqrt{2g_m R_g C-(g_m R_g C)^2}} \tag{3}$$

$$C=1+\frac{C_{gs}}{C_{gd}} \tag{4}$$

It is important to notice that the measured $H_{21}$, $f_t$, $G_{max}$, and $f_{max}$ gradually saturate as device scaling down. The saturation rate is faster for $G_{max}$ and a reducing $f_{max}$ is even observed.

Furthermore, the measured $H_{21}$ and $f_t$ are about 50% lower than the calculated value from conventional equation of $g_m/2\pi C_{gs}$ or $v_{sat}/2\pi(L_g-2L_{ov})$, where $L_{ov}$ is the gate-drain overlap length. We have therefore derived a more accurate $H_{21}$ and $f_t$ (at $H_{21}=1$) equations using modified BSIM3v3 equivalent circuit model and including the NQS effect.

Although the $R_{nqs}$ related term in $H_{21}$ is negligible at low frequency, it becomes more important as increasing frequency near $f_t$. Good matching between measured and simulated $f_t$ in Table 1 can only be obtained by considering the NQS effect. Because of the additional term, $f_t$ increases slower than 1/ $L_g$ scaling down.

Similar large difference of 300%-350% exists in the measured and calculated $f_{max}$ using the well-known equation of $(f_t/8\pi R_g C_{gd})^{1/2}$. This difference is because the above equation is derived from the unilateral gain with a constant gain roll-off while $G_{max}$ changes to 30-40dB/decade decrease in MAG

To further analyze the frequency response, we have also derived $G_{max}$ and $f_{max}$ by using the equivalent circuit modeling and including the NQS effect. From derived $G_{max}$, $C_{gd}$ related pole gives the 10dB/decade $G_{max}$ roll-off in MSG, while the large slope of ~30-40dB/decade in MAG is due to additional poles in K or the NQS effect on $g_m$.

Although similar method can be used to calculate $f_{max}$ at $G_{max}=1$, unfortunately, no analytical solution can be derived for $f_{max}$. In contrast, analytical $f_{max}$ at MSG=1 can be obtained when $\left|\left(K-\sqrt{K^2-1}\right)\right|=1$, we have therefore analyzed $f_{max,MSG=1}$ to obtain a better understand of device design parameters on $f_{max,MSG=1}$.

Good agreement between the measured and calculated $f_{max,MSG=1}$ is achieved and shown in Table 1. The primirary parameter for $f_{max,MSG=1}$ increase is due to the $g_m$ increase and $C_{gd}$ decrease. In fact, $C_{gd}$ is dominated by the $C_{gdo}$ that is difficult to proportionally scale down with $L_g$.

We have also used numerical device simulation for further analysis. We have studied the NQS effect on $G_{max}$ and $f_{max}$. As shown in Fig. 1, the MAG increases with decreasing $R_{nqs}$ and eventually gives $G_{max}$ the same 10dB/decade roll-off as MSG when $R_{nqs}$ equals 0. Therefore, the NQS effect is responsible for the transition from MSG to MAG. Because $R_{nqs}$ is inversely related to $C_{gs}$, a higher dielectric or thinner gate thickness is required to improve the high frequency gain.

On the other hand, $G_{max}$ has a simple analytical solution in the most useful MSG region for amplifier design. Because the $R_{nqs}(C_{gs}+C_{gd})$ related zeros are effective only at high frequencies, $G_{max}$ in MSG can be further simplified and expressed by $g_m/\omega C_{gd}$ or $v_{sat}/\omega L_{ov}$. The numerical simulation result is shown in Fig. 2. It is clear that the reduction of $C_{gdo}$ leads to a higher $G_{max}$ and $f_{max}$. However, the difference between the ideal $2C_{ox}Wt_{ox}$ and the measured data is larger as scaling down.

Here, a minimum $C_{gdo}$ of $C_{ox}WL_{ov}$ ($L_{ov}=2t_{ox}$) [4] is required in order to develop a reproducible and manufacturable process, where $C_{ox}$ and $t_{ox}$ are the gate capacitance and oxide thickness, respectively. Although down scaling gives a smaller $L_g$ and a higher $C_{ox}$, limited $G_{max}$ improvement in MSG is due to the slower scalable $L_{ov}$. The reason for $L_{ov}$ failing to follow $t_{ox}$ scaling down in deep sub-μm devices is due to the lateral diffusion from source and drain impurities. High temperature annealing after source and drain implantation is necessary to reduce the junction leakage but largely increases the lateral diffusion. The formation of silicide junction also requires high temperature RTA. Because of the combined small $G_{max}$ and K factor improvement, limited $f_{max}$ improvement as device scaling down can be expected.

The smaller increase of measured $G_{max}$ than calculated value in Table 1 as down scaling may be due to the parasitic effect neglected in our device model.

## 五、參考文獻

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## Figure Captions:

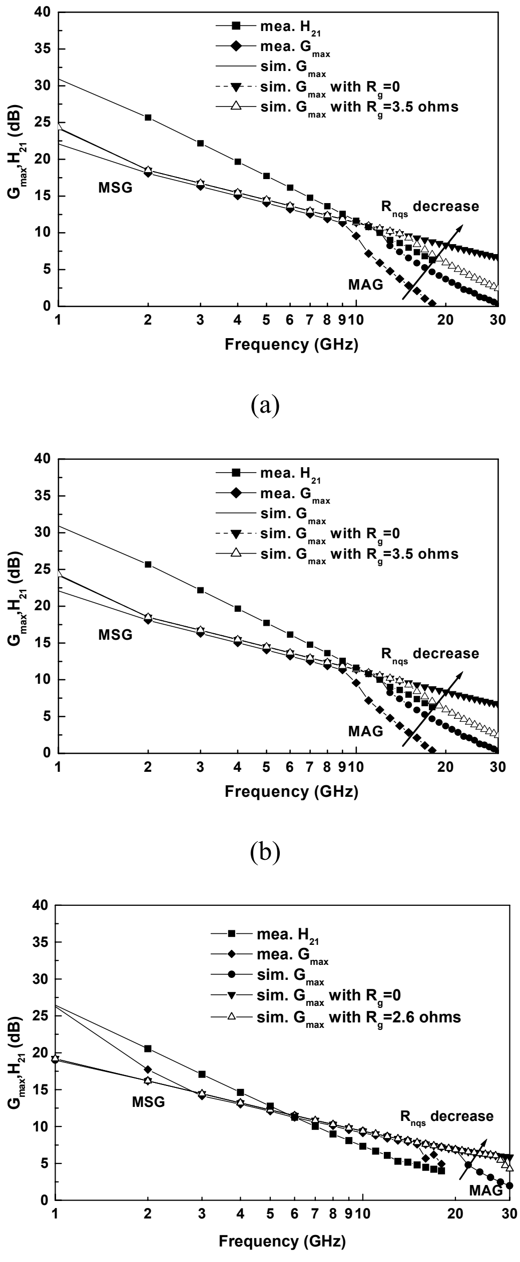
Table I Measured and calculated RF data.

Fig.1 Gain-frequency response for measured and simulated (a) 0.18, (b) 0.25, and (c) 0.5μm MOSFETs.

Fig.2 The effect of reducing $C_{gdo}$ on gain-frequency response for (a) 0.18, (b) 0.25, and (c) 0.5 μm MOSFETs.

Table I. Measured and calculated RF data.

| measured/ calculated values | mea. $H_{21}$ (dB) 4GHz | mea. $f_T$ (GHz) $H_{21}$ =1 | cal. $f_T$ (GHz) $H_{21}$ =1 | mea. $f_{max}$ (GHz) MAG =1 | mea. $f_{max}$ (GHz) MSG =1 | cal. $f_{max}$ (GHz) MSG =1 | mea. $G_{max}$ (dB) 4GHz | cal. $G_{max}$ (dB) 4GHz |
|---|---|---|---|---|---|---|---|---|
| 0.5-μm | 14.7 | 25 | 23 | 20 | 82 | 80 | 13.0 | 13.9 |
| 0.25-μm | 19.7 | 42 | 38 | 18 | 119 | 127 | 15.0 | 15.9 |
| 0.18-μm | 22.2 | 58 | 56 | 17 | 161 | 171 | 16.3 | 18.0 |

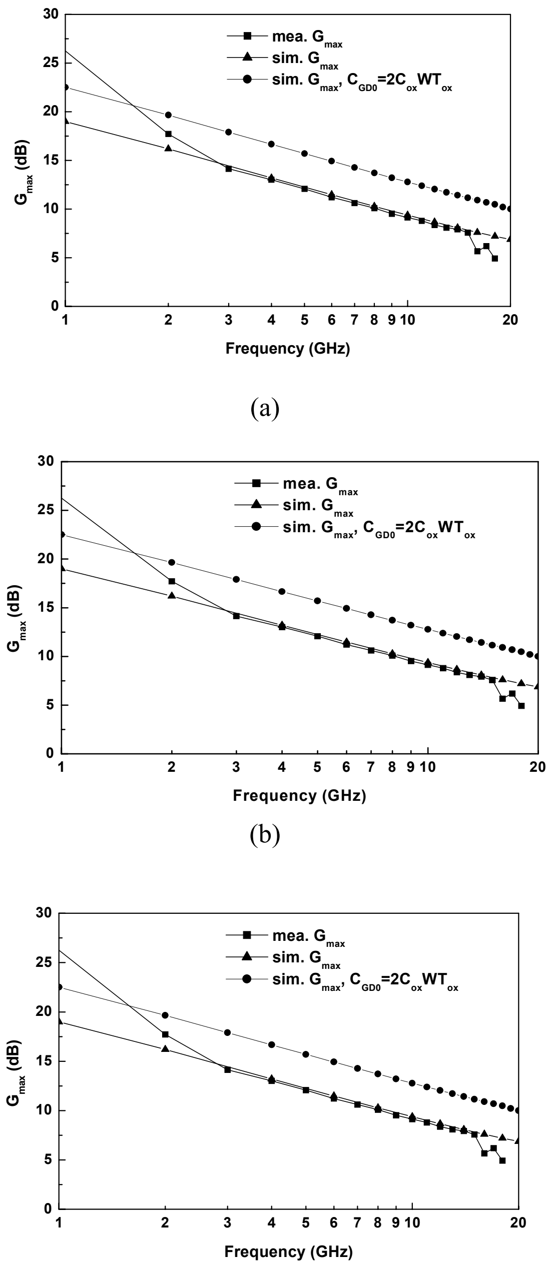


(a)

(b)

(c)

Fig. 1



(a)

(b)

(c)

Fig. 2