AIP Applied Physics Letters

Stress-induced morphology and fine-line stability enhancement of NiSi on poly-SiGe with a buffer polycrystalline silicon interlayer

Chi-Chang Wu, Wen-Fa Wu, Fu-Hsiang Ko, Hsin-Chiang You, and Wen-Luh Yang

Citation: Applied Physics Letters **92**, 182106 (2008); doi: 10.1063/1.2920202
View online: http://dx.doi.org/10.1063/1.2920202
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/92/18?ver=pdfcov
Published by the AIP Publishing

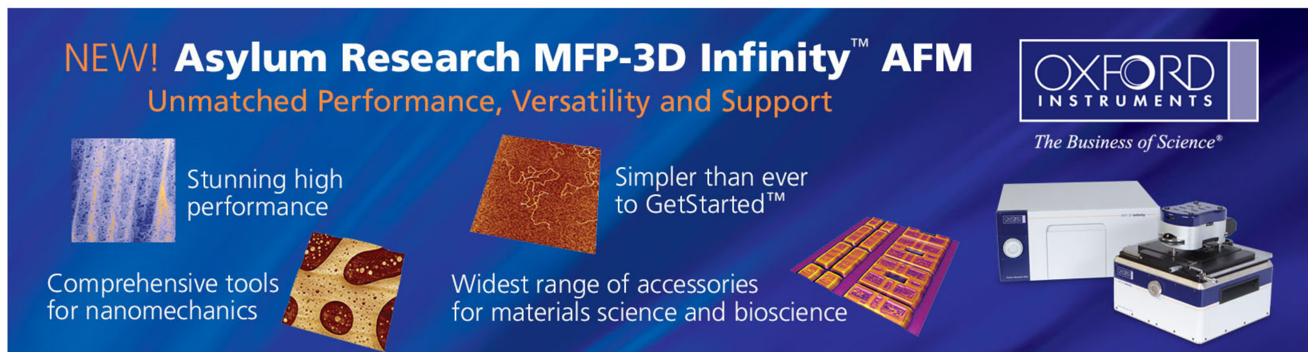
Articles you may be interested in
Thermal stability of supercritical thickness-strained Si layers on thin strain-relaxed buffers
J. Appl. Phys. **102**, 123502 (2007); 10.1063/1.2825042

Effect of Mo interlayer on thermal stability of polycrystalline NiSi thin films
J. Appl. Phys. **101**, 063544 (2007); 10.1063/1.2714490

Formation of nickel silicide and germanosilicide layers on Si(001), relaxed Si Ge Si (001) , and strained Si/relaxed Si Ge Si (001) and effect of postthermal annealing
J. Vac. Sci. Technol. A **24**, 1468 (2006); 10.1116/1.2210942

Ge fraction dependent improved thermal stability of in situ doped boron in polycrystalline Si 1 x Ge x (0 x 0.5) films on SiON
J. Appl. Phys. **97**, 054909 (2005); 10.1063/1.1854731

F-enhanced morphological and thermal stability of NiSi films on BF 2 + -implanted Si(001)
Appl. Phys. Lett. **81**, 5138 (2002); 10.1063/1.1533856



This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 23:05:31

Stress-induced morphology and fine-line stability enhancement of NiSi on poly-SiGe with a buffer polycrystalline silicon interlayer

Chi-Chang Wu,[1,2] Wen-Fa Wu,[2,a)] Fu-Hsiang Ko,[1,b)] Hsin-Chiang You,[3] and Wen-Luh Yang[4]
[1]*Institute of Nanotechnology and Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 300, Taiwan*
[2]*National Nano Device Laboratories, Hsinchu 300, Taiwan*
[3]*Department of Computer Science and Information Engineering, Asia University, Taichung 413, Taiwan*
[4]*Department of Electronic Engineering, Feng Chia University, Taichung 407, Taiwan*

(Received 14 January 2008; accepted 16 April 2008; published online 9 May 2008)

The thermal and morphological stability of NiSi is enhanced by inserting a polycrystalline (poly-Si) buffer layer between the Ni and poly-SiGe films. NiSi films formed on poly-Si/poly-SiGe stack layers possessed continuous, smooth structures after annealing at 500–850 °C. Moreover, nickel germanosilicide [Ni(Si, Ge)] lines formed on the poly-SiGe exhibited a fine-line effect, i.e., the sheet resistance increased upon decreasing the linewidth, whereas the sheet resistance of NiSi lines formed on the poly-Si/poly-SiGe stack layers remained less than 5 Ω/square. A model for the stress-confined grain growth and recrystallization is proposed to explain the improved properties of the poly-Si-buffered film. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2920202]

Nickel self-aligned silicidation (NiSi) is a critical process used to diminish contact resistance prior to metal interconnection in ultralarge-scale integration technology. This silicidation process is particularly important when the device dimensions are less than 100 nm. The formation of NiSi on gate electrodes improves the driving current and transconductance (G_m) of metal oxide semiconductor field effect transistor devices.[1]

Polycrystalline silicon-germanium (poly-SiGe) is a suitable candidate material for replacing polycrystalline silicon (poly-Si) at the gate electrode because of its lower dopant activation energy, higher carrier mobility,[2] and good compatibility with standard silicon complementary metal-oxide semiconductor processing technologies, as well as the possibility of tuning its work function merely by changing the mole fraction of Ge.[3] In addition, poly-SiGe films can be deposited at temperatures lower than those required for poly-Si films, presumably because of the lower binding energies of the Si–Ge and Ge–Ge bonds in poly-SiGe films relative to those of the Si–Si bonds in poly–Si films.[4] Unfortunately, combining nickel silicide processing with poly-SiGe materials suffers from the drawback that the direct reaction between nickel and poly-SiGe provides materials exhibiting relatively poor morphological stability relative to those obtained from poly-Si (Ref. 5) because the melting point of the ternary alloy Ni(Si, Ge) is lower than that of NiSi. This problem restricts the further application of nickel silicide and poly-SiGe gate materials.

In this paper, we compare the morphological stabilities and fine-line effects of Ni/poly-Si/SiO_2/Si-substrate, Ni/poly-SiGe/SiO_2/Si-substrate, and Ni/poly-Si/poly-SiGe/SiO_2/Si-substrate systems. We studied the effects of the silicidation temperature on the sheet resistance of various films. In addition, we examined the fine-line effects of nickel (germano) silicided narrow lines. Although it has been reported that the resistance of NiSi formed on poly-Si lines exhibits independent geometrical dimensions,[6] no literature exists describing the electrical properties of Ni(Si, Ge) formed on narrow poly-SiGe lines. Thus, we evaluated the morphology and recrystallization effects of these films, and propose a model that accounts for the stress-induced grain growth suppression and recrystallization effects.

These experiments employed 6 in. (100)-oriented silicon wafers. A 500 nm thick silicon oxide film was first formed, followed by the deposition of a (1) 200 nm poly-Si film, (2) 200 nm poly-SiGe layer, or (3) 40 nm poly-Si/160 nm poly-SiGe stack layer. After Radio Corporation of America (RCA) standard cleaning, 10 nm Ni and 4 nm TiN films were deposited through dc sputtering. After metal deposition, the Ni-silicidation reaction was performed in a rapid thermal annealing system. Finally, a mixture of H_2SO_4 and H_2O_2 (3:1) was used to selectively remove the unreacted metal at a temperature of 120 °C. The sheet resistance of the silicide film was determined using a four-point probe system. A bridge structure was used in conjunction with an Agilent 4156A semiconductor analyzer to characterize the values of resistance of various narrow lines. The morphology of the film was examined using transmission electron microscopy (TEM). The stresses of these films were measured using a Tencor FLX-2320 instrument.

After performing the silicidation reaction, the stacked (1) Ni/poly-Si/SiO_2/Si-substrate, (2) Ni/poly-SiGe/SiO_2/Si-substrate, and (3) Ni/poly-Si/poly-SiGe/SiO_2/Si-substrate films were transformed into (i) NiSi/poly-Si/SiO_2/Si-substrate, (ii) $Ni(Si_{1-x}Ge_x)$/poly-SiGe/SiO_2/Si-substrate, and (iii) NiSi/poly-SiGe/SiO_2/Si-substrate species, respectively. The phase for sample (iii) was identified to be NiSi by x-ray diffraction. Figure 1(a) provides a comparison of the sheet resistances of these films as a function of the annealing temperature. The sheet resistances of samples (i) and (ii) slightly increased upon increasing the annealing temperature over the range 500–800 °C and then abruptly increased at temperatures higher than 850 °C. In contrast, the resistance of sample (iii) remained constant after annealing at temperatures between 500 and 850 °C. This observation sug-

a)Electronic mail: wfwu@ndl.org.tw.
b)Electronic mail: fhko@mail.nctu.edu.tw.

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 23:05:31

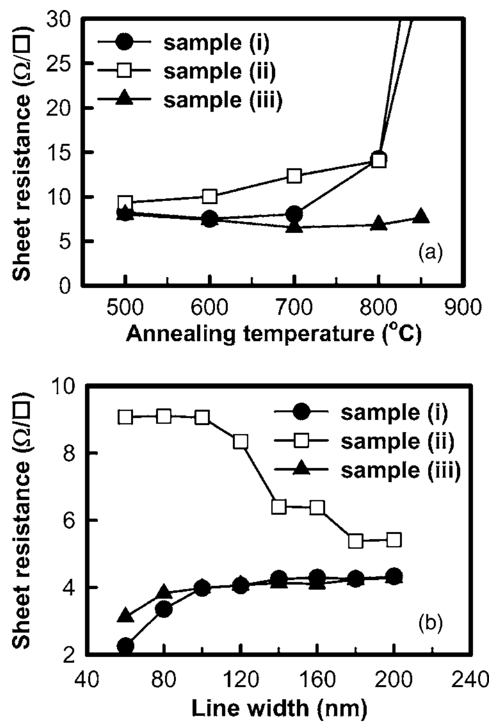


FIG. 1. (a) Sheet resistances of the nickel (germano)silicide films formed on poly-Si [sample (i)], poly-SiGe [sample (ii)], and poly-Si/poly-SiGe stack layers [sample (iii)] as a function of the annealing temperature. (b) Sheet resistances of the nickel [germano]silicide lines annealed at 600 °C as a function of the linewidth.

gests that the insertion of the buffer film, i.e., poly-Si, between the Ni and poly-SiGe films was beneficial to the electrical and thermal properties.

Figure 1(b) displays the sheet resistances of various narrow lines of samples (i)–(iii) annealed at 600 °C. The sheet resistance of lines of sample (i) remained nearly constant for linewidths ranging from 200 to 100 nm, which is consistent with previous findings.[7] The slight decrease in resistance that occurred after shrinking the linewidth from 100 to 60 nm was caused by edge effects of the recessed spacer forming a thicker silicide at the line's edge.[8] In contrast, the sheet resistance for sample (ii) increased upon reducing the linewidth. This phenomenon, the well-known fine-line effect, had been reported from a study of Ti silicide,[9] but has never been reported for Ni(Si, Ge) lines formed on poly-SiGe. The fine-line effect vanished after insertion of poly-Si, i.e., for sample (iii). This behavior should improve the process stability of such systems, especially for sub-100 nm devices. We infer that the larger Ni(Si, Ge) grains resulting from the ready grain growth of poly-SiGe after annealing was the main cause of the increased sheet resistance in sample (ii). Similar behavior resulting from grain size effects has been previously described.[10]

Figure 2 displays cross-sectional TEM micrographs of the silicide films obtained after annealing at 850 °C. Samples (i) and (ii) [Figs. 2(a) and 2(b), respectively] possessed completely agglomerated silicide structures that were responsible for the poor electrical properties observed in Fig. 1. These images also reveal the occurrence of layer inversion, i.e., the reversal of the positions of the silicide and poly-Si(Ge) layers, which is consistent with previous findings.[11] These agglomerated silicide islands resulted from poly-Si(Ge) grain growth and a recrystallization effect dur-

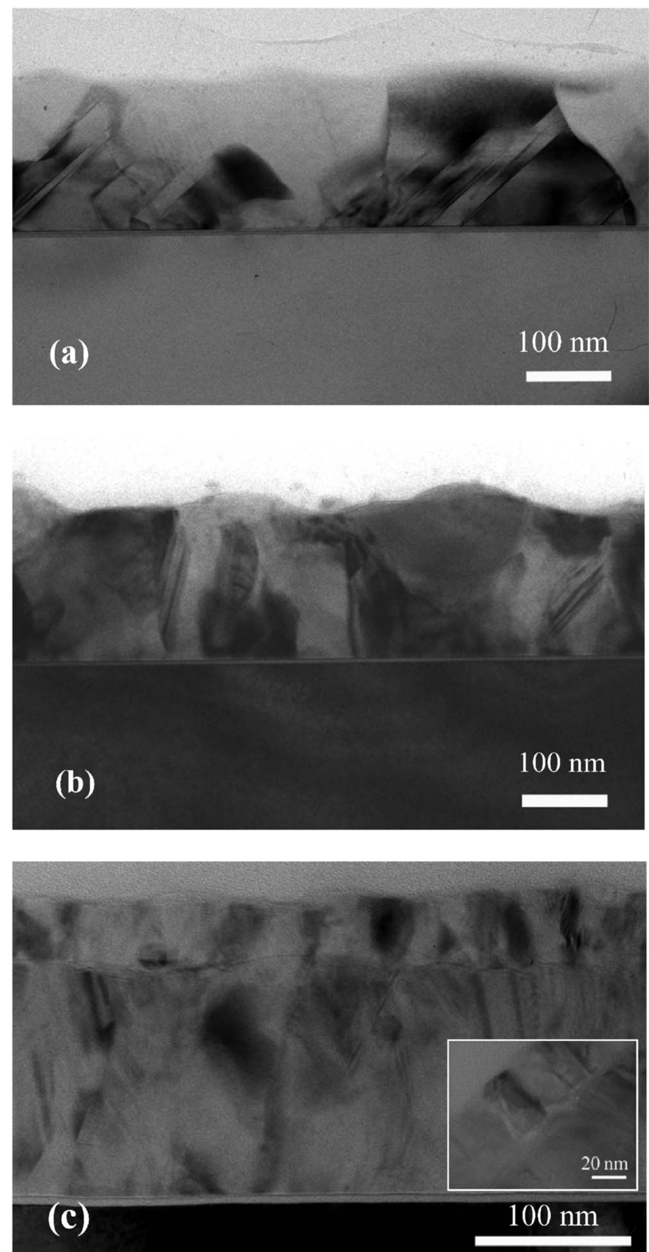


FIG. 2. Cross-sectional TEM micrographs of the nickel (germano)silicide films formed on (a) poly-Si [sample (i)], (b) poly-SiGe [sample (ii)], and (c) poly-Si/poly-SiGe stack layers [sample (iii)] after annealing at 850 °C.

ing treatment at high temperatures. Moreover, Chen *et al.* have reported that the Ge segregation effect of Ni(Si, Ge) would result in a more severe thermal stability problem for Ni(Si, Ge) formed on poly-SiGe.[12] The segregation of Ge from Ni(Si, Ge) grains is driven by the heat of formation for NiSi being more favorable than that of NiGe. In contrast, the grains in sample (iii) retained their columnar structure and a uniform interface existed between the silicide and poly-SiGe [see Fig. 2(c) and its inset]. The uniform interface is likely caused by the Ge, which is expelled from the Ni–Si–Ge compound, blocked the Ni diffusion paths, and resulted in the delay in the formation of $NiSi_2$.[13,14] Similar results were also reported for $CoSi_2$ formed on a SiGe layer.[15] This observation implies that the insertion of the poly-Si film in sample (iii) maintained the film's continuance and curtailed agglomeration in the silicide film.

In Fig. 3, we propose a model to explain the stress-induced grain growth suppression of the silicide film. In

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 23:05:31

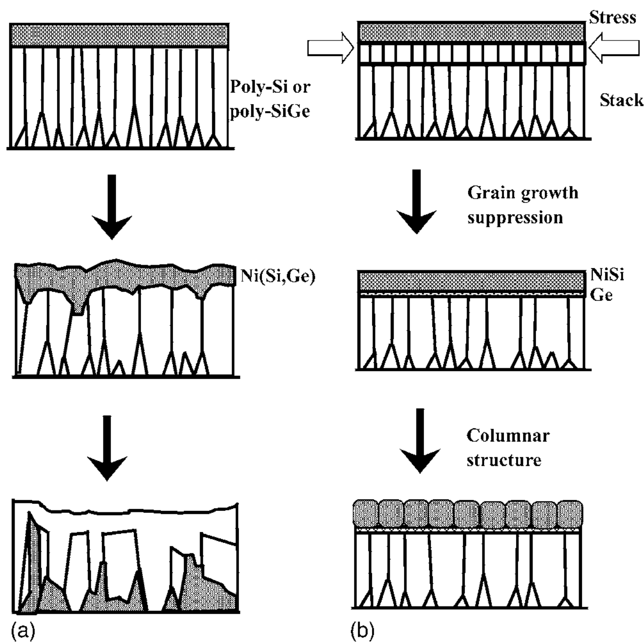


FIG. 3. Schematic models of nickel (germano)silicide formation at high annealing temperatures: (a) on poly-Si [sample (i)] and poly-SiGe [sample (ii)] and (b) on poly-Si/poly-SiGe stack layers [sample (iii)].

terms of thermodynamics, the driving force for the morphological transformation of a grain is the reduction in interfacial energy. Figure 3(a) schematically displays the morphology changes that occurred to samples (i) and (ii) after annealing. Increasing the annealing temperature enhances the sizes of the poly-Si and poly-SiGe grains, with the silicide migrating along the grain boundary, ultimately resulting in agglomerated island and layer inversion occurring at excessively high temperatures.[16] Figure 3(b) provides an explanation of the benefit of inserting the poly-Si film into sample (iii). The underlying poly-SiGe layer exerts a compressive stress upon the upper poly-Si film. This stress suppressed the grain growth of the poly-Si and silicide, which in turn retarded the agglomeration and layer inversion effects. In addition, the Ge layer between the silicide and poly-SiGe film also play the role to retard layer inversion.[13–15] This model can also explain the behavior of the Ni(Si, Ge) fine lines of sample (ii). The thermal stability of silicided-narrow lines is determined by the laterally confined areas, and larger grains induce linewidth-dependent degradation.[17] Larger silicide grains readily formed columnar structures and then converted into bamboolike structures as the linewidth shrank. Agglomeration into islands then occurred during annealing. For sample (iii), the fine-line effect was eliminated in the presence of the inserted poly-Si layer because of suppression in the growth of silicide grains. Therefore, the formation of bamboolike structures was retarded.

To support this model with respect to the stress effect in sample (iii), we prepared three samples having various poly-SiGe film thicknesses. We found that samples possessing smaller compressive stresses exhibited inferior electrical properties after annealing at high temperatures, especially when the annealing temperature exceeded 850 °C. This finding is consistent with our prediction that compressive stress enhances the thermal and morphological stabilities of nickel silicide samples.

In conclusion, we have investigated the thermal stability and electrical behavior of various nickel (germano) silicide structures. The insertion of a poly-Si film on the poly-SiGe significantly enhances the thermal and morphological stabilities of NiSi films. We have derived a stress-confined grain growth and Ge blocking model to explain the beneficial effects of the poly-Si film and confirm the predictions made after scrutiny of TEM images. The presence of poly-Si films improved the properties of both the thin-film and fine-line NiSi structures.

[1] C. C. Wu, W. F. Wu, P. Y. Su, L. J. Chen, and F. H. Ko, Microelectron. Eng. **84**, 1801 (2007).
[2] X. Yu, C. Zhu, and M. Yu, Appl. Phys. Lett. **89**, 163508 (2006).
[3] J. Huang, N. Wu, Q. Zhang, C. Zhu, M. F. Li, A. A. O. Tay, Z. Y. Cheng, C. W. Leitz, and A. Lochtefeld, Appl. Phys. Lett. **88**, 143506 (2006).
[4] M. Mitsui, K. Arimoto, J. Yamanaka, and K. Nakagawa, Appl. Phys. Lett. **89**, 192102 (2006).
[5] J. Seger, T. Jarmar, Z. B. Zhang, H. H. Radamson, F. Ericson, U. Smith, and S. L. Zhang, J. Appl. Phys. **96**, 1919 (2004).
[6] Y. He, X. L. Liu, J. Y. Feng, and Q. L. Wu, J. Appl. Phys. **96**, 6928 (2004).
[7] H. Iwai, T. Ohguro, and S. I. Ohmi, Microelectron. Eng. **60**, 157 (2002).
[8] Q. Xiang, C. Woo, E. Paton, J. Foster, B. Yu, and M. R. Lin, *IEEE Conference Proceedings, 2000 Symposium on VLSI Technology, Digest of Technical Papers*, p. 76 (2000).
[9] S. L. Zhang and U. Smith, J. Vac. Sci. Technol. A **22**, 1361 (2004).
[10] R. W. Mann, G. L. Miles, T. A. Knotts, D. W. Rakowski, L. A. Clevenger, J. M. E. Harper, F. M. d'Heurle, and C. Cabral, Jr., Appl. Phys. Lett. **67**, 3729 (1995).
[11] T. Jarmar, J. Seger, F. Ericson, D. Mangelinck, U. Smith, and S.-L. Zhang, J. Appl. Phys. **92**, 7193 (2002).
[12] L. J. Chen, J. B. Lai, and C. S. Lee, Micron **33**, 535 (2002).
[13] W. W. Wu, S. L. Cheng, S. W. Lee, and L. J. Chen, J. Vac. Sci. Technol. B **21**, 2147 (2003).
[14] W. W. Wu, J. H. He, S. L. Cheng, S. W. Lee, and L. J. Chen, Appl. Phys. Lett. **83**, 1836 (2003).
[15] W. W. Wu, T. F. Chiang, S. L. Cheng, S. W. Lee, L. J. Chen, Y. H. Peng, and H. H. Cheng, Appl. Phys. Lett. **81**, 820 (2002).
[16] P. S. Lee, K. L. Pey, D. Mangelinck, J. Ding, D. Z. Chi, J. Y. Dai, and L. Chan, J. Electrochem. Soc. **149**, 331 (2002).
[17] K. Maex, Mater. Sci. Eng., R. **11**, 53 (1993).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 23:05:31