高速雙絞線網路發收機單晶片系統 (III)
High-Speed UTP Network Transceiver SOC (III)

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1 摘要

本計畫將設計一數位類比混合式單晶片系統之發收機. 此發收機將用於雙絞線 250 Mbps 之資訊傳輸. 調變方法是根據 Gigabit Ethernet 標準訂定的 125 Mbaud 符元率 5 階之脈波振幅調變 (PAM). 較複雜之發收機功能, 如通道編碼和解碼, 等化, 以及時序還原等, 將使用數位訊號處理之技術. 而類比電路, 如放大器, 數位類比轉換器, 類比數位轉換器, 以及數位相位轉換器等則是處於數位處理器和傳輸介質之間的介面.

關鍵詞: 數位類比混合式積體電路, 發收機, 十億位元乙太網路, 單晶片系統.

Abstract

This project is to design a mixed-signal transceiver system on a chip for 250 Mbps data transmission over an unshielded twisted pair (UTP) cable. Partially following the Gigabit Ethernet standard, a 5-level baseband pulse amplitude modulation (PAM) with 125 Mbaud symbol rate is assumed. Digital signal processing techniques are used in channel encoding/decoding, equalization, and timing recovery. Analog circuits, such as amplifiers, digital-to-analog converters, analog-to-digital converters, and digital-to-phase converters, provide the interface between the digital processor and the transmission media.

Key Words: Mixed-Signal Integrated Circuit, Transceiver, Gigabit Ethernet, System on A Chip.

2 Motivation and Objectives

Deep submicron CMOS technologies have enabled cost-effective multi-million-transistor integrated circuits capable of powerful digital computing. As a results of such advances, high-performance digital communication systems, that employ sophisticated signal processing techniques to overcome transmission media imperfections and various interferences, have become affordable to the average consumers and filled the need for ever growing broadband services.

In a modern physical-layer transceiver, although most signal processing functions are performed in the digital domain, analog circuitry is always required for interfacing between the digital functional units and the transmission media. A good design methodology that enable both the analog and digital functional blocks to operate together monolithically is the key to realize a successful transceiver system on a chip (SOC).

This project is investigate the mixed-signal SOC design techniques for implementing a broad-band network transceiver. The transceiver will be designed for high-speed data transmission over an unshielded twisted pair (UTP) cable in the LAN environment fol-

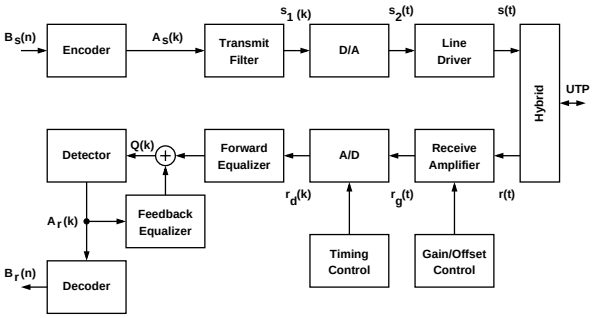

Figure 1: Transceiver block diagram.

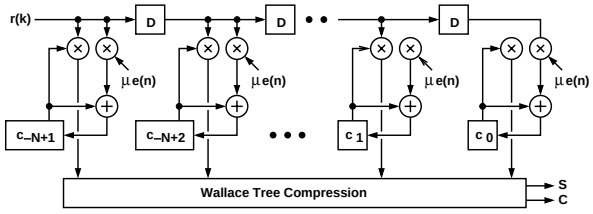

Figure 2: Feedforward equalizer (FFE) filter.

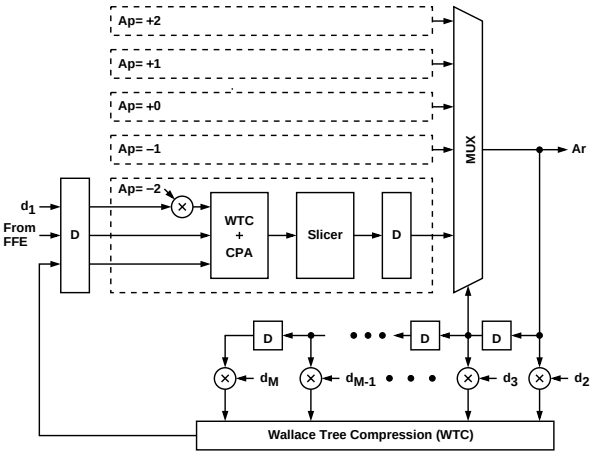

Figure 3: Decision-feedback equalizer (DFE) filter.

lowing the Gigabit Ethernet standard [1]. In addition, new mixed-signal circuit techniques will be investigated for transceiver functions such as automatic gain control, digital-to-analog converters, analog-to-digital converters, and timing recovery.

3 Accomplishments

3.1 Transceiver Architecture

The block diagram of the base-band transceiver for this project is shown in Fig. 1. We assume the symbol rate is 125 Mbaud, and each symbol is a PAM-5 code. The UTP cable is limited to less than 100 meter long. Several adaptive control mechanisms are required in the receiver, such as gain/offset control to maximize dynamic range, timing control to recover symbol clock, feedforward equalization (FFE) and decision-feedback equalization (DFE) to eliminate inter-symbol interference (ISI). The system is operated with symbol-rate sampling, i.e., system clock is 125 MHz. Besides bandwidth, linearity must be considered in designing the analog signal path to guarantee the required signal-to-noise ratio.

An analog-digital mixed-signal simulation platform is established for transceiver design. The simulator is written in C++ programming language and based upon the SystemC class library [2]. All functional blocks are implemented as modules for easy reuse and maintenance. The operation of digital modules is cycle-based, making them easy for direct hardware translation. The UTP channel is measured, and approximated by the s-domain transfer functions in the simulation.

3.2 Digital Equalizer

Fig. 2 shows the architecture of the FFE. The coefficient updating for c_j follows the least-mean-square (LMS) adaptation algorithm. Fig. 3 shows the architecture of the DFE, which includes the slicers and an adaptive FIR filter. The coefficient updating for d_j also follows the LMS adaptation algorithm. The symbol-lookahead parallel processing technique is used to ensure that the operation of DFE's convolution and summation with FFE's output can be completed in one clock cycle.

Realized with 0.25 μm CMOS standard cell library, the total area of the FFE and DFE is 1.37×1.37 mm^2 [3]. The FFE's critical-path delay is 6.75 nsec. In the DFE, the critical-path delay is 4.85 nsec for the multi-path slicer block, and is 5.48 nsec for the FIR filter block. The power dissipation of the entire equalizer

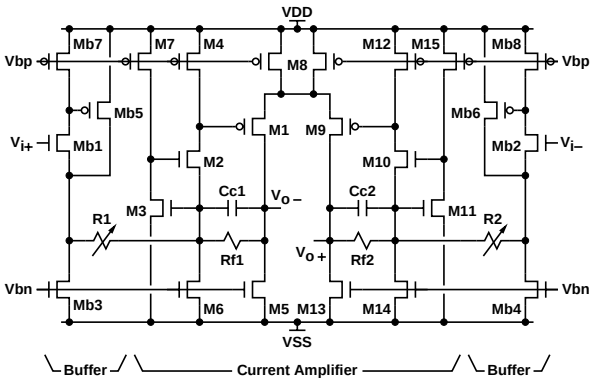

Figure 4: PGA circuit schematic.

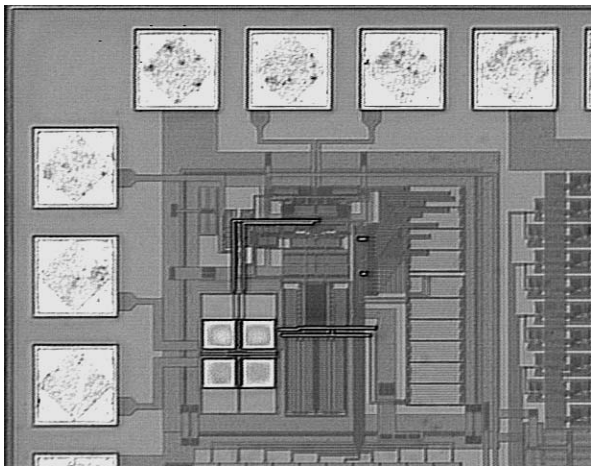

Figure 5: PGA chip microphotograph.

is 460 mW.

3.3 PGA

The programmable-gain amplifier (PGA) is placed in the receiver's front end. Its gain is digitally controlled by an automatic gain/offset control block so that receiver's dynamic range can be maximized. Shown in Fig. 4, the PGA is based on the current-mode technique to achieve high linearity and wide bandwidth simultaneously while minimizing power dissipation. The PGA's voltage gain is varied by changing the resistance of the input variable resistors, R_1 and R_2, which are realized using MOSFET switches linearized by polysilicon resistors in series connection.

Fig. 5 shows the chip photograph of the PGA fabricated in a 0.35 μm CMOS technology [4]. Active area is 0.18 mm^2. The PGA's voltage gain can vary from 0 dB to

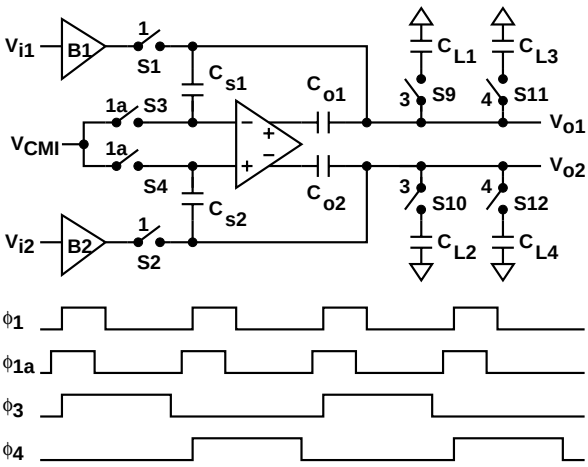

Figure 6: SHA block diagram.

19 dB with a db-linear step size of 2 dB, while maintaining a constant bandwidth of 125 MHz when driving 2 pF capacitive loads. The PGA exhibits third-order intermodulation distortion (IM3) ≤ -60 dB at 1 Vpp output for 0–70 MHz and -79 dB at 10 MHz with 2 Vpp output. The differential input noise is as low as 8.63 nV$/\sqrt{\text{Hz}}$. Power dissipation is 21 mW from a 3.3 V supply.

3.4 SHA

The block diagram of the sample-and-hold amplifier (SHA) is shown in Fig. 6 [5], which can be used in a two-path time-interleaved ADC system. In the fully-differential bottom-plate sampling configuration, the switches S3 and S4 are turned off before S1 and S2, reducing the effects of aperture jitter and switching error due to clock feedthrough and charge injection. The combination of precharging and opamp output capacitor coupling can reduce the requirements for the opamp's the dc gain, unity-gain bandwidth, and output voltage swing.

The precharged SHA is fabricated in a standard 0.25μm CMOS process. Operating from a 2.5 V supply, the total power dissipation is 33 mW. The chip microphotograph is shown Fig. 7. With a 50.038 MHz 2 Vpp sinusoidal input at 100 MHz sampling frequency, the 3rd-order harmonic distortion is measured to be less than -78 dB.

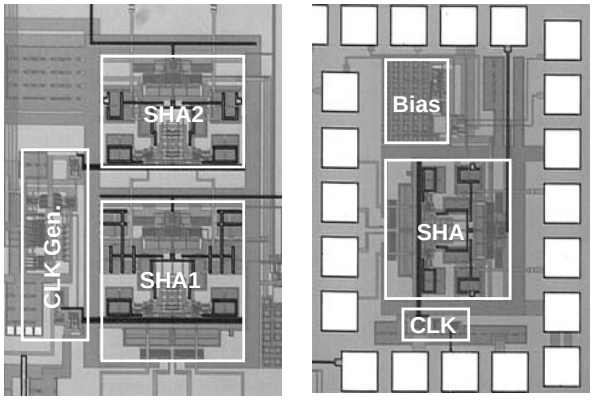

Figure 7: SHA chip microphotograph.

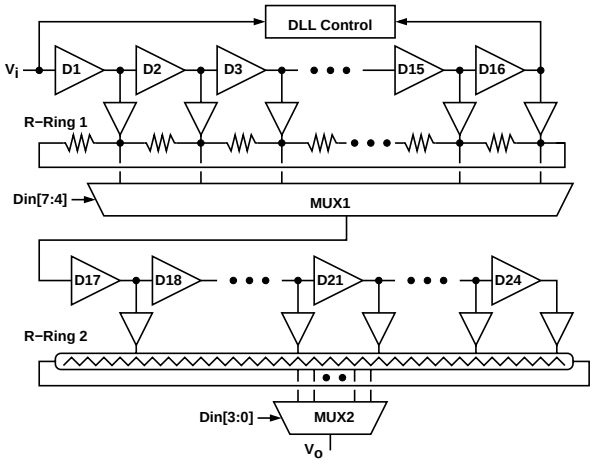

Figure 8: DPC block diagram

3.5 DPC

The digital-to-phase converter (DPC) produces the system clock for the receiver. Its clock phase relative to the received input is digitally controlled by a timing control block so that the receiver's signal-to-noise ratio is maximized. An 8-bit 125 MHz digital-to-phase converter (DPC) is shown in Fig. 8. The DPC receives a reference clock at V_i and generate a clock at V_o with phase controlled by the digital input Din[7:0]. The DPC consists of two delay lines, D1–D16 and D17–D24. All delay cells are identical and have the same time delay. The delay is controlled by a DLL, so that the total delay of the first delay line, D1–D16, is one clock period. The first ring, R-Ring 1, is added to reduce phase error caused by mismatches among the delay cells as well as the buffers driving the MUX1 [6]. The second ring, R-Ring 2, interpolates additional 16 phases from the delay of a single delay cell.

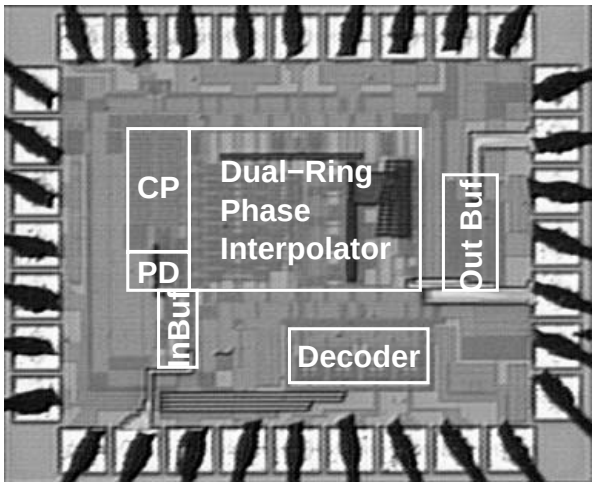

Figure 9: DPC chip photograph.

Fig. 9 shows the chip micrograph of the DPC fabricated in a 0.35 μm CMOS technology. Die area is 980 × 1180 μm^2. Input frequency can be varied from 50 MHz to 250 MHz. Power dissipation is 110 mW from a 3.3 V supply. The measured output jitter at 125 MHz is 5.1 psec rms. The DNL is less than ±1 LSB at most of the input codes, except the recurring −1.8 LSB DNL errors every 16 input codes. The integral nonlinearity (INL) is less than ±2 LSB.

4 Conclusions

In this project, we have studied the modern broad-band transceiver architectures, which utilize complex signal processing techniques and multiple adaptive control loops. A C++ mixed-signal simulation platform has been established for full transceiver simulation.

Several key functional blocks have been studied and realized in silicon, which include a fully-digital cell-based 125 MHz adaptive equalizer, a 125 MHz constant bandwidth programmable-gain amplifier with high linearity, a 100 MHz low-distortion sample-and-hold amplifier, and a 125 MHz 8-bit digital-to-phase converter. Those functional blocks have specifications better than the original transceiver requirements, and can be used in

other high-performance applications such as software radios.

A new low-voltage class-AB UTP driver and a new pipelined analog-to-digital converter are still under investigation.

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