Sensitivity of Multigate MOSFETs to Process Variations—An Assessment Based on Analytical Solutions of 3-D Poisson's Equation

Yu-Sheng Wu and Pin Su, *Member, IEEE*

***Abstract*—This paper investigates the sensitivity of multigate MOSFETs to process variations using analytical solutions of 3-D Poisson's equation verified with device simulation. FinFET and Tri-gate with both heavily doped and lightly doped channels have been examined regarding their immunity to process-induced variations and dopant number fluctuation. Our study indicates that lightly doped FinFET has the smallest threshold voltage ($V_{\rm th}$) dispersion caused by process variations and dopant number fluctuation. For heavily doped devices, dopant number fluctuation may become the dominant factor in the determination of overall $V_{\rm th}$ variation. The $V_{\rm th}$ dispersion of Tri-gate may therefore be smaller than that of FinFET because of its better immunity to dopant number fluctuation.**

***Index Terms*—3-D Poisson's equation, FinFET, multigate MOSFETs, Tri-gate, variation.**

I. Introduction

DUE to its better gate control, multigate structure is an important candidate for CMOS scaling [1]–[3]. Dependent on the aspect ratio (AR), FinFET (AR>1) and Tri-gate (AR = 1) are two main options in the multigate device design. Whether there is an optimum choice between the two options merits investigation.

For nano-CMOS device design, the challenge lies in dispersions [4]. They are mainly due to process variations and dopant fluctuation that result in the dispersion of threshold voltage, and are closely related to the device electrostatics [4]. In other words, electrostatics and variability are crucial in assessing the feasibility of various multigate options. In this paper, we tackle these issues using theoretical calculations. We conduct a comprehensive comparison of sensitivity to process variations between FinFET and Tri-gate based on their electrostatics using analytical solutions of 3-D Poisson's equation.

This paper is organized as follows. In Section II, we derive an analytical potential distribution for a multigate device structure. The threshold voltage ($V_{\rm th}$) can then be determined based on the potential solution. In Section III, we investigate the $V_{\rm th}$ sensitivity to process variations for FinFET and Tri-gate based on our theoretical calculation. The conclusions will be drawn in Section IV.

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The authors are with the Department of Electronics Engineering, National Chiao Tung University, Hsinch 30013, Taiwan (e-mail: oison.ee93g@nctu.edu.tw; pinsu@mail.nctu.edu.tw).

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II. Potential Solution and $V_{\rm th}$ Calculation

An analytical potential solution is crucial to the derivation of device subthreshold characteristics such as $V_{\rm th}$. Fig. 1(a) shows the schematic sketch of a multigate SOI structure. The Si-fin body covered by gate insulator is a cuboid with six faces, and each face is connected to a voltage bias. In the subthreshold regime, the Si-fin body is fully depleted with negligible mobile carriers. Therefore, the potential distribution $\phi(x,y,z)$ satisfies the Poisson's equation

$$\frac{\partial^2\phi(x,y,z)}{\partial x^2}+\frac{\partial^2\phi(x,y,z)}{\partial y^2}+\frac{\partial^2\phi(x,y,z)}{\partial z^2}=-\frac{qN_a}{\varepsilon_{\rm si}} \quad (1)$$

where N_a is the doping concentration of the Si-fin. The required boundary conditions can be described as

$$\phi(W_{\rm fin},y,z)+t_{i,f}\frac{\varepsilon_{\rm si}}{\varepsilon_i}\frac{\partial\phi(x,y,z)}{\partial x}\bigg|_{x=W_{\rm fin}}=V_{\rm fg}-V_{\rm fb} \quad (2a)$$

$$\phi(0,y,z)-t_{i,b}\frac{\varepsilon_{\rm si}}{\varepsilon_i}\frac{\partial\phi(x,y,z)}{\partial x}\bigg|_{x=0}=V_{\rm bg}-V_{\rm fb} \quad (2b)$$

$$\phi(x,y,H_{\rm fin})+t_{i,t}\frac{\varepsilon_{\rm si}}{\varepsilon_i}\frac{\partial\phi(x,y,z)}{\partial z}\bigg|_{z=H_{\rm fin}}=V_{\rm tg}-V_{\rm fb} \quad (2c)$$

$$\phi(x,y,0)-t_{{\rm ox},u}\frac{\varepsilon_{\rm si}}{\varepsilon_{\rm ox}}\frac{\partial\phi(x,y,z)}{\partial z}\bigg|_{z=0}=V_{\rm ug}-V_{\rm fb} \quad (2d)$$

$$\phi(x,0,z)=-\phi_{\rm ms} \quad (2e)$$

$$\phi(x,L_{\rm eff},z)=-\phi_{\rm ms}+V_{\rm DS} \quad (2f)$$

where $\varepsilon_{\rm si}, \varepsilon_i$ and $\varepsilon_{\rm ox}$ are dielectric, constants of the Si-fin, gate dielectric and oxide, respectively. $W_{\rm fin}, H_{\rm fin}$, and $L_{\rm eff}$ are defined as fin width, fin height, and channel length, respectively. $t_{i,t}, t_{i,f}, t_{i,b}$, and $t_{{\rm ox},u}$ are thicknesses of top gate dielectric, front gate dielectric, back gate dielectric, and buried oxide, respectively. $V_{\rm fg}$, $V_{\rm bg}$, $V_{\rm tg}$, $V_{\rm ug}$, and $V_{\rm DS}$ are the voltage biases of front gate, back gate, top gate, buried gate, and drain terminal, respectively. $V_{\rm fb}$ is the flat-band voltage for these gate terminals. $\phi_{\rm ms}$ is the built-in potential of the source/drain to the channel.

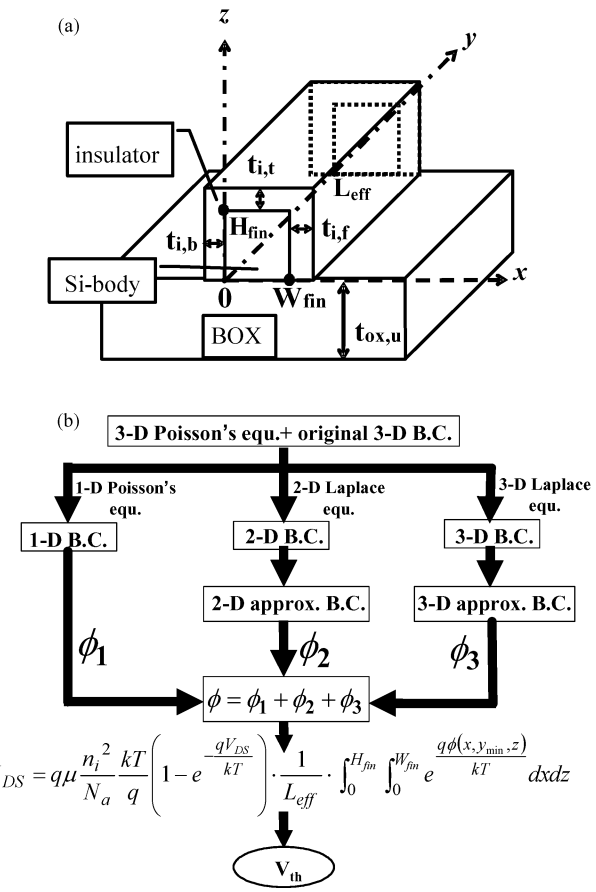

Fig. 1. (a) Schematic sketch of the multigate device structure investigated in this study. (b) Flow chart demonstrating the $V_{\rm th}$ calculation of multigate devices. Approximation was made to simplify the 2-D and 3-D boundary conditions (B.C.) to obtain a simplified channel potential solution form.

Fig. 1(b) shows the flow chart of the $V_{\rm th}$ calculation by solving the 3-D boundary value problem. This 3-D boundary value problem can be divided into three sub-problems, including 1-D Poisson's equation, 2-D, and 3-D Laplace equation. Using the superposition principle, the complete potential solution is $\phi = \phi_1 + \phi_2 + \phi_3$, where ϕ_1, ϕ_2, and ϕ_3 are solutions of the 1-D, 2-D, and 3-D sub-problems, respectively. The 1-D solution ϕ_1 can be expressed as

$$\phi_1(z) = -\frac{qN_a}{2\varepsilon_{\rm si}} z^2 + az + b \tag{3a}$$

$$a = \frac{(V_{\rm tg} - V_{\rm fb}) - (V_{\rm ug} - V_{\rm fb}) + (qN_a/(2\varepsilon_{\rm si}))\,(H_{\rm fin}^2 + 2(\varepsilon_{\rm si}/\varepsilon_i) t_{i,t} H_{\rm fin})}{H_{\rm fin} + (\varepsilon_{\rm si}/\varepsilon_i) t_{i,t} + (\varepsilon_{\rm si}/\varepsilon_{\rm ox}) t_{{\rm ox},u}} \tag{3b}$$

$$b = \frac{\varepsilon_{\rm si}}{\varepsilon_{\rm ox}} t_{{\rm ox},u} a + (V_{\rm ug} - V_{\rm fb}) \tag{3c}$$

In solving the 2-D and 3-D sub-problems, approximation was made to avoid the numerical iterations required in finding the eigenvalues [5] and to simplify the solution form. The boundary conditions [(2a)–(2d)] are simplified by converting the gate dielectric thickness to $(\varepsilon_{\rm si}/\varepsilon_{\rm i})$ times and replacing the gate dielectric region with an equivalent Si region [6]. The electric field discontinuity across the gate dielectric and Si-fin interface can thus be eliminated. In other words, the Si-fin body and the gate dielectric region are treated as a homogeneous silicon cuboid with an effective width $W_{\rm eff}$ and an effective height $H_{\rm eff}$ given by (4) and (5), respectively.

$$W_{\rm eff} = W_{\rm fin} + \frac{\varepsilon_{\rm si}}{\varepsilon_i} (t_{i,f} + t_{i,b}) \tag{4}$$

$$H_{\rm eff} = H_{\rm fin} + \frac{\varepsilon_{\rm si}}{\varepsilon_i} t_{i,t} + t_{{\rm ox},u}\,. \tag{5}$$

The 2-D solution ϕ_2 can be obtained using the method of separation of variables

$$\phi_2(x,z) = \sum_{i=1}^{\infty} \left[c_i \sinh\left(\frac{i\pi}{H_{\rm eff}} \left(x + \frac{\varepsilon_{\rm si}}{\varepsilon_i} t_{i,b}\right)\right) + c_i' \sinh\left(\frac{i\pi}{H_{\rm eff}} \left(W_{\rm eff} - \left(x + \frac{\varepsilon_{\rm si}}{\varepsilon_i} t_{i,b}\right)\right)\right)\right] \times \sin\left(\frac{i\pi}{H_{\rm eff}} (z + t_{{\rm ox},u})\right) \tag{6a}$$

where

$$c_i = \frac{1}{\sinh\left(i\pi (W_{\rm eff}/H_{\rm eff})\right)} \left[2 (V_{\rm fg} - V_{\rm fb} - b) \frac{1 - (-1)^i}{i\pi} + 2a \left(\frac{t_{{\rm ox},u}}{i\pi} + \frac{(H_{\rm eff} - t_{{\rm ox},u})(-1)^i}{i\pi} \right) + \frac{qN_a}{\varepsilon_{\rm si}} \left(\frac{(t_{{\rm ox},u})^2}{i\pi} - \frac{(H_{\rm eff} - t_{{\rm ox},u})^2 (-1)^i}{i\pi} + 2H_{\rm eff}^2 \frac{(-1)^i - 1}{(i\pi)^3} \right) \right] \tag{6b}$$

$$c_i' = \frac{1}{\sinh\left(i\pi (W_{\rm eff}/H_{\rm eff})\right)} \left[2 (V_{\rm bg} - V_{\rm fb} - b) \frac{1 - (-1)^i}{i\pi} + 2a \left(\frac{t_{{\rm ox},u}}{i\pi} + \frac{(H_{\rm eff} - t_{{\rm ox},u})(-1)^i}{i\pi} \right) + \frac{qN_a}{\varepsilon_{\rm si}} \left(\frac{(t_{{\rm ox},u})^2}{i\pi} - \frac{(H_{\rm eff} - t_{{\rm ox},u})^2 (-1)^i}{i\pi} + 2H_{\rm eff}^2 \frac{(-1)^i - 1}{(i\pi)^3} \right) \right]. \tag{6c}$$

Similarly, the 3-D solution ϕ_3 can also be obtained and expressed as

$$\phi_3(x,y,z) = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} [e_{m,n} \sinh(k_y y) + e_{m,n}' \times \sinh\left(k_y (L_{\rm eff} - y)\right)] \cdot \sin\left(\frac{m\pi}{W_{\rm eff}} \left(x + \frac{\varepsilon_{\rm si}}{\varepsilon_i} t_{i,b}\right)\right) \times \sin\left(\frac{n\pi}{H_{\rm eff}} (z + t_{{\rm ox},u})\right) \tag{7a}$$

where

$$k_y = \sqrt{\left(\frac{m\pi}{W_{\text{eff}}}\right)^2 + \left(\frac{n\pi}{H_{\text{eff}}}\right)^2} \tag{7b}$$

$$\begin{aligned} e_{m,n} = \frac{1}{\sin(k_y L_{\text{eff}})} \Bigg\{ \Bigg[& (-\phi_{\text{ms}} + V_{\text{DS}} - b)\frac{1-(-1)^m}{m\pi} \\ & + \frac{qN_a}{2\varepsilon_{\text{si}}} \Bigg(-\frac{(W_{\text{eff}} - (\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b})^2 (-1)^m - ((\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b})^2}{m\pi} \\ & + \frac{2W_{\text{eff}}^2((-1)^m - 1)}{(m\pi)^3} \Bigg) \\ & + a\left(\frac{(W_{\text{eff}} - (\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b})(-1)^m + (\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b}}{m\pi}\right) \Bigg] \\ & \times \frac{4(1-(-1)^n)}{n\pi} \\ & + 2c_m \frac{((-1)^n/n\pi)\sinh(m\pi(H_{\text{eff}}/W_{\text{eff}}))}{1+((m/n)(H_{\text{eff}}/W_{\text{eff}}))^2} \\ & - 2c'_m \frac{(1/n\pi)\sinh(m\pi(H_{\text{eff}}/W_{\text{eff}}))}{1+((m/n)(H_{\text{eff}}/W_{\text{eff}}))^2} \Bigg\} \end{aligned} \tag{7c}$$

$$\begin{aligned} e'_{m,n} = \frac{1}{\sin(k_y L_{\text{eff}})} \Bigg\{ \Bigg[& (-\phi_{\text{ms}} - b)\frac{1-(-1)^m}{m\pi} \\ & + \frac{qN_a}{2\varepsilon_{\text{si}}} \Bigg(-\frac{(W_{\text{eff}} - (\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b})^2 (-1)^m - ((\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b})^2}{m\pi} \\ & + \frac{2W_{\text{eff}}^2((-1)^m - 1)}{(m\pi)^3} \Bigg) \\ & + a\left(\frac{(W_{\text{eff}} - (\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b})(-1)^m + (\varepsilon_{\text{si}}/\varepsilon_i)t_{i,b}}{m\pi}\right) \Bigg] \\ & \times \frac{4(1-(-1)^n)}{n\pi} \\ & + 2c_m \frac{((-1)^n/n\pi)\sinh(m\pi(H_{\text{eff}}/W_{\text{eff}}))}{1+((m/n)(H_{\text{eff}}/W_{\text{eff}}))^2} \\ & - 2c'_m \frac{(1/n\pi)\sinh(m\pi(H_{\text{eff}}/W_{\text{eff}}))}{1+((m/n)(H_{\text{eff}}/W_{\text{eff}}))^2} \Bigg\}. \end{aligned} \tag{7d}$$

Our potential solution has been verified by 3-D device simulation [11]. Fig. 2(a) and (b) compares the derived channel potential distribution with device simulation (at $V_{\text{GS}} = -0.2$ V) for heavily doped devices and lightly doped devices, respectively. Note that a smaller equivalent oxide thickness (EOT) is used in the lightly doped case to sustain the electrostatic integrity [3]. Fig. 2(c) compares the potential distribution for lightly doped device at another gate bias ($V_{\text{GS}} = 0$ V). It can be seen that our model shows satisfactory accuracy.

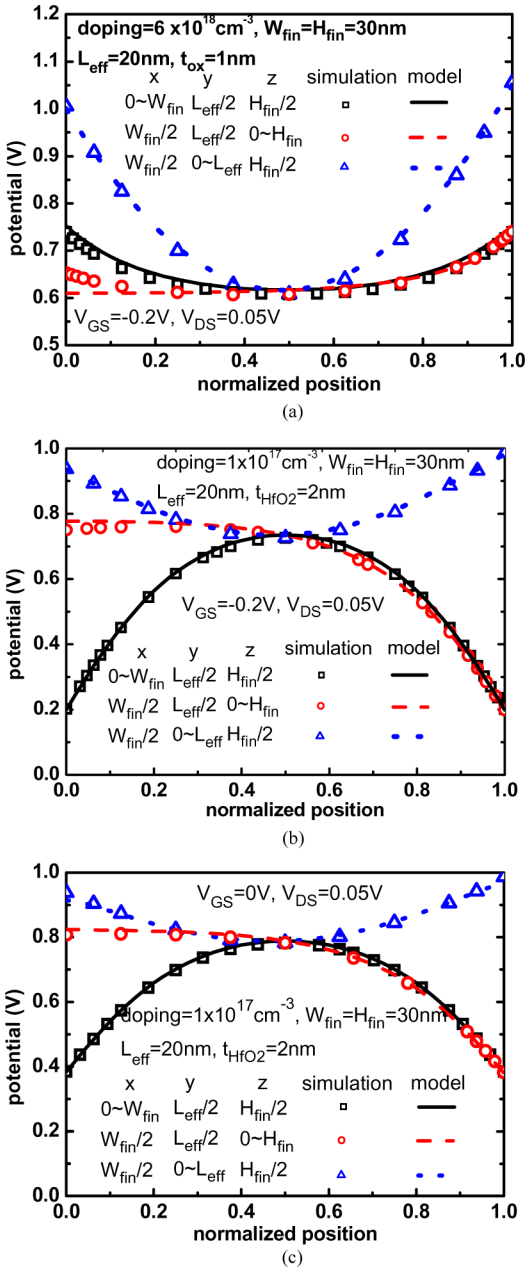

Fig. 2. Analytical potential distribution compared with the result of 3-D device simulation. For the lightly doped case, a midgap work function is used (4.7 eV).

After deriving the channel potential solution, the subthreshold current can be calculated by [7]

$$I_{\text{DS}} = q\mu\frac{n_i^2}{N_a}\frac{kT}{q}\left(1 - e^{-(qV_{\text{DS}}/kT)}\right)\frac{1}{L_{\text{eff}}} \times \int_0^{H_{\text{fin}}}\int_0^{W_{\text{fin}}} e^{q\phi(x,y_{\min},z)/kT}\,dxdz \tag{8}$$

where $\phi(x, y_{\min}, z)$ is the minimum potential (i.e., the highest barrier for carrier flow) along the y (channel length) direction [8]. For devices biased in the linear region, the minimum potential occurs at $y_{\min} = L_{\text{eff}}/2$ due to the nearly symmetrical potential distribution along the channel. We define the V_{th} as the gate voltage at which the calculated subthreshold current $I_{\text{DS}} =$

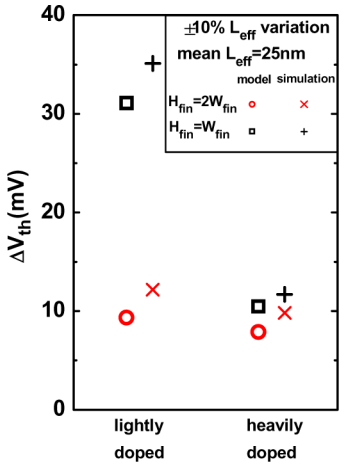

Fig. 3. Comparison of $\Delta V_{\rm th}$ caused by $L_{\rm eff}$ variation between FinFET (AR = 2) and Tri-gate (AR = 1). Both heavily doped and lightly doped channels are considered.

$300\ {\rm nA} \times W_{\rm total}/L_{\rm eff}$ [9], where $W_{\rm total} = 2H_{\rm fin} + W_{\rm fin}$ is the total width of the multigate device.

Compared with the technology computer-aided design (TCAD) device simulation, our methodology shows higher efficiency in determining the $V_{\rm th}$ of a multigate device. For TCAD simulation, the CPU time needed for a single $V_{\rm th}$ is about tens of minutes, while in our calculation, only several seconds is needed. More importantly, this theoretical framework provides more scalable and predictive results than experimental or TCAD simulation does.

III. Sensitivity of Multigate MOSFETs to Process Variations

To assess the sensitivity of multigate devices to process variations, we assume that the device parameters such as channel length ($L_{\rm eff}$), fin width ($W_{\rm fin}$), and doping level vary by $\pm 10\%$, and the corresponding $V_{\rm th}$ variation can be calculated as $\Delta V_{\rm th} = \mid V_{\rm th}(+10\%) - V_{\rm th}(-10\%) \mid /2$ [10]. In addition, the impact of dopant number fluctuation is also crucial to $V_{\rm th}$ variation. In this paper, we assess the $V_{\rm th}$ sensitivity to dopant number fluctuation using our analytical model. We assume that the channel dopant number follows the Poisson distribution [10] and the standard deviation (σ) of the dopant number is ${n_a}^{1/2}$, where n_a is the average dopant number in the Si-body. The $V_{\rm th}$ variation for dopant number fluctuation can be calculated as $\Delta V_{\rm th} = \mid V_{\rm th}(+3\sigma) - V_{\rm th}(-3\sigma) \mid /2$.

To compare the multigate devices with various ARs (AR = $H_{\rm fin}/W_{\rm fin}$), we focus on the FinFET (AR = 2) and Tri-gate (AR = 1) structures. The total width ($W_{\rm total} = 2H_{\rm fin} + W_{\rm fin}$) of FinFET and Tri-gate are both equal to 75 nm to make fair comparison. Devices with various channel doping are considered in this study. For heavily doped devices, the channel doping is equal to $6\times10^{18}\ {\rm cm}^{-3}$. For lightly doped channel, the channel doping is $1\times10^{17}\ {\rm cm}^{-3}$. Besides, gate oxide ($t_{\rm ox}$ = 1 nm) is used for heavily doped devices, while high k dielectric ($t_{\rm HfO_2} = 2$ nm and the dielectric constant of HfO_2 is 25) is used for lightly doped ones to sustain the device electrostatics [3].

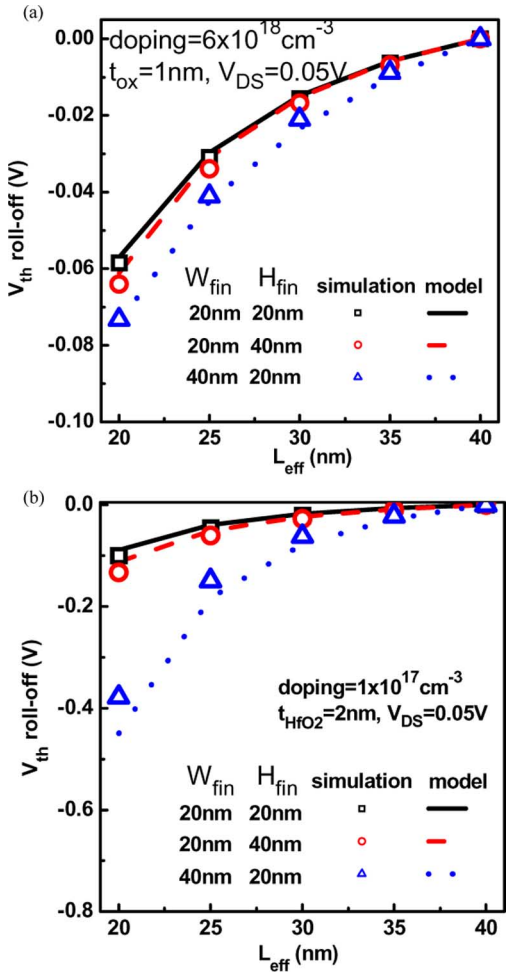

Fig. 4. Impact of $W_{\rm fin}$ scaling and $H_{\rm fin}$ scaling on the $V_{\rm th}$ roll-off behaviors. (a) Heavily doped channel. (b) Lightly doped channel with high k dielectric.

Fig. 3 shows the calculated $\Delta V_{\rm th}$ caused by $L_{\rm eff}$ variation, and the results are verified with device simulation [11]. In both lightly and heavily doped cases, FinFET shows superior $V_{\rm th}$ variation immunity than Tri-gate. Besides, the discrepancy of $\Delta V_{\rm th}$ between FinFET and Tri-gate for lightly doped channel is larger as compared with that of heavily doped channel. The $\Delta V_{\rm th}$ due to $L_{\rm eff}$ variation is determined by the $V_{\rm th}$ roll-off characteristics. Fig. 4 demonstrates that $W_{\rm fin}$ scaling is more effective than $H_{\rm fin}$ scaling in the suppression of $V_{\rm th}$ roll-off, especially for lightly doped case. Therefore, the $V_{\rm th}$ variation for narrower $W_{\rm fin}$ devices like FinFET is smaller. To reduce the $\Delta V_{\rm th}$ caused by $L_{\rm eff}$ (i.e, $V_{\rm th}$ roll-off) in Tri-gate, corner rounding can be used. Fig. 5 demonstrates that the Tri-gate lightly doped devices with corner rounding exhibit improved $V_{\rm th}$ roll-off characteristic.

Fig. 6 shows the calculated $\Delta V_{\rm th}$ caused by $W_{\rm fin}$ variation. It indicates that for heavily doped case, the $\Delta V_{\rm th}$ of FinFET is larger than that of Tri-gate. For lightly doped case, however, the $\Delta V_{\rm th}$ of Tri-gate is significantly larger than that of FinFET. This can be explained by the $W_{\rm fin}$ dependence of $V_{\rm th}$. Fig. 7(a) shows that for heavily doped devices, the $V_{\rm th}$ decreases with $W_{\rm fin}$ because of the reverse narrow width effect. Also shown

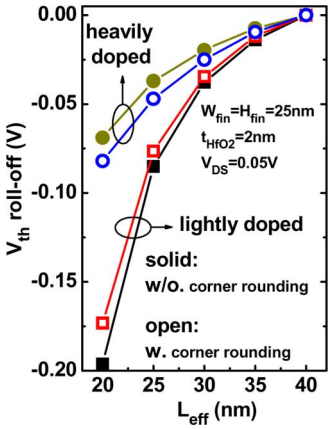

Fig. 5. Impact of corner rounding on the $V_{\rm th}$ roll-off for Tri-gate structure. The results are from TCAD simulation.

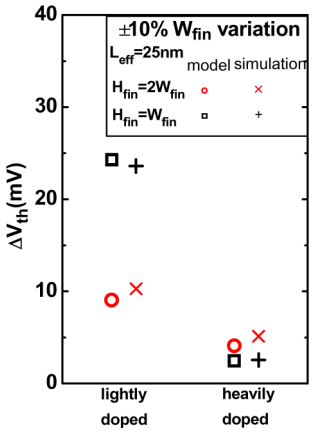

Fig. 6. Comparison of $\Delta V_{\rm th}$ caused by $W_{\rm fin}$ variation between FinFET and Tri-gate.

in Fig. 7(a) is that the $V_{\rm th}$ sensitivity to $W_{\rm fin}$, $|{\rm d}V_{\rm th}/{\rm d}W_{\rm fin}|$, is larger for devices with narrower $W_{\rm fin}$. Therefore, FinFET with its inherently narrower $W_{\rm fin}$ shows larger $\Delta V_{\rm th}$ as $W_{\rm fin}$ varies. Fig. 7(b) shows that for lightly doped devices, the $V_{\rm th}$ increases as $W_{\rm fin}$ decreases because of smaller $V_{\rm th}$ roll-off in narrower devices. Also shown in Fig. 7(b) is that the $V_{\rm th}$ sensitivity to $W_{\rm fin}$ is larger for devices with wider $W_{\rm fin}$. Therefore, Tri-gate with its inherently wider $W_{\rm fin}$ shows larger $\Delta V_{\rm th}$ as $W_{\rm fin}$ varies. It should be noted that in our comparison, the $W_{\rm fin}$ variation ($\Delta W_{\rm fin}$) for FinFET and Tri-gate is not identical ($\pm$1.5 nm for FinFET and $\pm$2.5 nm for Tri-gate). For a given $\Delta W_{\rm fin}$, the discrepancy of $\Delta V_{\rm th}$ between FinFET and Tri-gate in Fig. 6 will become larger for heavily doped case, and the discrepancy will be smaller for lightly doped case.

Fig. 8 shows the calculated $\Delta V_{\rm th}$ caused by doping level variation. The $\Delta V_{\rm th}$ difference between FinFET and Tri-gate is not significant. However, the $V_{\rm th}$ sensitivity to doping level variation in heavily doped devices is much higher than the lightly doped case. It can be seen from Fig. 9 that the $V_{\rm th}$ is sensitive to doping level when the doping concentration is beyond 1×10^{18} cm^{-3}, and remains constant when the channel doping is below $\sim1\times10^{17}$ cm^{-3}.

Besides the doping level variation, dopant number fluctuation is also crucial to the $V_{\rm th}$ dispersion of nanoscale devices.

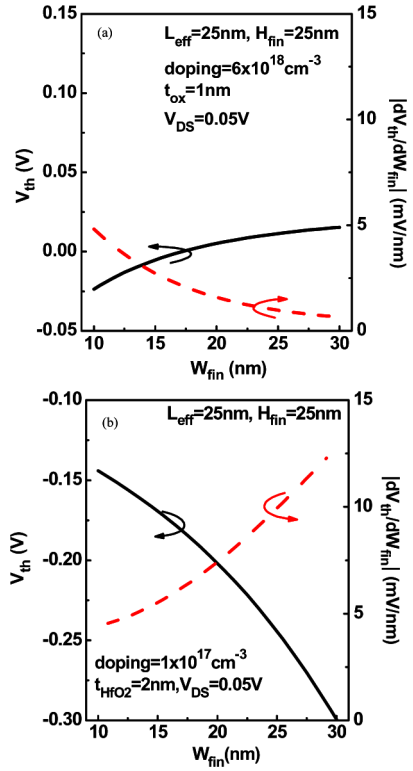

Fig. 7 $W_{\rm fin}$ dependence of $V_{\rm th}$ and $|\,dV_{\rm th}/dW_{\rm fin}\,|$. (a) Heavily doped devices. (b) Lightly doped devices.

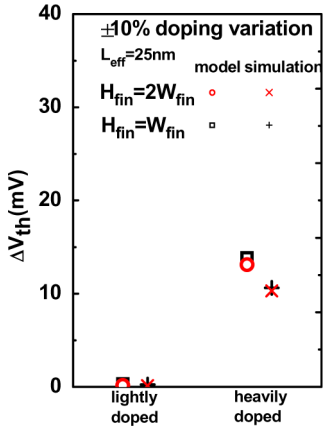

Fig. 8. Comparison of $\Delta V_{\rm th}$ caused by doping level variation between FinFET and Tri-gate.

Fig. 10 shows that for heavily doped channel, the $\Delta V_{\rm th}$ caused by dopant number fluctuation in FinFET is larger than that of Tri-gate. This is because for a given total width, FinFET possesses smaller channel volume than Tri-gate. It is worth noting that the $\Delta V_{\rm th}$ due to dopant number fluctuation is much larger than the $\Delta V_{\rm th}$ caused by $\pm$10% doping level variation. For heavily doped devices, the $\Delta V_{\rm th}$ caused by dopant number fluctuation is the dominant component in the overall $V_{\rm th}$ variations. Our result is consistent with the experimental data in [12]. In [12], for doped channel, the $\sigma V_{\rm th}$ of the devices with smaller volume is larger than that of the devices with larger volume.

It is worth noting that although lightly doped channel has been proposed [13] to suppress the dopant fluctuation, the $V_{\rm th}$

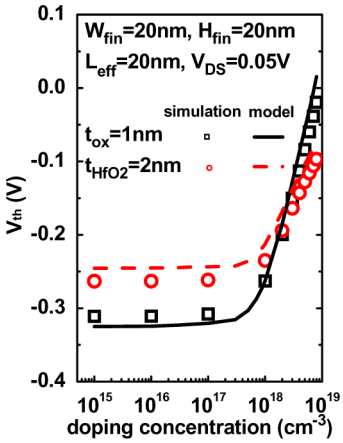

Fig. 9. Doping level dependence of $V_{\rm th}$ in multigate devices.

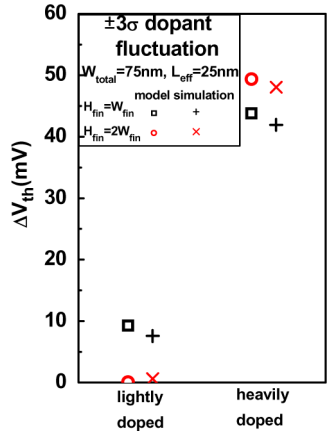

Fig. 10. Comparison of $\Delta V_{\rm th}$ caused by dopant number fluctuation between FinFET and Tri-gate. The $\Delta V_{\rm th}$ is derived from devices with $\pm 3\sigma$ dopant numbers.

dispersion due to geometry variations and dopant position variation [14]–[16] may become concerns for lightly doped devices (especially Tri-gate). Our result is also consistent with [12], which showed that for undoped channel, the devices with larger $W_{\rm fin}$ show larger $\sigma V_{\rm th}$.

IV. Conclusion

We have investigated the sensitivity of multigate MOSFETs to process variations using analytical solutions of 3-D Poisson's equation verified with device simulation. Lightly doped FinFET shows the smallest $V_{\rm th}$ dispersion caused by process variations and dopant number fluctuation. For heavily doped devices, dopant number fluctuation may become the dominant factor in the determination of overall $V_{\rm th}$ variation. The $V_{\rm th}$ dispersion of Tri-gate may therefore be smaller than that of FinFET because of its better immunity to dopant number fluctuation.

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Yu-Sheng Wu was born in Tainan, Taiwan, in 1982. He received the B.S. and M.S. degrees in electronics engineering in 2004 and 2006, respectively, from the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree from the Institude of Electronics.

His current research interests include design and modeling of advanced CMOS devices.

Pin Su (M'05) received the Ph.D. degree from the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, in 2002.

From 1997 to 2003, he was with the Device Group of the University of California, Berkeley. Since 2003, he has been with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he is currently an Associate Professor. He is the author or coauthor of more than 50 papers. His current research interests include silicon-based nanoelectronics, advanced CMOS devices, and device modeling.