行政院國家科學委員會補助專題研究計畫成果報告

總計畫

計畫類別：□ 個別型計畫　　■ 整合型計畫
計畫編號：NSC－90－2215－E－009－111
執行期間：　　90 年　　8 月　　1 日至　　91 年　　7 月　　31 日

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□赴國外出差或研習心得報告一份

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□出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

執行單位：國立交通大學電子研究所

中 華 民 國　　92　年　　1　月　　10　日

子計畫一

互補式金氧半射頻發收機前置電路模組設計IP建立及應用研究(III)

計畫編號：NSC-90-2215-E-009-108

執行日期：90年8月1日起至91年7月31日止

主持人：吳重雨　國立交通大學電子研究所 教授

計畫參與人員：周忠昀、王文傑、康漢彰、陳宗明、蔡俊良

一、摘要

本計畫擬以互補式金氧半製程，設計低電壓以及低功率，適用於工作頻率在幾十億赫茲的射頻前端積體電路。並且，將設計應用在可攜式、多標準發收機，並將電路建為IP；這些積體電路IP核心電路將設計成可工作於各頻率範圍的不同版本，以符合多標準發收機之要求。

本計畫以 TSMC 1P5M 0.25 μm CMOS 設計並實現互補式金氧半射頻前端 IP 核心電路，主要的 IP 核心電路如下所示：(1) 低雜訊放大器(Low Noise Amplifiers)、(2)混波器(Mixers)、(3) 四相位產生器(Quadrature Generators)、(4) 電壓控制振盪器(Voltage Controlled Oscillators)以及(5)功率放大器(Power Amplifiers)。

最後，這些互補式金氧半射頻前端IP電路，將整合並應用於在一單晶多標準射頻前端發收機系統中。

關鍵詞：射頻前端發收機, 低雜訊放大器, 混波器, 四相位產生器, 電壓控制振盪器

Abstract

This project is to design and implement a low-voltage, and low-power CMOS Radio- Frequency (RF) front-end integrated circuits (ICs). This RF Front-end IC will be implemented as an intellectual property (IP) cores which operate in the frequency range of Giga-Hertz, and the specifications of these IP cores will fit the requirements of multi-standard portable RF transceivers.

The CMOS RF front-end IP cores are designed and implemented in TSMC 0.25 μm standard CMOS process. The main IP circuits in this project consist of low noise amplifiers (LNAs), mixers, Quadrature generators, voltage- controlled oscillator (VCOs), and power amplifiers (PAs).

These IP cores circuits are tested and proven, and will finally be integrated and apply for a multi-standards RF transceiver prototype system on a single chip.

KeyWords: RF transceiver, low noise amplifier, mixer, Quadrature generator, voltage- controlled oscillator, power amplifier

子計畫二

液晶監視器影像訊號擷取介面積體電路(III)

計畫編號：NSC-90-2215-E-009-109

執行日期：90年8月1日起至91年7月31日止

主持人：吳錦川　國立交通大學電子研究所 教授

計畫參與人員：蔡淑惠、陳相志

一、摘要

本計畫擬開發一個應用於高速串列數位影像傳輸介面，使用最小轉換差動信號的傳送器和接收器。

整個傳送器電路包含多相位之鎖相迴路，十對一多工器及輸出驅動器。多相位之鎖相迴路的輸入為25MHz~165MHz，提供 10 個相位且輸出頻率同樣為 25~165MHz 的時脈。

接收器部份，其輸入資料傳輸速率範圍為 250 Mbs ~ 1.65 Gbs。而輸入時脈傳輸速率範圍為 25 MHz ~ 165 MHz。整體架構採用三倍頻取樣資料回復演算法。

關鍵詞：傳送器、接收器、鎖相迴路、多工器、驅動器、三倍頻

Abstract

This plan is to develop a transmitter and receiver for a high-speed serial digital display interface

The transmitter consists of a multi-phase phase-locked loop (PLL), a 10-to-1 multiplexer and a data driver. The multi-phase PLL with input frequency range from 25MHz to 165MHz can offer ten-phase clock output that has the same frequency with the input signal.

In receiver part， The range of input data transmission rate is 250 Mbs ~ 1.65 Gbs. And the range of input clock transmission rate is 25 MHz ~ 165MHz。 The overall system is based on three times oversampling data recovery algorithm.

KeyWords: transmitter 、 receiver 、 phase-locked loop (PLL)、multiplexer、 driver、three times oversampling

子計畫三
高速雙絞線網路發收機單晶片系統(III)

計畫編號：NSC-90-2215-E-009-110

執行日期：90年8月1日起至91年7月31日止

主持人：吳介琮　國立交通大學電子研究所 教授

計畫參與人員：徐建昌、周儒明、傅昶綜、蔡乙仲、范啟威、翟芸

一、摘要

本計畫將設計一個數位類比混合式單晶片系統之發收機.此發收機將用於雙絞線 250Mpbs 之資訊傳輸. 調變方式是根據 Gigabit Ethernet 標準訂定的 125Mbaud 符元率 5 階之脈波振幅調變(PAM). 較複雜之發收機功能,

如通道編碼和解碼, 等化, 以及時序還原等, 將使用數位訊號處理之技術. 而類比電路, 如放大器, 數位類比轉化器, 類比數位轉換器, 以及數位相位轉換器等則是處於數位處理器和傳輸介質之間的介面.

關鍵字:數位類比式混合式積體電路,發收機,十億位元乙太網路,單晶片系統

Abstract

This project is to design a mixed-signaltransceiver system on a chip for 250 Mbpsdata transmission over an unshielded twistedpair (UTP) cable. Partially following the Gigabit Ethernet standard, a 5-level baseband pulse amplitude modulation (PAM) with 125 Mbaud symbol rate is assumed. Digital signal processing techniques are used in channelencoding/decoding, equalization, and timing recovery. Analog circuits, such as amplifiers, digital-to-analog converters, analog-to-digital converters, and digital-to-phase converters, provide the interface between the digita processor and the transmission media.

KeyWords: Mixed-Signal Integrated Circuit,Transceiver, Gigabit Ethernet, System on A Chip

目錄

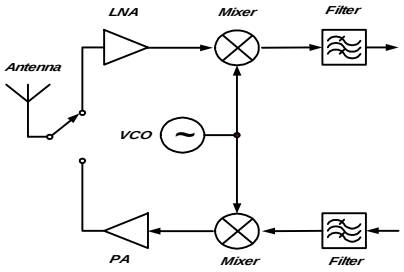
子計畫一之報告內容

前言

近年來，由於無線行動通訊市場的快速成長，帶動了對於低成本以及高性能通訊積體電路晶片的大量需求。過去，高性能的通訊用電路大多使用 Bipolar 的電路，並使用砷化鎵或矽化鍺等較昂貴、整合不易的製程技術來實現；而隨著 CMOS 製程的不斷進步，以及金氧半電晶體效能的提升，電晶體操作頻率（f_T）的提高，再加上 CMOS 的成本低廉，以及對於系統整合度高的優點，使的如何利用 CMOS 來完成並實現整個無線通訊系統於單一晶片，成為了近年來熱門的一個研究領域[1]-[6]。

圖(一)為一個通訊系統所使用的射頻發收機的簡單架構，主要可以分為兩個部分，即接收機（Receiver）以及發射機（Transmitter）。

接收機內部的主要模組電路包含了低雜訊放大器（Low Noise Amplifiers）、降頻混波電路 (Down-conversion Mixers)、以及中頻率波器(IF Filters)。低雜訊放大器將接收到的訊號放大的同時，電路本身的雜訊能不被放大，使電路的輸出端的訊雜比（SNR）提高，如此可以降低系統的雜訊指數（noise figure, NF），由於是在整個接收機的最前端，對整個系統的 sensitivity 影響最大，如何在提供足夠訊號增益時，降低此 LNA 的 NF，為設計 LNA 的重要著眼處。降頻混波器將載波的頻率降低以利後級的率波器做頻道的選擇，為了避免所要訊號頻道在降頻時受到其他的頻道的干擾，降頻混波器的線性度很重要，此外，對於鏡像頻率（image frequency）的雜訊抑制也是降頻混波器設計的重要的考量。



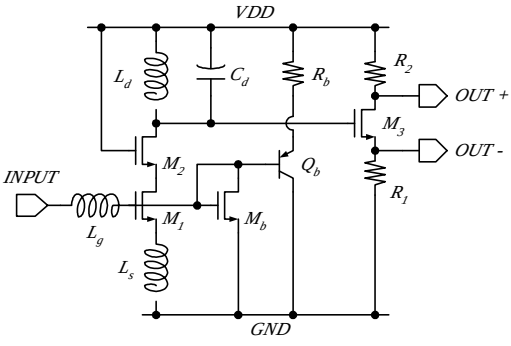
圖一 射頻收發機架構

發射機內部的主要模組電路包含了升頻混波器（即一般所謂的調變器，modulators），以及功率放大器(Power Amplifier)。調變器將由基頻（Base-Band）送來的 I-Q 訊號調變至載波頻率後，經由功率放大器將訊號傳送出。由於目前無線通訊系統的頻帶寬度逐漸變寬，設計一個高線性度的功率放大器，避免訊號間的交互調變（inter-modulation），並且在高線度下能夠提供高的功率效益，已減低功率消耗為設計功率放大器的一個重要考量。要能夠得到一個高性能的通訊系統，射頻前端電路的優劣，將是個非常重要的決定要素。

電路設計

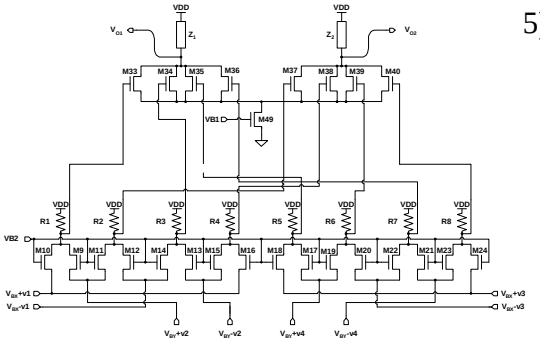
詳細電路架構於子計畫中有仔細說明, 下面僅列出使用到的電路區塊名稱和電路圖

1) 低雜訊放大器（Low Noise Amplifier）



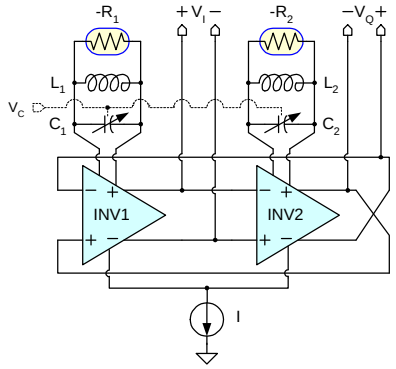
2.4GHz 低雜訊放大器

2) 正交相位調變器（Quadrature Modulator）

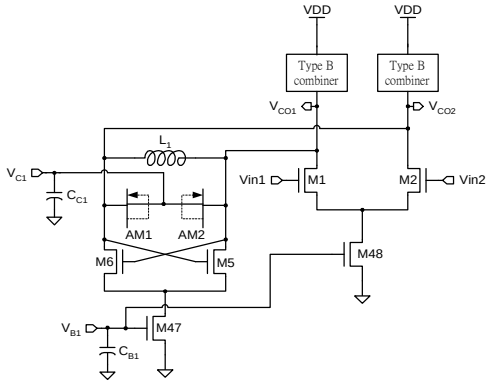


正交相位調變器

3) 電壓控制振盪器與電感電容負載的全差動反相器

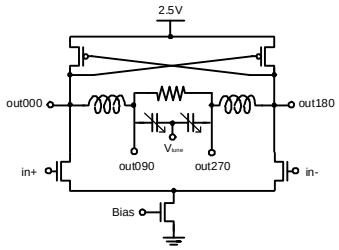


兩級環狀震盪器方塊圖

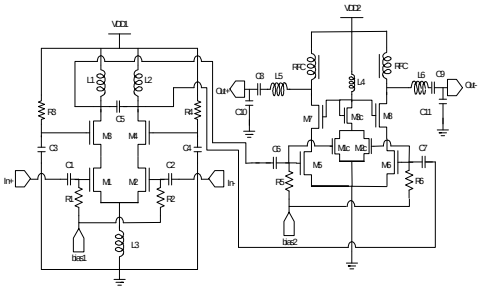


電感電容負載的全差動反相器

4) 四相位產生器（Quadrature generator）



5) 功率放大器



兩級之功率放大器

結論

目前已完成的 IP 有：低雜訊放大器、正交相位調變器、電壓控制振盪器、四相位產生器以及功率放大器。低雜訊放大器具有低雜訊、低功率消耗和高線性度等特性。正交相位調變器使用了電流重覆使用的原理，大幅度的降低功率消耗，在電路的性能上，經過四個 corner 的模擬驗證後，皆能滿足需求。電壓控制振盪器可產生一組相位精確正交的 LO 信號，其可調頻率範圍在 2.65GHz 到 2.15GHz 間，涵蓋 2.4GHz ISM 頻帶。四相位產生器可以涵蓋整個 2.4GHz ISM 頻帶並產生準確的 4 個正交相位的輸出。功率放大器的設計中，一個兩級串接的差動功率放大器被設計達到足夠的輸出功率及優良的效率，具有偶次諧波消除效果及對震盪器信號產生較小干擾的優點。

計畫成果自評

目前已完成射頻前端電路各個 IP 模組的設計以及量測驗證無誤。初步的結果證明這一些 IP 電路可適用於低功率的無線通訊系統中。

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[6] K. C. Tsai, and P. R. Gray, “A 1.9 GHz 1W CMOS Class E Power Amplifier for Wireless Communications,” 24th European Solid-State Circuits Conference, The Hague, Netherlands, Sept. 1998.
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子計畫一之報告內容

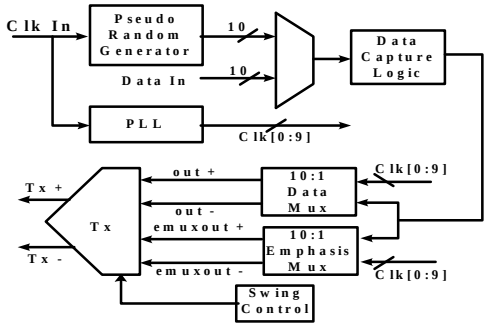
路圖

研究方法與成果

詳細電路架構於子計畫中有仔細說明，下面僅列出使用到的電路區塊名稱和電

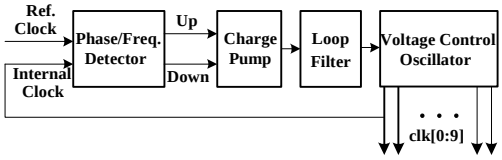
傳送器設計原理與架構

1)傳輸器架構圖



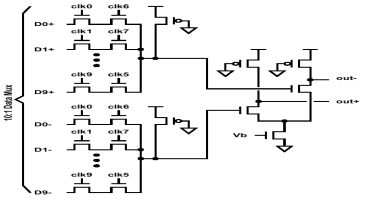
傳輸器基本架構圖

2)鎖相迴路架構圖

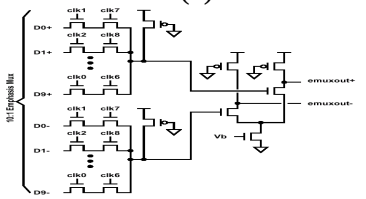


十個相位的鎖相迴路時脈產生器

3) 十對一多工器電路



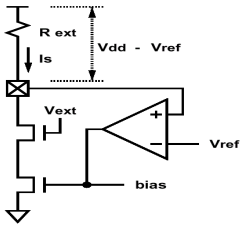
(a)



(b)

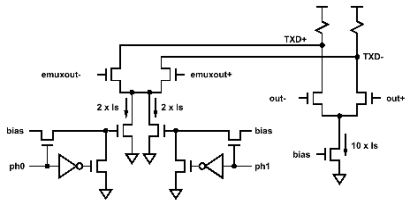
圖三. 十對一多工器電路

4) 輸出振福調整電路



輸出振福調整電路

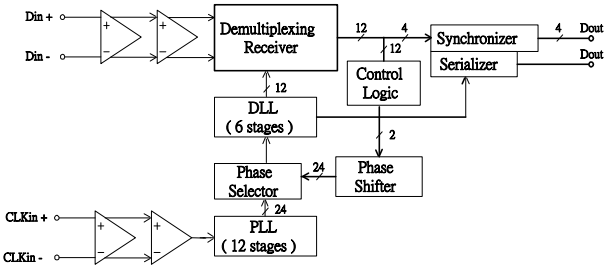
5) 傳輸線驅動器



傳輸線驅動器

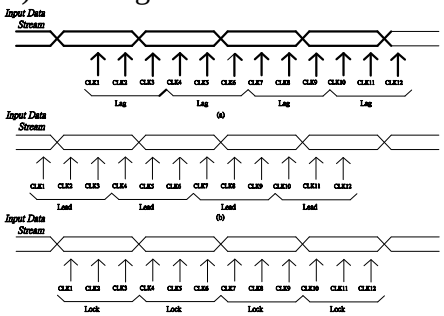
接收器設計原理與架構

1)接收器架構圖



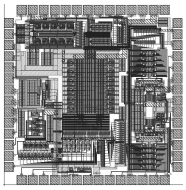
Receiver Block diagram

2) Tracking mechanism

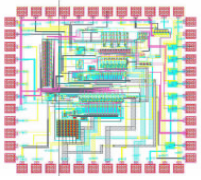


tracking mechanism

晶片佈局



Transmitter Chip Floorplane



Receiver Chip Floorplane

成果計畫自評

本計畫今年是最後一年,而本計畫

也部份完成當初的期望,整個 funtion 是正常,只是可能因為一些小地方因為經驗不足導致沒有辦法達到整個規格的要求,經驗累積起來之後,再做相關的應用電路,應該都不成問題.

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子計畫三之報告內容

Motivation and Objectives

Deep submicron CMOS technologies have Enabled cost-effective multi-million-transistor integrated circuits capable of powerful digital computing. As a results of such advances, high-performance digital communication systems, that employ sophisticated signal processing techniques to overcome transmission media imperfections and various interferences, have become a.ordable to the average consumers and filled the need for ever growing broadband services.

In a modern physical-layer transceiver, although most signal processing functions are performed in the digital domain, analog circuitry is always required for interfacing between the digital functional units and the transmission media. A good design methodology that enable both the analog and digital functional blocks to operate together monolithically is the key to realize a successful transceiver system on a chip (SOC).

This project is investigate the mixedsignal SOC design techniques for implementing a broad-band network transceiver. The transceiver will be designed for high-speed data transmission over an unshielded twisted pair (UTP) cable in the LAN environment following the Gigabit Ethernet standard [1]. In addition, new mixed-signal circuit techniques will be investigated for transceiver functions such as automatic gain control, digital-toanalog converters, analog-to-digital converters, and timing recovery.

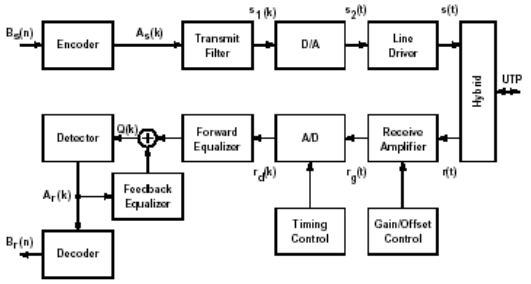

Figure 1: Transceiver block diagram.

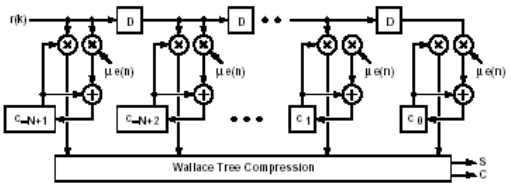

Figure 2: Feedforward equalizer (FFE) filter.

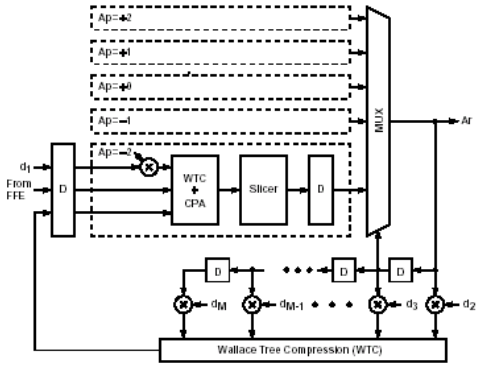

Figure 3: Decision-feedback equalizer (DFE) filter.

Digital Equalizer

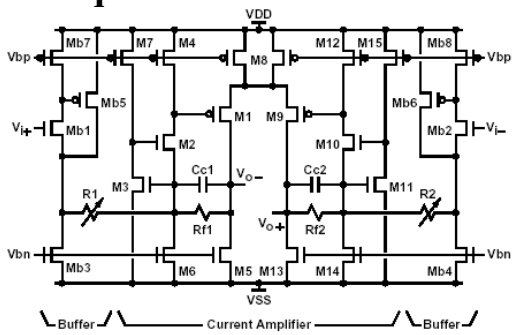

Figure 4: PGA circuit schematic.

Accomplishments

Transceiver Architecture

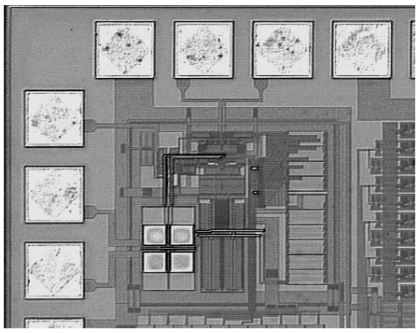

Figure 5: PGA chip microphotograph.

PGA

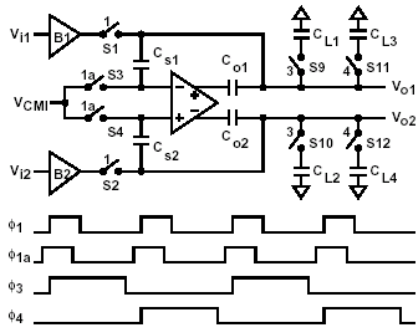

Figure 6: SHA block diagram.

SHA

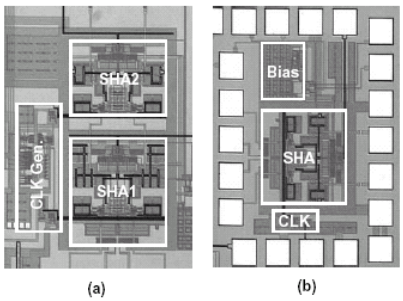

Figure 7: SHA chip microphotograph.

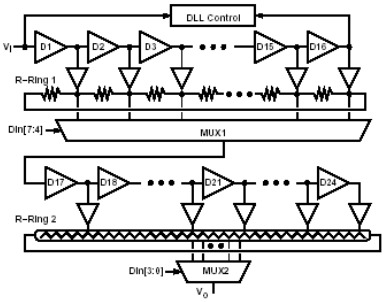

Figure 8: DPC block diagram

DPC

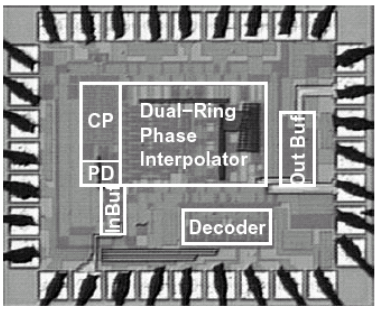

Figure 9: DPC chip photograph.

Conclusions

In this project, we have studied the modern broad-band transceiver architectures, which utilize complex signal processing techniques and multiple adaptive control loops. A C++ mixed-signal simulation platform has been established for full transceiver simulation.

Several key functional blocks have been studied and realized in silicon, which include a fully-digital cell-based 125 MHz adaptive equalizer, a 125 MHz constant bandwidth programmable-gain amplifier with high linearity, a 100 MHz low-distortion sample-andhold amplifier, and a 125 MHz 8-bit digitalto-phase converter. Those functional blocks have specifications better than the original transceiver requirements, and can be used in other high-performance applications such as software radios. A new low-voltage class-AB UTP driver and a new pipelined analog-to-digital converter are still under investigation.

References

[1] “Physical layer specification for 1000 Mb/s operation on four pairs of category 5 or better balanced twisted pair cable (1000BASE-T),” IEEE Draft P802.3ab.

[2] SystemC User’s Guide, Version 1.1 ed.

[3] Z.-M. Lee and J.-T. Wu, “A 125 MHz digital equalizer for high-speed ethernet,” in VLSI Design/CAD Symposium, August 2001.

[4] C.-C. Hsu and J.-T. Wu, “A 125 MHz .86 dB IM3 programmable-gain amlifier,” in Symposium on VLSI Circuits Digest of Technical Papers, June 2002, pp. 32–34.

[5] ——, “A 33-mW 12-bit 100-MHz sample-and-hold amplifier,” in IEEE Asia-Pacific Conference on ASIC, August 2002, pp. 169–172.

[6] K. Bult and A. Buchwald, “An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2,” IEEE J. Solid-State Circuits, vol. 32, no. 12, pp. 1887–1895, December 1997.