以智財單元為基系統晶片設計之測試技術研究
Testing Technology Exploitation for IP-Based SOC Design

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一、中文摘要

本計畫是在“以智財單元為基系統晶片設計之驗證與測試技術開發研究”總計畫項下之一子計畫，目的是研究有關以智財單元為基之系統晶片於深次微米情況下之測試諸問題。本計畫分三年執行，本年度(第二年)之執行計劃摘要如下：

(一)、對於智財單元的耦合障礙測試之研究：

在此一子題中，吾人基於振盪測試技術，對數位電路中的耦合障礙提出一有效之測試架構與方法。相對於傳統測試圖樣產生法，其具有簡單易於實現的特點，並能有效降低產生測試圖樣的複雜度。吾人將本架構與方法應用於許多 benchmark 電路來驗證其有效性。

(二)、對類比智財元件考慮輸出響應的容忍區間之測試圖樣產生法：

在此一子題中，吾人考慮待測電路測試規格的限制，針對線性類比電路的參數型障礙，提出一個方法來找出有效的測試頻率。其先根據測試規格的臨界值來得到待測電路元件參數的容忍區間，並將此元件參數的容忍區間藉由電路模擬對應到量測參數上，在此一對應的過程中，其相互間的關係可能是單調的或非單調的，本研究對於此兩種情況分別提出不同的測試訊號產生法。

(三)、減少類比智財元件的測試規格數目方法之研究：

減少測試規格的數目可以節省測試所需的時間，降低電路測試成本。針對此一子題，本研究提出一個系統化的方法來減少測試所需要的規格數目。其主要是先根據測試規格的臨界值來得到待測電路元件參數的邊界值，然後根據這些邊界條件，對於每一個元件參數找出其最主要的測試規格，最後過濾出不重要的測試規格並加以去除。另一方面，本論文採用統計分析與模擬的方式來考慮實際電路製程的擾動效應，以俾本研究能更接近實際的情況。

(四)、類比鎖相迴路電路之測試與診斷技術之研究：

本子題研究提出一鎖相迴路之可診斷性設計。首先分析鎖相迴路中各組成方塊的障礙特性並建立障礙傳遞的路徑。數位電路部分的障礙將反映在類比觀測點上，同時根據反應之類比障礙行為的差異進行診斷。利用此法，只需在原電路中加入十個控制開關、一個控制訊號及調變輸入訊號即可。

關鍵詞：超大型積體電路測試、智財單元、振盪測試技術、類比電路測試、鎖相迴路診斷、內建式自我測試。

Abstract

This project is one of sub-projects of the

integrated joint project Verification and Testing Technology Exploitation for IP-Based SOC Design. It aims to study issues and problems encountered in testing and verification of the IP-based SOC design in the deep submicron regime. The topics and abstracts of this year are:

(1) Signal induced coupling fault testing for IP interconnection wires:

In this topic, a test scheme for the crosstalk fault based on the oscillation signal is proposed. It uses an oscillation signal applied on an affecting line and detects induced pulses on a victim line if a crosstalk fault exists between these two lines. It is simple and eliminates the complicated timing issue during test generation for the crosstalk fault in the conventional approaches. The test generation and fault simulation based on the scheme are described. Experimental results are also presented to show the described test generation procedure is effective in generating test patterns for this scheme.

(2) Test tolerance on observation signature for analog signal IP circuit testing:

In this topic, an approach to generating the sinusoidal stimulus of the right frequency of a linear analog circuit for testing circuit parameter faults under the constraints of the specifications of the circuit under test (CUT) is presented. This approach considers tolerance bounds due to fabrication process fluctuations of tested parameters using a statistical model and maps them to an accepted region of the observed signature of the CUT. The generated test stimulus is derived based on a proposed testing confidence level. Test generation procedures for both the monotonic and non-monotonic relationships between the signature and the parameter are proposed and demonstrated.

(3) Specification reduction for analog IP testing:

Specification reduction can reduce test time, consequently, test cost. In this topic, a methodology to reduce specifications during specification testing for analog circuits is proposed and demonstrated. It starts with first deriving relationships between specifications and parameter variations of the circuit-under-test (CUT) and then reduces specifications by considering bounds of parameter variations. A statistical approach by taking into account of circuit fabrication process fluctuation is also employed and the result shows that the specification reduction depends on the testing confidence.

(4) Analog PLL IP testing and diagnosis:

In this subject, a design for diagnosis scheme for PLL is presented. The basic idea is to analyze the faulty behavior between each functional block of PLL and create the path for fault propagation. The faulty effect of digital parts are led into analog observational signature, and identified from analog faulty behavior according to different demonstrative characteristics. By this method, several switches which are controlled by one “test” input in conjunction with modulated reference input signal, are added to achieve diagnosis for the scheme. The scheme is simple but efficient.

Keywords: VLSI Testing, IP, Oscillation Ring Test Technique, Analog Circuit Testing, PLL Diagnosis, BIST.

二、緣由與目的

(一)、對於智財單元的耦合障礙測試之研究：

此問題之發生是因一深次微米SOC晶圓線路中，兩信號線上的訊號同時轉態，因近距離電容的藕合效應下，將會導致藕合障礙的發生。障礙發生後可能又會因為電路結構問題，而放大此效應。當此延遲時間超越了系統時脈的週期時間，就會導致邏輯值出錯，發生系統錯誤。吾人考慮對此問題以振盪測試方法，來測試此種延遲障礙。其優點是此方法可以很容易地使用內建自我測試(BIST)架構實現，非常適合於高複雜度系統晶片中的智財元件，且其

是是屬 at speed 測試，能更實際地測試出電路的真實行為。

(二)、對類比智財元件考慮輸出響應的容忍區間之測試圖樣產生法：

於數位電路中，電路發生障礙時，在適當的輸入測試圖樣下，其輸出所顯現障礙效應皆是很清楚可分辨的"0"或"1"信號。但於類比電路中，線路之信號為連續性，當電路發生巨變型障礙時，電路常發生不正常運作，一般皆很容易藉由觀察電路之輸出而決定此電路之正常與否；但當電路發生參數型障礙時，電路輸出可能有某種程度之變動，但此時並不是太容易直接由輸出響應上明確地斷定此電路是否有障礙發生。對於「障礙」、「規格」、「輸出響應」中間有一些複雜但卻緊密的關連。吾人對此一問題，提出一系統化方法，將之釐清，進而對任一類比智財元件，清楚的定義出輸出響應的好壞邊界。

(三)、減少類比智財元件的測試規格數目方法之研究：

一般而言，類比電路的測試是驗證其效能是否能符合所有規格的規範，而不是嘗試著去測試所有的障礙。然而相較於數位電路，一方面因測試類比電路之測試機台非常昂貴；另一方面因其測試規格數目眾多，測試時間冗長，造成測試成本居高不下。因此，若要減少測試成本主要的方法是減少其必需測試的規格的數目。本子題所要探討的問題為，在考慮製程的統計資料下，針對類比智財單元求得其最少的必須測試規格，如此可用最少的測試時間而仍然能夠維持很高的障礙涵蓋率。

(四)、類比鎖相迴路電路之測試與診斷技術之研究：

鎖相迴路是由相位檢測器、充放電線路與迴路濾波器、電壓控制振盪器所組成，因為鎖相迴路及其中的電壓控制振盪器的電路架構具有迴授迴路，使得障礙發生時不易偵測，因此測試或偵錯上產生許多困難點。以往在鎖相迴路的測試與偵錯上僅有少數針對其障礙模型或針對其組成電路之測試方法的研究報告。對此一子題，吾人從分析電路的特性著手，找出可資利用的參數作為偵錯時的判斷特徵，考量一可測性設計方案對鎖相迴路各部分電路不同的特點，產生不同測試圖樣，將各電路的障礙所反應於鎖相迴路上的效應凸顯，以達到障礙偵錯的目的。

三、結果與討論

(1) Signal induced coupling fault testing for IP interconnection wires:

In this work, we propose a test scheme to test crosstalk faults. It uses an oscillation signal applied on an affecting line and detects induced pulses on a victim line if a crosstalk fault exists between these two lines. It is simple and eliminates the complicated timing issue during test generation for the crosstalk fault. The scheme is very simple and easy to be implemented. Two test generation approaches, i.e., the guided random test generation and the deterministic test generation are described and experimental results are presented. The experimental results show that the proposed test generation approach, i.e., it first uses the guided random test generation then a deterministic approach can effectively generate crosstalk fault test patterns for circuits. Some results of this work have been presented in ATS'2002 [1].

(2) Test tolerance on observation signature for analog signal IP circuit testing:

In this topic, we have presented a structure-based specification-constrained test generation method which starts with derivation of the relationship between the specifications and the device and/or component parameters, and it then considers variations of component parameters due to fabrication process fluctuation by using a statistical model. The relationship between the observed signature and the parameter may be monotonic or non-monotonic. A criterion that combines signature sensitivity and input-output transfer factor is used to generate test patterns for monotonic type

parameters. For non-monotonic type parameters, test generation with the aim of reducing the degree of misclassification has also been proposed. Simultaneously, a tolerance range that corresponds to the limitations imposed by the specifications is obtained. An example circuit has been used to demonstrate the test generation procedure and to show the effectiveness of the generated test frequency in increasing the observability and reducing the degree of misclassification. Besides, we have written several papers based on this work [2, 3].

(3) Specification reduction for analog IP testing:

In this topic, we have presented an approach to reduce the number of test specifications for analog circuits. It starts with derivation of the relationship between specifications and device and/or component parameters then defines upper and lower bounds for parameters to find essential test specifications. Then the variations on component parameters due to fabrication process fluctuations are considered by using a statistical model to reduce test specifications with a testing confidence probability. A continuous time state-variable filter example circuit has been used to demonstrate the specification reduction procedure and it has been shown that 2, 3 or 4 out of 10 specifications can be ignored during specification testing under the 99%, 90% and 50% testing confidence level respectively. The procedure is effective and can be used in manufacturing specification test for analog circuits to reduce test time. Besides, several papers based on this research work have been presented [4, 5].

(4) Analog PLL IP testing and diagnosis:

In this topic, we have presented a design for diagnosis scheme which make the PLL output a periodic signal through the use of some extra circuit. This enhances the conveniences to observe signals under test. In addition, the design for the PLL diagnosis proposed is simple but efficient in identifying representative faults for the PLL during the manufacturing stage when the PLL does not oscillate or meet the performance specifications. Some results of this work have been presented in IMSTW [6].

四、計畫成果自評

本計畫於第一年已建立智財單元本身與相互間連線的測試機制，在本執行年度(第二年)的期間也順利地分別對數位、類比與混合訊號電智財單元提出有效的測試與診斷的架構與方法，相信將有助於後續計劃之執行。大部分的研究成果皆符合吾人原提計劃，完成度應達 90%以上，且部分成果已發表於國際之期刊[1-6]或博、碩士論文中[7-9]。

五、參考文獻

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