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CMOS hot carrier luminescence imaging and advanced gate dielectrics

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CMOS 激光顯像與閘極介電層材料

摘要

在 CMOS 發光顯像方面，吾人發現元件在動態臨界電壓場效電晶體(DTMOS)操作模式下會有增強熱載子退化，而此現象無法用傳統熱載子理論解釋。因此吾人提出一歐傑再結合(Auger recombination)增強電子能量機制。吾人利用熱載子激光與熱載子閘極電流入射實驗來證明通道中電子能量因正偏基極引發電動入射產生歐傑再結合效應而增加。根據研究結果顯示，在此操作模式下汲極電流與汲極雜訊(noise)退化較傳統熱載子操作下更嚴重。不同於傳統熱載子所造成的元件退化，歐傑再結合所造成元件退化和溫度成正相關，因此對於在高溫操作的先進元件會有更嚴重的可靠性問題。同時吾人也觀察在超薄氧化層元件中因價帶電子穿隧(valence-band electron tunneling)所引發的歐傑再結合增強熱載子退化，此增強退化現象和基極電壓成正相關，因此對於 SOI 和 DTMOS 元件將會造成嚴重的可靠性問題。

另一方面來說，吾人將利用歐傑再結合增強電子能量機制發展出一套新式快閃式記憶體寫入方法。根據相關理論,歐傑再結合效應所強化之閘極入射電流與溫度成正相關，因此此方法適用於高溫操作。同時由於通道電子擁有較高的能量，此方法將可適用於低電壓操作。

在先進閘極介電材料方面，藉由使用電子迴旋共振化學氣相沈積（ECR-CVD）法，吾人成功的在 Si 介面上長成一厚度範圍在 1.8nm-3.5nm 的 silicon oxynitride 薄膜。在成長完成後，為增進薄膜的品質，吾人會將薄膜置放於 N_2O 的氣體中並施以 950°C，60 秒的高溫退火(anneal)動作。以等效氧化層厚度為 1.8nm 的薄膜為例，在量測電壓範圍為 1-1.5V 時，其所產生漏電流約為同厚度之氧化層的二十分之一。吾人除了以 C-V 方法進行分析外，也將會利用 *X*-ray photoelectron spectroscopy (XPS)來了解薄膜的鍵結狀況並進一步驗證所成長的薄膜厚度。

CMOS hot carrier luminescence imaging and advanced gate dielectrics

Abstract

In the section of CMOS hot carrier luminescence imaging, enhanced hot carrier degradation in DTMOS-like operation mode is observed. This degradation is attributed to Auger recombination assisted hot electron energy gain process. In this process, holes created by positive bulk to source bias (V_{bs}) provide for Auger recombination with electrons in the channel, thus substantially increasing the hot electron energy. Measured hot electron gate current and light emission spectrums in nMOSFET provide evidence that the high-energy tail of channel electrons is increased by the application of a positive substrate bias. Two-dimensional device simulations are also performed to evaluate the Auger recombination rate along the channel. To further demonstrate the Auger effect on device reliability, the drain current and flicker noise degradation are measured. The drain current and flicker noise degradations are about ten times more serious in the DTMOS than in the conventional MOSFET. Consistently with this picture, the Auger enhanced degradation, as opposed to the convention hot carrier degradation, exhibits positive temperature dependence, and the critical substrate voltage that triggers this additional energy gain process (i.e. Auger effect) even becomes smaller as temperature is raised. Therefore, this phenomenon may cause a severe reliability issue in positively biased substrate devices and is more significant at low drain bias. Besides, Auger recombination enhanced hot carrier degradation with stress V_g in the valence-band tunneling regime is also observed. Our result shows that the valence-band tunneling enhanced degradation, as opposed to maximum Ib stress induced degradation, exhibits positive dependence on substrate bias.

Moreover, a hot electron programming method by taking advantage of Auger recombination is proposed. Faster programming rate and higher electron injection

efficiency than conventional channel hot electron programming (CHE) are obtained. In contrast to CHE, this technique shows excellent temperature stability from T=25C to T=125C.

In advanced gate dielectrics parts, ultra-thin silicon oxynitride films with thickness in the range of 1.8-3.5 nm have been produced on Si (100) by nitridation of an NO-oxidized surface with an electron-cyclotron resonance plasma source. The films were annealed in N_2O at 950 °C for times up to 60 s and formed into Al-gated capacitors for capacitance-voltage (CV) and current-voltage analysis. The rapid annealing increases the oxygen content of the films but results in capacitors with excellent electrical properties. For a plasma oxynitride with equivalent oxide thickness, t_{eq} = 1.8 nm, current reductions of ~20 over that for SiO_2 films have been obtained for gate voltages in the range 1-1.5V. For comparison, the thickness of the oxynitrides was obtained by *X*-ray photoelectron spectroscopy (XPS) of the Si-2p, N-1s and O-1s photoelectrons. By analyzing the yield from thick silicon dioxide and silicon nitride films, the electron escape depth in silicon nitride was estimated to be 1.7 nm for the Si-2p electrons. By correcting the measurements of the oxygen/nitrogen concentration ratio obtained from the O-1s and N-1s XPS peaks, and calculating the dielectric constant with a Bruggeman effective medium approximation, the equivalent oxide thickness was calculated. Agreement to ~0.2 nm was obtained with t_{eq} determined by the CV analysis. Information obtained from the XPS analysis can also give information about bonding configurations and possible errors due to non-uniform stoichiometry as a function of depth.

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Table Captions

Table1:

Full width at half maximum (FWHM) and binding energy (BE) of the N-1s XPS peak for plasma-deposited silicon oxynitride films after various process steps during formation and after annealing at 950 ºC in N_2O.

Chapter 1 Introduction

The supply voltage for ULSI circuits will have to be reduced as channel length decreases due to hot electron reliability limitations. In contradiction to predictions based on the simple lucky carrier concept [1], non-negligible hot carrier degradation has been observed in MOS devices even at a drain bias below the threshold for interface state generation (W_{it} ~ 3.7eV) [2-6]. There are several possible mechanisms for low-voltage hot carrier degradation. For example, by using Monte Carlo or other simulation techniques to nMOSFET's, it has been predicted that at the drain voltage below 3V, electrons heated by electron-electron (e-e) scattering should dominate the high-energy tail of the electron energy distribution function above W_{it} [7,8]. Moreover, Monte Carlo simulations and theoretical considerations suggest that the electron-phonon interaction at high energies in the silicon conduction band can lead to a quantum-mechanical collisional broadening which results in a dispersion of the electron energy levels [9]. Recently, Auger recombination has also been proposed to be a major mechanism for supplying the additional required energy for hot electron degradation at a low applied voltage [10], [11]. This process involves electron and hole recombination, transferring their energy to another electron. Thus, the high-energy tail of channel electrons is increased.

Recently, the feasibility of applying a positive substrate bias in nMOSFET's to achieve better performance has received extensive attention in certain analog and digital circuits. For example, enhanced low-power analog performance can be achieved by applying a positive substrate bias that enables reduced short channel effects [12]. Less threshold voltage roll off suggests that a better device matching property can be obtained. *Hsu* et al. demonstrated that buried-channel (B.C.) MOSFET's operated in DTMOS-like operation mode (V_{gs}=V_{bs}) is more appropriate for low-noise analog applications [13]. In addition, a DTMOS that is suitable for low voltage ULSI circuits was proposed [14,15]. The on-state threshold voltage in this structure is reduced by forward biasing the substrate,

resulting in a significantly higher I_{on}/I_{off} ratio than the conventional MOSFET's as shown in Fig.1.1. The applied substrate bias here is sometimes as large as 0.7V [16] or even larger [17,18]. However, the reliability issue of MOSFET's in such a bias condition has seldom been studied. In this work, we report a new hot carrier degradation mode in DTMOS operation. The observed degradation cannot be simply explained by conventional channel hot electron theory. Instead, an Auger recombination assisted hot electron energy gain process is proposed. The hot electron gate injection current and light emission spectrum, which reflects the high-energy tail of the channel electrons have been measured to support our model. The temperature and the substrate bias dependencies of the Auger effect in DTMOS operation are characterized. The Auger enhanced degradation exhibits positive temperature dependence and may become a serious reliability problem at a high temperature. Besides, enhanced hot carrier degradation with stress V_g in the valence-band tunneling regime is observed in ultra-thin gate oxide MOSFET's. This degradation is attributed to channel hole creation by valence-band electron tunneling. The created holes provide for Auger recombination with electrons in the channel and thus increase hot electron energy. In ultra-thin gate oxide nMOSFETs, our result shows that the valence-band tunneling enhanced degradation, as opposed to maximum I_b stress induced degradation, exhibits positive dependence on substrate bias. This phenomenon may cause a severe reliability issue in floating substrate or positively biased substrate devices. On the other hand, by taking advantage of the Auger recombination assisted hot electron energy gain process, a new HE programming technique is proposed for flash EEPROM operation. The proposed method provides a faster programming rate and higher electron injection efficiency than the conventional hot electron programming. This technique also shows excellent temperature stability from T=25C to T=125C. This method is promising in low voltage and high temperature operation.

Except the hot carrier reliability issues, intrinsic gate leakage current is also an incoming problem. Silicon nitride and oxynitrides are being evaluated as replacements for silicon dioxide in the gates of aggressively scaled CMOS devices. Although boron penetration and hot-electron stress effects can potentially be reduced by mono-layer quantities of nitrogen, larger nitrogen concentrations result in a higher dielectric constant, allowing for reduction of the direct tunneling currents. Treatment of the Si (100) surface with a nitrogen plasma results in the formation of a defective silicon nitride layer. In order to reduce defects in gate-quality oxynitrides, they are often annealed in nitrous oxide [19] after formation, and this results in an increase in the oxygen content of the films. Previous work has focused on measuring the redistribution of nitrogen at the interface between Si (100) and silicon dioxide films during N_2O annealing [20], or the effect of long (up to 30 min) oxidations of silicon nitride films in N_2O [21]. The amount of nitrogen left in ultra-thin oxynitride films after rapid thermal oxidation in N_2O has not been the subject of much comment by those who measure equivalent oxide thickness using capacitance measurements.

A major reason for this is the difficulty of determining the nitrogen profile of ultra-thin films since ion-beam techniques such as medium-energy ion scattering [20], or narrow resonance nuclear reaction analysis [22] are not readily available for routine analysis, while other methods such as secondary-ion mass-spectrometry [23] have reached their resolution limits. A simple and generally available technique such as *X*-ray photoelectron spectroscopy (XPS) can give useful information such as the film thickness and the oxygen/nitrogen concentration ratio and can provide a measure of the non-uniformity with depth.

A recent review discusses much of the literature describing the XPS analysis of ultra-thin silicon dioxide films [24]. It highlights the sensitivity of ellipsometry measurements to surface contamination, in contrast to the XPS technique that involves a ratio of two peak areas equally attenuated by contaminants. XPS measurements on SiO_2

films have also been carefully calibrated against other techniques such as transmission electron microscopy and capacitance-voltage (CV) measurements [25]. Previous work was facilitated by the relative simplicity of growing a number of stoichiometric silicon dioxide films with thickness in the range of interest. For silicon nitride films the calibration is more difficult since it cannot generally be assumed that nitrogen concentration does not change with film thickness.

In this paper the equivalent oxide thickness of plasma-nitrided films annealed in N_2O at 950 ºC was determined by capacitance-voltage (CV) measurements, and the quality of these films was determined by CV and current-voltage (IV) measurements. The thickness of N_2O-annealed oxynitride films produced by plasma nitridation and by low-pressure chemical-vapour deposition (LPCVD) was determined by analysis of the Si-2p (substrate) and Si-2p (bonded) XPS lines and their composition was determined by analysis of the N-1s and O-1s lines. The electron escape depth of Si-2p electrons from silicon nitride was determined by comparing the yields in thick silicon nitride and silicon dioxide standards. The XPS measurements, coupled with interpolations from the silicon dioxide and silicon nitride standards, were used to self-consistently recalculate the thickness. The dielectric constant determined from a Bruggeman effective medium approximation [26] using the oxygen/nitrogen ratio was then used to calculate the equivalent oxide thickness for comparison with the CV measurements. Finally, estimates are made of potential errors in the XPS analysis introduced by assuming that the films have uniform composition with depth.

In this study, Chapter 2 contains a brief description of device characterization and Auger recombination assisted hot electron energy gain process. The measured hot electron gate current and the photon luminescence spectrum are also shown in this Chapter. These measurements confirm that the increase of the high-energy tail of channel electrons results from the DTMOS operation mode. In addition, the device simulation results of the Auger recombination rate in the channel are shown here to give further

evidence that Auger effect is significantly enhanced under such a bias condition. In Chapter 3, Auger recombination enhanced device degradation in DTMOS operation mode is measured. The temperature and bias effects on the Auger enhanced degradation are also analyzed. In Chapter 4, valence-band tunneling enhanced hot carrier degradation in ultra-thin oxide nMOSFET's is observed. This phenomenon is also attributed to Auger recombination effect. The substrate bias dependence of valence-band tunneling enhanced hot carrier degradation is examined. Moreover, we demonstrate a new hot electron programming technique by taking advantage of Auger recombination enhanced gate injection current in flash EEPROM in Chapter 5. Improved hot electron injection efficiency and temperature stability can been obtained. The fabrication process flow and characterization method for advanced gate dielectrics will be described in Chapter 6. In Chapter 7, the characteristics of fabricated ultra-thin gate dielectrics will be shown. The thickness of the dielectrics has been verified by C-V method and XPS analysis. Furthermore, the bonding configurations are also analyzed by XPS method. The conclusions drawn from this work were embodied in Chapter 8.

Chapter 2 Evidence of Auger Recombination Assisted Hot Electron Energy Gain Process

2.1 Device Characterization Method

A four-terminal nMOSFET was used with a gate width of 100μm and a gate length of 0.25μm. The device has a gate oxide thickness about 50Å. Maximum I_b stress around V_g=0.5V_d was performed in DTMOS-like mode (V_b>0) and in the standard mode (V_b=0). Drain current in the triode region was measured to monitor drain current degradation. Temperature and drain bias dependence of the Auger enhanced degradation was also characterized. Hot carrier luminescence measurement was performed with single photon counting system that allowed for spectral analysis in the range 1.2eV-2.9eV [27]. Photons emitted from a MOSFET are detected by a photon counting camera through the optical microscope. The photon numbers at each wavelength are counted individually using band pass filters. The measured data are then corrected for the energy dependence of the filter transmittance. During the luminescence measurement, drain current was monitored to check the possible presence of aging, which was found to be negligible.

2.2 Auger Recombination Assisted Hot Electron Energy Gain Process

It has been reported that Auger recombination can enhance hot electron tail and cause more serious degradation in MOSFETs [11], [28], [29]. The process for Auger recombination in various device operation conditions is illustrated in Fig.2.1. In Fig.2.1 (a), a small part of holes created by impact ionization may flow to the region near the source (where electron concentration is high) [30] and provide for Auger recombination. In Fig.2.1 (b), a positive substrate bias is applied and the channel hole concentration and thus Auger recombination rate are increased due to substrate hole injection [29]. In ultra-thin oxide nMOSFETs, a positive gate bias can cause valence-band electron tunneling to

the gate and leave holes behind in the channel (Fig.2.1 (c)). In the following, we will first investigate the significance of positive substrate bias injected holes to device reliability.

Fig.2.2 illustrates the electron energy gain process in conventional hot carrier stress and in DTMOS hot carrier stress, respectively. In conventional hot carrier stress, the electron energy gain mechanism is field heating near the drain junction as shown in Fig.2.2 (a). In DTMOS hot carrier stress, i.e., with a positive substrate bias applied, holes are injected from the positively biased substrate to the channel as shown in Fig.2.2 (b). The injected holes can provide for recombination with electrons in the channel and give excess energy to other channel electrons as shown in Fig.2.3 (a). This is the Auger recombination process and also a major energy gain process in DTMOS operation. The energetic electrons arising from the Auger process are then accelerated by a channel electric field, thus resulting in a larger hot electron tail than in the standard MOSFET's operation condition as shown in Fig.2.3 (b).

2.3 Hot Electron Light Emission Measurement

As we know, the hot electron luminescence and the light emission in nMOSFET's can reflect the electron energy distribution [31], [32]. Fig.2.4 (a) and Fig.2.4 (b) are the micrographs of the hot electron light emission from nMOSFET's with L_g=0.25μm and W_g=100μm. Bias conditions are: V_{ds}=2.9V, V_{gs}=1.5V, V_{bs}=0V and V_{ds}=2.9V, V_{gs}=1.5V, V_{bs}=0.7V, respectively. The bandwidth of the band pass filter is 800Å. Square block regions are aluminum pad with 100μm by 100μm for electrical contacts. The total exposure time is 100 seconds. Note that the light intensity is relatively stronger as the positive substrate bias is applied. Fig.2.5 shows the light intensity and the substrate current as a function of the gate voltage with different substrate biases. It should be mentioned that the substrate current arising from impact ionization near the drain junction strongly depends on channel field and so does the hot electron light emission. Therefore, the hot electron light emission correlates well to the substrate current in the conventional

hot carrier stress. However, the substrate current in the DTMOS hot carrier stress condition is more complex due to an additional current path from the substrate to the channel. Therefore, the light emission provides a reliable monitor for hot electron energy in MOSFET's, which can be used as an alternative monitor to the substrate current.

The hot electron light emission spectrum is measured to analyze the hot electron distribution, as illustrated in Fig.2.6 In this figure, the y-axis represents the normalized light intensity and the x-axis represents the photon energy. The light intensity is normalized to the drain current to compensate for the different carrier flux in the channel. As the substrate bias increases from 0V to 0.5V, the hot electron actually decreases due to a smaller electric field. As the substrate bias continues to increase to 0.8V, the hot electron tail is significantly enhanced by an order of magnitude.

2.4 Hot Electron Gate Current

Another evidence is the hot electron gate injection current. Since hot electron gate inction current, I_g, is a sensitive measure of the high-energy tail of the hot carrier distribution [33]. Fig.2.7 demonstrates the normalized hot electron gate injection current as a function of gate bias with different substrate biases. The drain bias is fixed at 3.5V and the substrate bias is increased from 0V to 0.8V. Again, the gate injection current first decreases and then increases with the substrate bias. In Fig.2.8, we measure the hot electron gate current at different drain biases. From the above two figures, the hot electron gate current depends on both drain bias and substrate bias. The drain bias determines the field heating and the substrate bias determines the Auger effect. The dependence on both the drain bias and the substrate bias confirms that the electron energy gain process in DTMOS operation consists of Auger recombination and field acceleration.

2.5 Two-Dimensional Device Simulation Results

Figure 2.9 shows the two-dimensional device simulation results of the Auger recombination rate and electric field in the channel. In this figure, the *x*-axis is the distance from the source junction. The open symbol represents the result with a substrate bias of 0.5V and the full symbol represents a substrate bias of 0.8V. Note that the electric field slightly decreases as the substrate voltage increases from 0.5V to 0.8V due to body effect, whereas the Auger recombination rate increases by several orders of magnitude due to the exponential dependence of hole injection. Notably, hole injection is restricted to the low field region near the source. Therefore, the energetic electrons arising from the Auger recombination are then accelerated by a lateral electric field, thus leading to a large hot electron tail, and so do the hot electron light emission and the gate injection current.

Chapter 3 Device Degradation Enhanced by Auger Recombination

Experimental evidence of the Auger recombination enhanced hot electron tail is shown in the above Chapter. In the following, device performance degradations due to the Auger recombination effect are discussed. The measured result includes on-state drain current degradation, off state drain leakage current degradation and flicker noise degradation.

3.1 On-State Drain Current Degradation

To demonstrate the Auger effect on device reliability, the linear drain current degradation at different substrate biases is measured in the Fig.3.1. Stress drain bias is 2.9V and gate bias is 1.5V. The device has a gate length of 0.25μm. The drain current degradation is increased by an order of magnitude when the substrate bias increases from 0V to 0.8V. The gate length dependence of Auger enhanced degradation is examined in Fig.3.2. The enhanced degradation is still remarkable as the gate length is down to 0.13μm.

3.2 Off-State Drain Leakage Current Degradation

Figure 3.3 shows the off-state drain leakage current degradation by the conventional hot carrier stress and by the DTMOS hot carrier stress. The dashed line represents the conventional hot carrier stress and the dotted line is the DTMOS hot carrier stress. At a medium drain bias, the drain leakage current degradation is primarily caused by interface trap creation. Fig.3.4 shows the drain leakage current enhancement by the two stresses. Apparently, the drain leakage degradation by the DTMOS hot carrier stress is more serious. Fig.3.5 shows the on-state drain current (I_{on}) measured at V_{gs}=2V and

V_{ds}=0.1V versus the off-state drain leakage current (I_{off}) measured at V_{gs}=0V and V_{ds}=1.5V with different stress substrate biases. Note that the I_{on}/I_{off} characteristics in the L_g=0.13μm device after DTMOS hot carrier stress is worse than that of the L_g=0.2μm device. This means that short gate length nMOSFET's operated in the DTMOS operation mode has a severe reliability problem.

3.3 Flicker Noise Degradation

With respect to analog devices, we compare the flicker noise degradation by the conventional hot carrier stress and by the DTMOS hot carrier stress. As shown in Fig.3.6, the flicker noise degradation by the DTMOS hot carrier stress is enhanced by several times. Therefore, analog devices in DTMOS operation will suffer from a higher drain current noise.

3.4 Temperature Dependence

Historically, elevated temperatures resulted in a decrease in hot electron gate current (and hot carrier damage) due to increased phonon scattering [34], [35]. Fig.3.7 compares the temperature dependence of hot electron gate injection current in the conventional hot carrier stress and in the DTMOS hot carrier stress. The gate injection current in the conventional hot carrier stress has negative temperature dependence. However, the gate current in the DTMOS hot carrier stress exhibits positive temperature dependence. The reason for the positive temperature dependence is two-fold; first, the substrate hole injection increases with the temperature. Second, the Auger recombination rate itself has a positive temperature coefficient [36]. To our knowledge, a positive temperature dependence of hot electron gate injection current is observed here for the first time.

Figure 3.8 illustrates the temperature effect on the drain current degradation by the two stresses. As the temperature is increased from room temperature to 125C, the degradation by the DTMOS hot carrier stress is enhanced by about ten times. This point is particularly important to device reliability since today's high performance devices are required to operate in such high temperature range.

3.5 Substrate Bias Effect on Auger Enhanced Degradation

The substrate bias effect on the Auger enhanced degradation is investigated in Fig.3.9. The corresponding stress drain current is shown in Fig.3.10. As shown in Fig.3.9, the drain current degradation shows opposite temperature dependence in the low substrate bias region and in the high substrate bias region. In the low substrate bias region, the field heating is the dominant electron energy gain process. Therefore, the drain current degradation reduces at a higher temperature because of a larger phonon scattering rate. In the high substrate bias region, both the Auger effect and field heating play a major role in the electron energy gain process and, as mentioned previously, the former mechanism has a positive temperature effect. Furthermore, this figure also shows that the critical substrate voltage for the onset of the Auger enhanced degradation decreases as the temperature increases. The threshold substrate bias for the onset of the Auger effect is about 0.5V at 125C.

3.6 Drain Bias Dependence of Auger Enhanced Degradation

Figure 3.11 demonstrates the dependence of Auger enhanced drain current degradation on the stress drain bias. At a relatively high drain bias (region A), the field heating itself is sufficient to cause severe degradation. Thus, the degradation by conventional hot carrier stress and by DTMOS hot carrier stress is about the same. As the

drain bias reduces (region B), electrons by field heating solely do not gain sufficient energy for interface trap creation. As a result, the combination of Auger recombination and field heating processes can increase the hot electron energy above the threshold for trap creation. Consequently, the Auger enhanced degradation appears to be more significant. Finally, at an extremely low drain bias (region C), the Boltzmann distribution tail is believed to be dominant and the degradation is almost independent of the substrate bias.

Chapter 4 Valence-Band Tunneling Enhanced Hot Carrier Degradation in Ultra-Thin Oxide nMOSFET's

It has been shown in literature that in short gate-length devices hot carrier degradation at V_{gs}~V_{ds} stress is more serious than at maximum I_b stress (V_{gs}~0.5V_{ds}) [37], [38]. Fig.4.1 (a) and 5.1 (b) shows the drain current degradation in two different gate-length nMOSFETs, L_g=0.20μm and L_g=0.13μm, respectively. The gate oxide thickness is t_{ox}=25Å. The corresponding I_b in stress is plotted in Fig.4.2. In the 0.13μm device, the degradation increases first slightly with stress V_{gs}. This characteristic was explained in [38] because the channel hot electrons are confined more closely to the Si surface at a larger V_{gs}. As stress V_{gs} increases above 3V, a drastic rise of the degradation is noticed in both devices. Further study reveals that the degradations at a low stress V_{gs} and at a high stress V_{gs} are both due to interface trap creation (Fig.4.3).

To investigate the correlation of the rise of the degradation with valence band tunneling, we measured I_d degradation and valence-band tunneling current in nMOSFET's with different t_{ox} (Fig.4.4). The t_{ox}=33Å device has a gate length of 0.16μm and other devices have a gate length of 0.13μm. The substrate current measured at V_{ds}=0V, which reflecting valence-band tunneling, is shown in Fig.4.4 (b). The following features should be noted. First, the rise of the I_d degradation in the valence-band tunneling regime is observed in all the devices except for the t_{ox}=33Å device. The valence-band tunneling current in the 33Å device is found to be negligible (result not shown in Fig.4.4 (b)). Secondly, the degradation at maximum I_b stress decreases when t_{ox} reduces. This part is in agreement with the conclusion by *Momose* [39]. However, an opposite trend (i.e., the degradation increases as t_{ox} reduces) is found when the devices are stressed in the valence-band tunneling regime. The process for valence-band tunneling enhanced hot carrier stress is proposed in Fig.4.5. In Fig.4.5 (a), channel holes are created due to valence-band electron tunneling. The generated holes then provide for

recombination with electrons in the channel and transfer the excess energy to other conduction electrons (Fig.4.5 (b)). The energetic electrons arising from the Auger process are subsequently accelerated by a lateral electric field (Fig.4.5 (c)), thus resulting in a larger interface trap generation rate. The entire electron energy gain process therefore depends on V_{gs} (valence band tunneling) and V_{ds} (lateral field acceleration)

To further verify the role of valence-band tunneling created holes in the degradation, we change the substrate bias in stress (Fig.4.6). Fig.4.7 shows the dependence of gate current on substrate bias in stress. For t_{ox}=20Å devices (Fig.4.6 (a)), the degradation in the low V_{gs} region and in the high V_{gs} region exhibits opposite substrate bias dependence. The simulated lateral electric field distribution and the conduction band-edge diagram in the vertical direction are plotted in Fig.4.8. As V_{bs} changes from 0V to -1V, the peak lateral channel field slightly increases, implying stronger lateral field heating. Moreover, the vertical field is also increased, which means the channel electrons are pushed further toward the Si surface. These two factors lead to a larger gate current (Fig.4.7) and increased I_d degradation in the low V_{gs} region. In the high V_{gs} region, we have shown valence-band tunneling plays a role in the degradation. A negative substrate bias can help remove the channel holes to the substrate and thus reduce the hole effect. As a result, the I_d degradation becomes smaller at a negative substrate bias although the stress gate current is larger (Fig.4.7). This result actually excludes the possibility that the rise of the I_d degradation at a large V_{gs} is primarily caused by the increase of stress I_g.

In contrast, the t_{ox}=33Å device shows negative substrate bias dependence in the entire range of stress V_{gs} because of negligible valence-band tunneling effect. In Fig.4.9, we plot the I_d degradation versus the substrate bias in stress. The stress gate bias is 1.3V for the lower curve and 3.4V for the upper curve. The degradation in a floating substrate stress condition is also indicated in the figure.

Chapter 5 Auger Recombination Enhanced Hot Electron Programming in EEPROMs

A stack-gate EEPROM cell and a conventional gate dummy cell are used in this study. The tunnel oxide thickness is 100Å and the gate length is 0.7μm. The dummy cell has a gate width of 20μm.

5.1 Dummy Cell Characteristics

Figure 5.1 displays the dependence of hot electron gate current on substrate bias in a conventional gate nMOSFET. The drain voltage is 3.5V. When V_{bs} increases, the gate current initially decreases due to the reduction of channel lateral field and then increases with V_{bs}. The I_{gs}-V_{gs} characteristic at V_{bs}=1.5V differs from that at V_{bs}=0V. The I_{gs}-V_{gs} has a peak at V_{bs}=0V, while the gate current monotonically increases with V_{gs} at V_{bs}=1.5V. Fig.5.2 illustrates the drain bias dependence of hot electron gate injection current. The dependence on both drain bias and substrate bias confirms that the electron energy gain process in this method consists of Auger recombination and field acceleration. Hot electron luminescence and emission spectra are measured to analyze the hot electron distribution (Fig.5.3). The light intensity is normalized to the drain current. This finding confirms that applying a positive substrate bias can increase the high-energy tail of the channel electrons. In addition, Fig.6.3 shows a small hump around 1.6eV (=1.5E_g) with a positive substrate bias. Theoretically, the most probable electron energy gain in Auger process is about 1.5E_g [40,41]. The appearance of the hump is possibly related to the Auger effect.

The temperature dependence of conventional CHE and AECHE programming is examined in Fig.5.4. The CHE gate current has negative temperature dependence, while the AECHE gate current exhibits slightly positive temperature dependence. This feature

of the AECHE is particularly useful in applications that require high temperature operation.

The injection efficiency (I_g/I_s') of AECHE is evaluated in Fig.5.5, where I_s' is defined as $I_d+I_b(V_{bs}/V_{ds})$ to account for the voltage difference at the substrate and at the drain. Notably, although a large lateral BJT current exists in the AECHE operation, the programming efficiency of the AECHE is still much better than the CHE. In addition, diminishing temperature instability in programming efficiency is obtained in the AECHE.

5.2 EEPROM Characteristics

Figure 5.6 presents the programming characteristics in a EEPROM cell by the CHE and AECHE. V_{cg} is 12V and V_{bs} is 1.5V in the AECHE and V_{cg} is 6V in the CHE. The drain bias is 3.5V. To our knowledge, positive temperature dependence of the HE programming speed is reported for the first time in the AECHE. In contrast to the CHE, a 5x programming speed enhancement factor in the AECHE is obtained at T=25C. The speed enhancement factor is even larger at 125C. Besides, the fact that a higher V_{cg} is allowable in the AECHE makes it possible to achieve a larger threshold voltage window between the programmed state and the erased state.

Chapter 6 Fabrication Process and Characterization Technique of Advanced Gate Dielectrics

6.1 Formation of Oxynitrides

Si (100) wafers (0.025 ohm-cm *n*-type) were given a HF-last RCA clean prior to film deposition. Two types of silicon oxynitride were studied in this work. One set was formed by first oxidizing the wafers in nitric oxide (NO) at a pressure of 4 mTorr for 6 minutes at 780 ^{o}C. Without breaking vacuum, these wafers were exposed to nitrogen plasma for 5 s at a substrate temperature of 300 ^{o}C. The plasma was formed using 450 Watts of absorbed microwave power and 15 sccm of molecular nitrogen in an electron-cyclotron resonance (ECR) apparatus (described previously [42]) positioned 50 cm from the silicon substrates.

Another set of films, produced for comparison purposes, was formed by a standard low-pressure chemical-vapor deposition with silane and dichlorosilane at 780 ^{o}C. These were given a rapid anneal in flowing nitrogen for 30 s at 1000 ^{o}C to densify the films prior to oxidation.

6.2 Oxidation of Oxynitrides

The wafers were introduced into a Heatpulse 610 (Steag RTP Systems) rapid thermal processor (RTP) where they were first heated in flowing nitrogen for 4 minutes at 500 ^{o}C to drive off water vapor. The plasma nitrided wafers were immediately given a 30 s anneal in N_2 at 950 ºC to densify them prior to the oxidation in N_2O but this step was omitted for the LPCVD wafers since they were annealed in N_2 immediately after the LPCVD deposition. All the films were oxidized in flowing N_2O at 950 ºC. To compensate for the optical absorption by N_2O [43], the RTP pyrometer was calibrated by performing measurements on a test wafer with an embedded thermocouple. The accuracy of the temperature measurement is estimated to be ± 25 ^{o}C.

6.3 XPS Analysis of Oxynitrides

The analysis of film composition was done using a PHI XPS instrument which employed a non-monochromatic MgK_{α} *X*-ray source with a hemispherical electron energy analyser at an angle 〃 = 45° from the wafer normal (standard x-ray source position 54.7 ° from analyser). Spectra were obtained with a band-pass energy of 23.5 eV, resulting in an energy resolution of ~1 eV.

A technique for background removal, correcting the measured spectra for inelastic scattering, has been formulated by Tougaard [44] in terms of an inelastic scattering cross-section that varies with the energy lost as a result of the inelastic scattering. Calculations using the inelastic scattering cross-sections for SiO_2 provided in Ref. [44] have been used to evaluate the effect of inelastic scattering. The resultant primary excitation spectra were not significantly different than the spectra obtained from the measured peaks using a linear background correction. This was expected since the inelastic scattering must be small for scattering events that result in energy losses less than the oxynitride band-gap (> 5eV). The analysis of Tougaard [44] has shown that the commonly used Shirley background correction cannot be correct; however, its use would not result in significant changes in the measured intensity ratios, since the background is relatively flat under the main peaks.

The O1s and N1s peak areas were obtained from the fits of one or two Gaussian-Lorenzian functions to the observed spectra. The Si 2p peak was fit with two features: the $2p_{3/2}$-$2p_{1/2}$ doublet characteristic of electron emission from the Si substrate, and a broader Gaussian-Lorenzian peak due to emission from the overlying film. The doublet was characterized using a Si (100) wafer given an RCA-HF last clean and these features (0.61 eV splitting, 2:1 area ratio, 70% Gaussian-30% Lorentzian lineshape) were used for the fitting of the spectra of the oxynitride films. The fit of the oxynitride Si2p spectra thus involved optimizing seven parameters, the full width at half-maximum intensity (FWHM)

of the doublet, its intensity, its position, the intensity of the Si2p (oxynitride) peak, its FWHM, its position, and the ratio of Gaussian/Lorenzian components in its line shape.

In the following the subscripts *o*, *n*, *on*, and *Si* are used to designate parameters for the O1s, N1s, Si2p (substrate), and Si2p (bonded to O and N) features, respectively. It is assumed that the films are homogeneous, and this assumption will be investigated in more detail later. Thus λ_o, λ_n, and λ_{on} are the electron escape depths for the O1s, N1s, and Si2p electrons in an oxynitride film, S_o, S_n, and S_{on} are the atomic sensitivity factors, and C_o, C_n, and C_{on} are the concentrations of oxygen, nitrogen and silicon atoms in the film. The parameter λ_{Si} is the electron escape depth for Si2p electrons in the silicon substrate, C_{si} is the concentration of silicon atoms in the substrate, and d is the film thickness. The following quantities involving the areas, I_o, I_n, I_{on}, *and* I_{Si}, of the four features were used in the analysis of the films [45, 46]:

$$d = \lambda_{on}\cos(\theta)\ln[I_{on}/s_{on}I_{Si}+1], \tag{1}$$

$$R = \frac{C_o}{C_n} = \frac{I_o S_n[1-\exp(-d/\lambda_n\cos\theta)]}{I_n S_o[1-\exp(-d/\lambda_o\cos\theta)]}, \tag{2}$$

$$\frac{C_o}{C_{on}} = \frac{I_o S_{on}[1-\exp(-d/\lambda_{on}\cos\theta)]}{I_{on} S_o[1-\exp(-d/\lambda_o\cos\theta)]}, \tag{3}$$

and
$$\frac{C_n}{C_{on}} = \frac{I_n S_{on}[1-\exp(-d/\lambda_{on}\cos\theta)]}{I_{on} S_n[1-\exp(-d/\lambda_n\cos\theta)]}, \tag{4}$$

where $s_{on} = \lambda_{on}C_{on}/\lambda_{Si}C_{si}$. The sensitivity factor ratios in Eqs. (1)-(3) are related to the escape depths [45] by $S_o/S_{on} = T_o\lambda_o/T_{on}\lambda_{on}$ and $S_n/S_{on} = T_n\lambda_n/T_{on}\lambda_{on}$, where T_o, T_n, and T_{on} are the transmission of the electron analyzer at the energies of the O1s, N1s, and Si2p electrons, respectively. The escape depths were calculated for the O1s and N1s electrons from those for the Si2p electrons using the following expressions:

$$\lambda_o = \lambda_{on}(720/1150)^m, \quad \lambda_o = \lambda_{on}(855/1150)^m, \tag{5}$$

where the O1s, N1s and Si2p electrons have energies of 720, 855, and 1150 eV, respectively. A value of $m = 0.5$ has been used by Seah and Dench [47] and a value of $m = 0.7$ gives a good fit to the data of Tanuma *et al.* [48]. In fact, choosing any value between $m = 0.5$ and $m = 0.7$ results in negligible changes in the calculated values of d, and changes in R of <1.5%. With the use of Eq. (5), the sensitivity factor ratios become independent of oxynitride film composition, as is often assumed.

To calibrate the XPS thickness measurements, spectra were obtained from thick SiO_2 and silicon nitride films. The former was a thermal oxide grown at 1050 ^oC in O_2, while the latter was a high-quality silicon nitride film deposited using a plasma-CVD process [42] which results in a [N]/[Si] ratio of 1.37, as determined by nuclear reaction analysis (NRA) and Rutherford backscattering (RBS) measurements of the nitrogen and silicon contents, respectively. This sample is slightly nitrogen rich, consistent with the <5% at. % hydrogen bonded as NH [42]. The density of silicon dioxide was taken as 2.27 g/cm^3 [49] corresponding to a density of silicon atoms $C_{ox} = 2.28\times10^{22}$ at./cm^3 . The density of the silicon nitride film was determined from the NRA and RBS measurements and the thickness obtained by ellipsometry [42, 50]. This gave a value for the density of 2.95 g/cm^3 which corresponds to a silicon concentration $C_{nit} = 3.80\times10^{22}$ at./cm^3. The nitride wafer was given a 30 s clean in 1% HF solution, rinsed, and blown dry, and the substrates were placed side-by-side on a metal mount along with a piece of Si (100) given an RCA HF-last clean. Spectra were obtained for all three samples, taking care to ensure that the spectrometer alignment and incident x-ray intensity was the same for all three.

Since the films of interest had excellent electrical properties after annealing, it was assumed that the oxynitrides, consisting of molecules of SiO_xN_y, were free of O-N, Si-Si and dangling bonds; i.e., that $x/2+3y/4=1$, ("Mott's law" [51]). It follows that x is related to the oxygen/nitrogen concentration ratio, R, by $x = 4R/(3+2R)$. In Appendix A it is shown that the escape depth in an oxynitride film can be given to a good approximation

by a linear interpolation between those for pure silicon dioxide and nitride films, λ_{ox} and λ_{nit}, respectively, *viz*:

$$\lambda_{on} = \frac{x\lambda_{ox} + (2-x)\lambda_{nit}}{2} = \frac{2R\lambda_{ox} + 3\lambda_{nit}}{(3+2R)}. \tag{6}$$

Finally, it will be shown that σ_{on} differs by <5% for silicon nitride and silicon dioxide so only a small error will be introduced by using the following linear interpolation between the values for pure silicon dioxide and nitride films, σ_{ox} and σ_{nit}, respectively:

$$\sigma_{on} = \frac{x\sigma_{ox} + (2-x)\sigma_{nit}}{2}. \tag{7}$$

Since the electron escape depths depend on the oxygen/nitrogen ratio, and the determination of the latter depends on the calculated thickness, we have used a simple iterative procedure to calculate x and d. It uses pure silicon dioxide values as the initial guesses for λ_{on} and σ_{on}. The iterations, which can be carried out on a simple spreadsheet, involve calculating Eqs. (1), (2), (5), (6) and (7) and then repeating the sequence starting at Eq. (1). Convergence to <0.1% can be obtained after 2 or 3 iterations.

6.4 Electrical Measurements

Al-gated capacitors were made by evaporating aluminum through a shadow mask followed by annealing in forming gas at 380 ºC for 20 minutes and back contacts were made with In-Ga eutectic. The area of the capacitors, $\sim 5\times10^{-4}$ cm^2, was measured to an accuracy of ±2% with a calibrated digitizing camera. Electrical measurements were made by probing the Al gates in a probe-station attached to two instruments, a multi-frequency LCR meter (HP Model 4275A), and a picoammeter/DC voltage source (HP Model

4140B). High frequency CV measurements were made by stepping with 0.1 V steps each second, first from –3 V to +3 V and then in the reverse direction to look for hysteresis. IV characteristics were obtained with the picoammeter by stepping the voltage source from 0 volts in a positive direction (towards accumulation) until breakdown, which was characterized by a steep rise to currents above 10^{-2} A. The equivalent oxide thickness was obtained from the 100 kHz CV characteristics by using the NCSU CV fitting routine [52] which includes quantum effects in the channel.

A. Hajii *et al.* [26] have used a Bruggeman effective medium approximation to estimate the dielectric constant, κ_{oxnit}, of oxynitride films in terms of the value of x:

$$\kappa_{oxnit} = 8.85 - 4.82x + 0.89x^2. \qquad (8)$$

The coefficients were determined for oxynitride films produced by LPCVD with low oxygen contents but the estimate has been used here for our films with higher values of x. The equivalent oxide thickness, d_{eq}, was calculated from the XPS thickness using the relationship $d_{eq} = 3.85\, d/\kappa_{oxnit}$.

Chapter 7 Analysis of Advanced Gate Dielectrics

7.1 Characteristics of the N-1s XPS Peak

The N1s spectra for some of the plasma-nitrided samples are shown in Fig. (1a) and the fit of a single peak to a spectrum is shown in Fig. (2a) for the sample given a 15 s anneal in N_2O. The deviation between the measured spectrum (solid circles) and the fit peak (solid line) is shown by the dotted line (residual errors). With one exception, all the N1s spectra were well fit by one peak. The N_2 plasma increases the FWHM of the N1s spectrum from 1.46 to 1.73 eV and for this spectrum a better fit is produced using two peaks, one at 398.3 eV with 31 % of the total area, and the other at 398.8 eV. Subsequent annealing reduces the FWHM to 1.57 eV, as shown in Table I. The peaks were referenced to the $Si2p_{3/2}$ substrate peak at 99.9 eV, so sample charging or bandbending in the Si substrate could contribute to the small shifts from 398.3 to 398.8 eV shown in Table I. The high-resolution XPS measurements of Hussey *et al.* [53] identified two components in this energy range, a 398 eV peak assigned to Si_3N_4, and a 398.8 eV assigned to an oxynitride species of the form N-Si-O. Others have ascribed a peak at 398.6 eV to bonding states where each N atom is bonded to only two Si atoms, leaving a nitrogen dangling bond [54]. No feature near 400.7 eV attributable to N-O bond [55] was observed in any of the plasma-nitrided films after annealing in N_2O.

The N1s peak was at 398.5 eV for all the LPCVD samples, the FWHM was 1.70 eV before N_2O oxidation, and the FWHM was 1.66 ± 0.01 eV for all the oxidized LPCVD samples. The main peak was fitted with one component and there was no peak near 400.7 eV attributable to N-O bonds. However, the LPCVD films showed a small satellite, which was observable after the N_2O oxidation, with < 0.3 % of the area of the main peak situated at 4.2 eV to the high binding energy side of the main peak. This feature has previously been attributed to screening effects associated with the formation of islands of SiO_2 at the interface [56].

The Si2p spectra for the plasma-nitrided films are shown at various stages of processing in Fig. (1b). The spectral decomposition of the spectrum for the plasma-nitrided film after a 15 sec oxidation in N_2O is shown in Fig. (2b) with the background removed. The sum of the residual errors for the fits are typically < 0.3% of the area of the measured peak areas for all the films after annealing in N_2 or N_2O at 950 ℃. The residuals could be reduced by the addition of more components to the fits but the improvements were not statistically significant. The maximum errors in the area ratio of the Si2p (bonded) to the Si2p (substrate) peaks were estimated to be ~ ±10 %.

7.2 XPS Calibration

Analysis of the O1s signal from the silicon nitride sample indicated that there was approximately an amount of oxide on the nitride surface that would be contained in a 0.12 nm layer of silicon dioxide. Since a heater or sputter gun were not available on the XPS system to remove this contamination, which was probably mostly water, the measured peak areas were corrected by assuming there was a 0.12 nm thick fictitious layer on the surface of both the oxide and nitride standards that absorbed like silicon dioxide but contained no silicon. The sensitivity ratio obtained from the nitride standard was S_n/S_{on} = 1.59, and that from the silicon dioxide standard was S_o/S_{on} = 2.54, resulting in S_o/S_n = 1.59.

The Si2p spectra for the oxide and nitride standards, shown in Fig. (3), are remarkably similar. The intensities, I_{ox} and I_{nit} of the main Si 2p peak near 103 eV were obtained by integration using a linear background which, as discussed above, is consistent with Tougaard's background correction technique [44]. This gave I_{nit}/I_{ox} = 0.97±0.04. For SiO_2, the value of $\sigma_{ox} = 0.75$ and λ_{ox} = 2.96 nm were taken from Ref. [25], and the values, σ_{nit} = 0.73 and λ_{nit} = 1.73 nm, were calculated using the relationship

$\lambda_{\mathrm{nit}}/\lambda_{\mathrm{ox}} = I_{nit}/I_{ox} = (\rho_{nit}C_{nit})/(\rho_{ox}C_{ox})$. The calculated Si2p electron escape depth for silicon nitride is 33% smaller than the value of 2.59 nm obtained from the parameters of Seah and Dench [47].

For comparison with prior studies, the broad feature between 109 and 140 eV in Fig. (3) associated with inelastic scattering was integrated using a Shirley background. The yields, Y_{ox} and Y_{nit}, were estimated for the oxide and nitride films, respectively, by taking the ratios of the main peak intensity to the sum of the intensities of the main and plasmon peaks, $I_{nit}(\infty)$ or $I_{ox}(\infty)$, for the nitride and oxide samples. The results were $I_{nit}(\infty)/I_{ox}(\infty) = 1.03 \pm 0.04$, $Y_{ox} = 0.70$ and $Y_{nit} = 0.68$. The value for SiO_2 is identical to that found in Ref. [25]. The yields were not used in our analysis.

7.3 Thickness and Composition of Annealed Films

Figs. (4) and (5) show the calculated thickness (solid circles) and oxygen/nitrogen concentration ratios (open circles) as a function of N_2O annealing time for the LPCVD and plasma-nitrided films, respectively. Before oxidation in N_2O the silicon oxynitride film formed by plasma-nitridation had an oxygen/nitrogen concentration ratio, $R = 1.9$. The film deposited by LPCVD initially had more nitrogen but was not pure nitride (with $R = 0.9$), likely due to water vapour in the LPCVD furnace or the RTP system used for the post-deposition anneal at 1000 ºC. The LPCVD oxynitride films increased in thickness during the first 20 s by only 0.9 nm and the plasma-nitrided films increased by 1.0 nm during the same time. The more rapid oxidation of the plasma-nitrided films even though they initially have more oxygen is probably due to the fact that they are thinner.

In Fig. (4) the thickness of a film formed by directly oxidizing a Si(100) wafer given a HF-last RCA clean is shown, for comparison, by the open squares. The oxidations were done for 15 and 30 s at 950 ºC in N_2O. The thickness is in agreement with the N_2O oxidation measurements of Ting *et al.* [57], confirming the calibration of our pyrometer. XPS measurements indicate a low nitrogen concentration, as expected, with an N1s peak

position at 398.7 eV and a FWHM of 1.65 eV. Comparing these results with the results for the plasma-nitrided films in Fig. (5) and Table I indicates that, for comparable oxidation times at 950 ºC, the plasma-nitrided and oxidized films have lower equivalent thickness than the films produced by oxidizing bare Si(100) substrates in N_2O, have a much higher nitrogen concentration, and a smaller FWHM indicative of more ordered bonding arrangements.

The equivalent oxide thickness, shown by the solid triangles in Figs. (4) and (5), was calculated from the dielectric constant and XPS thickness. For the plasma-nitrided films in Fig. (5), these can be compared to the equivalent oxide thickness obtained from the CV measurements (solid squares). There is agreement to within 0.2 nm. For the LPCVD films, a higher leakage current interfered with the CV measurements and a reliable equivalent thickness could not be obtained in this manner. The leakage in the LPCVD films might be associated with the presence of silicon dioxide islands at the silicon interface deduced from the N1s spectra. It is also worth pointing out that Song *et al.* [19] annealed their LPCVD films in ammonia prior to N_2O oxidation to reduce their leakage currents.

In Fig. (5) the thickness obtained from the XPS measurements using Eq. (1) with the values of λ_{ox} and σ_{ox} for pure silicon dioxide films is shown for comparison (solid diamonds). The differences between these raw thickness values and those calculated using the values corrected for composition are <0.3 nm over the whole range of oxidation times. The corrections will be more significant for films with lower values of R.

The quantity $4/(2x + 3y) = 4C_{on}/(C_o + 3C_n)$ can be calculated using Eqs. (3) and (4) and a value of 1 is expected for ideal oxynitride films obeying Mott's law [51] (no Si-Si , O-N, or dangling bonds). Except for the plasma-nitrided film before N_2O oxidation, the values shown in Fig. (6) are close to 1, confirming the calibration of our XPS measurements and the high quality of the films.

Figs. (7) and (8) show the 100 kHz capacitance per unit area and current density, respectively, as a function of applied voltage for a plasma-nitrided film with an equivalent oxide thickness of 1.8 nm formed by annealing in N_2O at 950 ºC for 20 s. No hysteresis was observed between the forward and reverse CV sweeps. Fig. (7) also shows the result of the fit from the NCSU CV program used to obtain t_{eq} and Fig. (8) shows the current density for a silicon dioxide film with the same equivalent thickness obtained from the expression of Brar *et al.* [58]. The oxynitride film has lower currents by a factor of 18 at 1V and 22 at 1.5 V than a SiO_2 film with the same d_{eq} and breakdown occurred at 3.5 V. The current reductions are lower than the factor of 100 reduction achieved by Song *et al.* [19] for a N_2O annealed LPCVD nitride with comparable t_{eq}, and this may reflect a lower nitrogen concentration in our films since they were not annealed in ammonia prior to oxidation.

7.4 Discussion

The analysis presented here assumes a uniform stoichiometry throughout the films. To estimate the errors that could be introduced by this assumption, simulations of the O1s, N1s and Si2p intensities were done for films having equivalent thickness, d_{eq}, assuming that all the nitrogen is bonded as an Si_3N_4 layer with a thickness, d_n, under a layer of SiO_2 with a thickness d_o. The equations used are given in Appendix B, and similar equations apply for the other extreme where all the SiO_2 is in a layer situated under a Si_3N_4 layer. The ratio $f = d_o/(d_o+d_n)$ must satisfy the requirement that $d_{eq} = 3.85d_n/8.85 + d_o = d_o(1 + .435/f - .435)$, where the dielectric constants for silicon nitride and silicon dioxide, 3.85 and 8.85, respectively were obtained from Eq. (8). For each pair, f and d_{eq}, the ratios I_o/I_n and $(I_{sin} + I_{sio})/I_{si}$ were calculated, where I_{sio} and I_{sin} are the intensities of the Si2p (bonded) peak from the pure SiO_2 and Si_3N_4 layers, respectively. These ratios were treated as experimental inputs to the iterative solution of Eqs. (1), (2), (5), (6), and (7) to get a self-consistent value of d and R; i.e., the values of d and R our method would

deduce from the simulated peak intensities. Fig. (9) shows plots of d/d_{eq} vs R for d_{eq} = 1.0, 1.5, and 2.0 nm. The solid symbols pertain to the case where the nitride sits on top, and for the open symbols the oxide sits on top. The results show that the extreme distributions can result in large errors, but the errors become less significant for films with smaller d_{eq}. For the plasma-nitrided films used for the CV analysis, d_{eq} = 1.8 nm and $R > 3$, so that errors of up to 25% in the calculated equivalent oxide thickness are possible. The close agreement between the values calculated from the XPS and CV measurements indicates that our plasma-nitrided films have a relatively uniform nitrogen distribution, or that the centroid of nitrogen concentration is near the center of the film.

Obtaining nitrogen depth profiles for such thin films by angle-dependent XPS measurements or by the medium-energy ion-scattering technique available at a few research institutions could be used to verify this conclusion, but these techniques were not readily available and beyond the scope of this work.

Chapter 8 Conclusions

Auger recombination enhanced hot carrier degradation in DTMOS-like operation is reported. The hot electron luminescence and gate injection current measurements in DTMOS have been presented which provide evidence that the channel hot electron tail is increased by the application of a positive substrate bias. The drain current and flicker noise degradations are about ten times more serious by the DTMOS hot carrier stress than by the conventional hot carrier stress. Moreover, the DTMOS hot carrier stress exhibits strong positive temperature dependence. The degradation is increased by an order of magnitude when the temperature is increased from room temperature to 125C. This new degradation mode may cause a severe reliability issue in DTMOS operation and may impose a limitation on the substrate bias applied, thus calling for a trade-off between circuit speed and reliability. Besides, the significance of valence-band tunneling to hot carrier degradation in ultra-thin oxide MOSFETs has been evaluated. The valence-band tunneling enhanced degradation becomes more severe as the gate oxide thickness is reduced. Our study shows this degradation mode exhibits positive substrate bias dependence and may appear to be a new reliability issue in certain applications, such as floating substrate devices (SOI) or positively biased substrate devices (DTMOS). By taking advantage of Auger recombination assisted hot electron energy gain process, a novel hot electron programming technique is proposed. This method is particularly significant at a low drain bias, as electrons cannot gain sufficient energy from channel field to surmount the SiO_2 barrier. Because of different electron energy gain process, this method shows better temperature stability and programming characteristics than the conventional CHE programming.

Thin oxynitride films on Si (100) substrates have been oxidized in N_2O at 950 ºC for times up to 60 s to emulate a process commonly used to improve the quality of gate insulators being developed for deep-submicron CMOS technology. A considerable oxidation is observed to take place on this time-scale with oxygen/nitrogen ratios

increasing from one through four for the LPCVD films and from two through six for the plasma-nitrided films. The concomitant increase in equivalent oxide thickness has been determined by CV analysis, where leakage currents were low enough to perform reliable measurements at 100 kHz. The equivalent oxide thickness was also determined by correcting the thickness obtained by XPS for the dielectric constant (calculated from the oxygen/nitrogen ratio and EMA) were 0.2 nm larger. A 10 % error in the intensity ratios can account for 60 % of this discrepancy. Another possible source of the discrepancy may be the assumed silicon nitride density that was obtained from the silicon nitride standard. This density may not be appropriate for the calculations of the escape depths in silicon oxynitrides. However, an error in the silicon nitride density would produce a discrepancy that decreases with the [O]/[N] ratio, contrary to what is observed in Fig. (5). A larger difference would result from a non-uniform distribution of nitrogen through the films.

By analyzing the photoelectron yield from thick silicon dioxide and silicon nitride films, the electron escape depth in silicon nitride was estimated to be 1.7 nm. Some of the approximations developed to determine the thickness of the films by XPS could be refined. It would be worthwhile to determine the electron escape depths in silicon nitride or oxynitrides directly by comparing thickness measurements of uniform ultra-thin films with TEM measurements. This would require a technique for reliably producing stoichiometric silicon nitride films or uniform oxynitride films with varying thickness. However, the approximations used to extrapolate the electron escape depth for oxynitride from that previously determined for silicon dioxide are not expected to lead to significant errors in this work since the oxidized films had relatively large oxygen/nitrogen ratios. Of more concern is the use of the Bruggeman effective medium approximation, which has only been verified for higher nitrogen concentrations, than that obtained for this work [8].

Finally, we have shown that plasma nitridation of NO-oxidized Si(100) using an ECR nitrogen plasma is capable of producing high-quality gate dielectrics. For a plasma oxynitride with t_{eq}=1.8 nm we have achieved current reductions of ~20 for gate voltages

in the range 1-1.5V. Further analysis of these plasma-nitrided films on MOSFETs with poly-silicon gates would be worthwhile.

Appendix A. A linear approximation for λ_{on}

In this Appendix a linear interpolation for the electron escape depth in silicon oxynitride, λ_{on}, is derived in terms of the electron escape depths in pure silicon dioxide and nitride, λ_{ox} and λ_{nit}, respectively. An interpolation of the oxynitride molecular volume from the molecular volumes V_{ox} and V_{nit}, respectively, of the constituents SiO_2 and $SiN_{4/3}$ can be used for an oxynitride obeying Mott's law, *viz*:

$$V_{oxnit} = \frac{x}{2} \cdot V_{ox} + \frac{(2-x)}{2} \cdot V_{nit} = \frac{3}{3+2R} \cdot V_{nit} + \frac{2R}{3+2R} \cdot V_{ox}. \qquad \text{(A1)}$$

Since the energy of the Si 2p photoelectrons is relatively large ($E=1150$ eV), the simple relationship tabulated by Seah and Dench [47] can be used to relate the scattering mean-free path (in nm) for the oxynitride, $\lambda_{on} = 0.72a^{3/2}E^{1/2}$, where the monolayer thickness (in nm), $a = [V_{oxnit}/(1+x+y)]^{1/3}$, and V_{oxnit} is the volume of the oxynitride molecule with composition SiO_xN_y. This results in an estimate for the mean-free path for the oxynitride:

$$\lambda_{on} = 0.72E^{1/2}\left[\frac{3V_{nit} + 2R \cdot V_{ox}}{(7+6R)}\right]^{1/2} = 0.72E^{1/2}\left[\frac{3(1-x/2) \cdot V_{nit} + 3x/2 \cdot V_{ox}}{(7+x)}\right]^{1/2}. \qquad \text{(A2)}$$

The molecular volumes V_{ox} and V_{nit} were estimated from the densities of SiO_2 and Si_3N_4, 2.27 and 2.95 g/cm^3, respectively. The values of mean-free path calculated using this relation are $\lambda_{nit} = 2.59$ nm and $\lambda_{ox} = 2.93$ nm, for silicon nitride and silicon dioxide, respectively. The calculations show that between these limits a simple linear interpolation, $\lambda_{on} = x/2 \cdot \lambda_{ox} + (1-x/2) \cdot \lambda_{nit}$, results in deviations from Eq. (A2) of no larger than *1%*. This justifies the use of a linear interpolation for the oxynitride films; however, since the measured electron escape depths for silicon dioxide and silicon nitride films differ from those calculated above, the experimental values of λ_{ox} and λ_{nit} have been used in the interpolation for λ_{on}.

Appendix B. Intensities for Two-Layer Films

In this Appendix the intensities of the O1s, N1s, Si2p peaks are calculated assuming a film having an equivalent oxide thickness, d_{eq}, is composed of two layers, one pure oxide with thickness d_o and a dielectric constant of 3.85, and the other pure nitride with thickness d_n and dielectric constant of 8.85. The thicknesses of the two layers are fixed by d_{eq} and a specification of the fraction of the total thickness, f, which is silicon dioxide:

$$d_o = \frac{8.85 f d_{eq}}{8.85 f + 3.85(1-f)}, \text{ and } d_n = \frac{8.85(1-f) d_{eq}}{8.85 f + 3.85(1-f)}. \tag{B1}$$

Assuming the silicon nitride layer sits underneath the silicon dioxide layer, the following standard equations can be written [45, 46]:

$$I_o = S_o C_o [1 - \exp(-d_o / \lambda_o \cos\theta)], \tag{B2}$$

$$I_n = S_n C_n [1 - \exp(-d_n / \lambda_n \cos\theta)] \exp(-d_o / \lambda_{n,ox} \cos\theta), \tag{B3}$$

$$I_{Si} = S_{Si} C_{Si} \exp(-d_n / \lambda_{nit} \cos\theta) \exp(-d_o / \lambda_{ox} \cos\theta), \tag{B4}$$

$$I_{sio} = S_{ox} C_{ox} [1 - \exp(-d_o / \lambda_{ox} \cos\theta)], \text{ and} \tag{B5}$$

$$I_{\sin} = S_{nit} C_{nit} [1 - \exp(-d_n / \lambda_{nit} \cos\theta)] \exp(-d_o / \lambda_{ox} \cos\theta), \tag{B6}$$

where $\lambda_{n,ox}$ is the escape depth for the N1s electrons in silicon dioxide. Assuming, again, that the escape depths scale with $E^{1/2}$ [47], gives $\lambda_{n,ox} = \lambda_{ox}(855/1150)^{1/2}$. Similar equations can be derived for the case where the silicon nitride is on top of the silicon dioxide.

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Table I

Full width at half maximum (FWHM) and binding energy (BE) of the N-1s XPS peak for plasma-deposited silicon oxynitride films after various process steps during formation and after annealing at 950 ºC in N_2O.

Process	**FWHM** (eV)	**BE** (eV)
NO at 780 ºC for 6 min	1.46	398.3
N_2 plasma at 300 ºC for 5 s	2.11	398.6
anneal at 950ºC in N_2 for 30 s	1.60	398.6
15 s in N_2O	1.58	398.7
20 s in N_2O	1.57	398.8
30 s in N_2O	1.57	398.8
60 s in N_2O	1.57	398.8

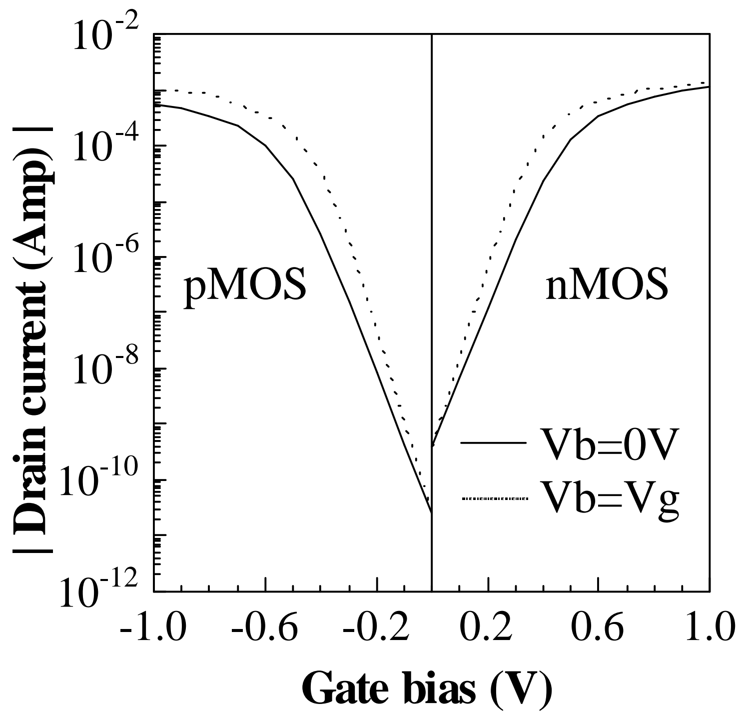


Fig.1.1 Subthreshold characteristics of nMOSFET's and pMOSFET's, operating in DTMOS and standard MOS regimes. $|V_{ds}|$=0.1V. Higher I_{on}/I_{off} ratio can be obtained in DTMOS operation mode.

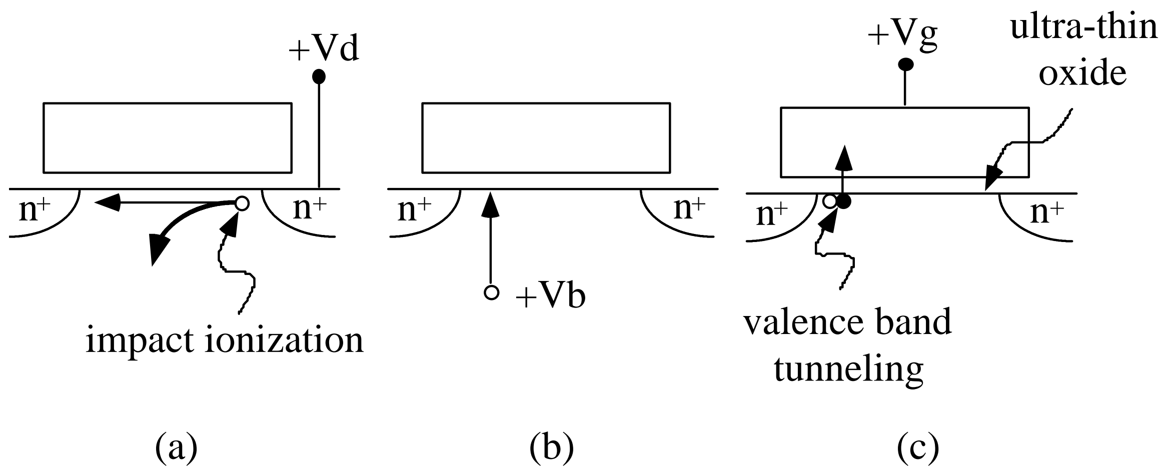
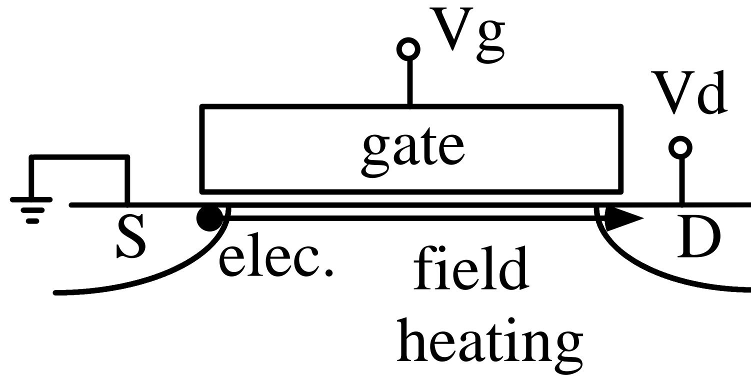


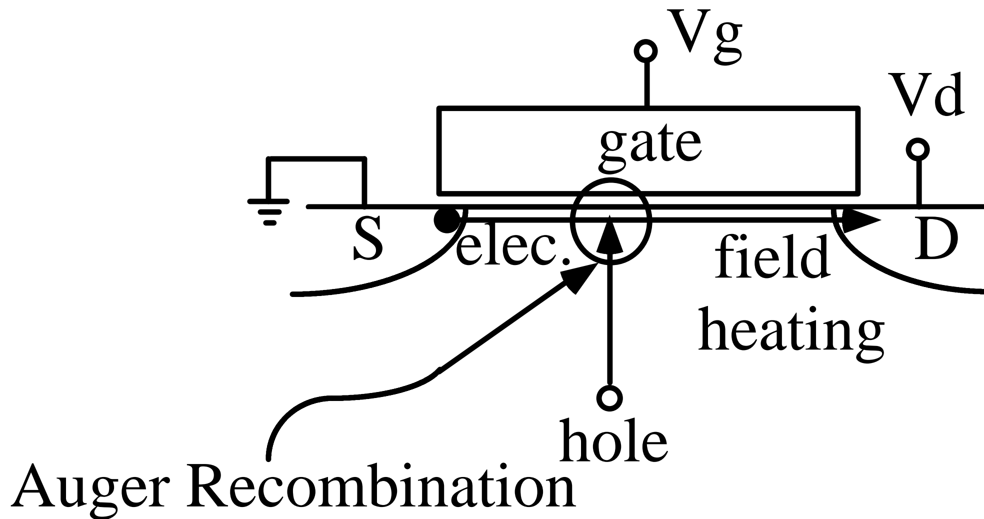
Fig. 2.1 Auger recombination process in various nMOSFET's operation conditions. (a)Impact ionization created holes flowing to the region near the source. (b)Substrate hole injection to the channel with a positive substrate bias. (c)+V_g induced valance-band electron tunneling and leaving holes in the Si substrate.

conventional HC stress (V_b=0)



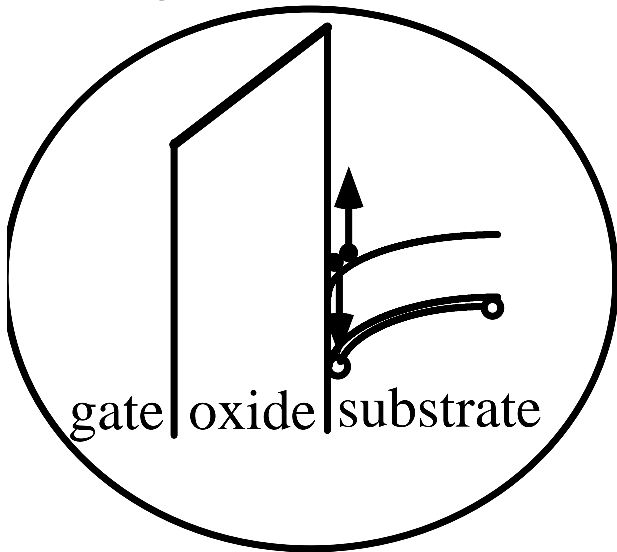
(a)

HC stress with positive V_b



(b)

Fig. 2.2 Electron energy gain process in the (a) conventional hot carrier stress (V_{bs}=0V) and (b) DTMOS hot carrier stress (V_{bs}>0V).



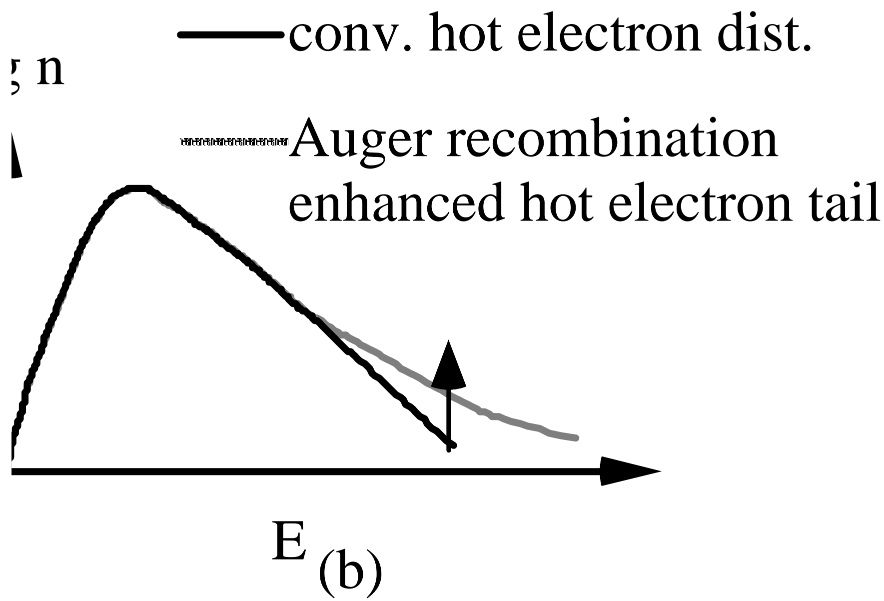


Fig. 2.3 (a) Auger recombination assisted hot electron energy gain process.

(b) Hot electron energy distribution in the conventional hot carrier stress and in the DTMOS hot carrier stress. High energy tail of channel electrons is increased in the DTMOS hot carrier stress.

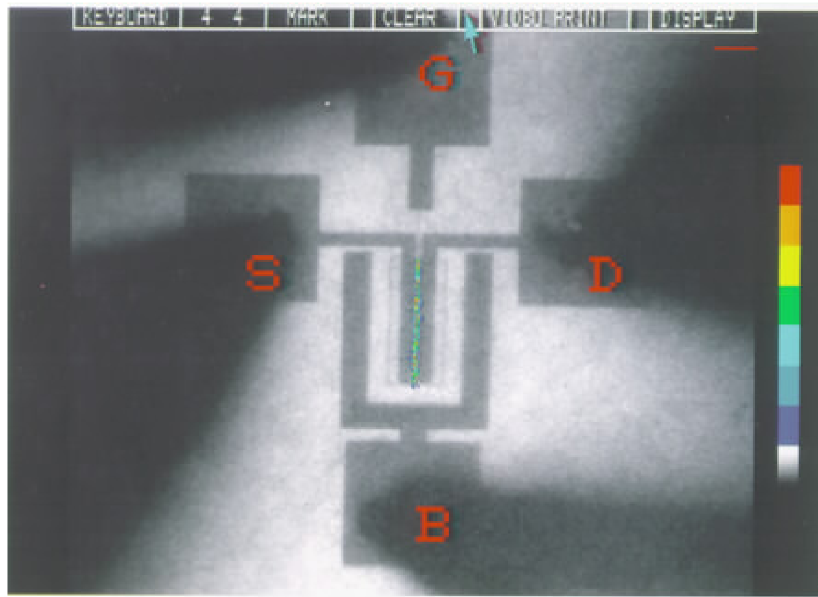


Fig. 2.4a The micrograph of hot carrier light emission from a nMOSFET with L_g=0.3μm and W_g=100μm. V_{ds}=2.9V, V_{gs}=1.5V and V_{bs}=0V. The band pass filter is 800Å. The total exposure time is 100 sec.

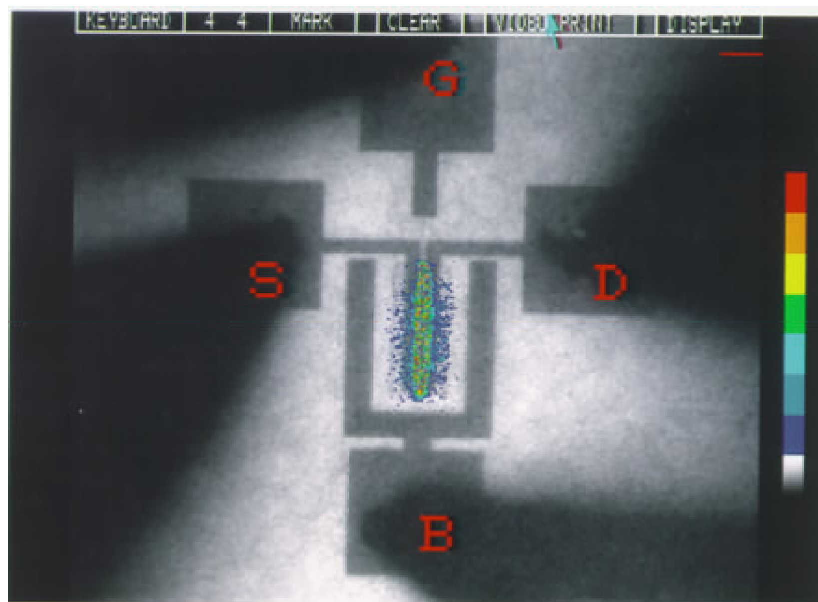


Fig. 2.4b The micrograph of hot carrier light emission from a nMOSFET with L_g=0.3μm and W_g=100μm. V_{ds}=2.9V, V_{gs}=1.5V and V_{bs}=0.7V. The band pass filter is 800Å. The total exposure time is 100 sec.

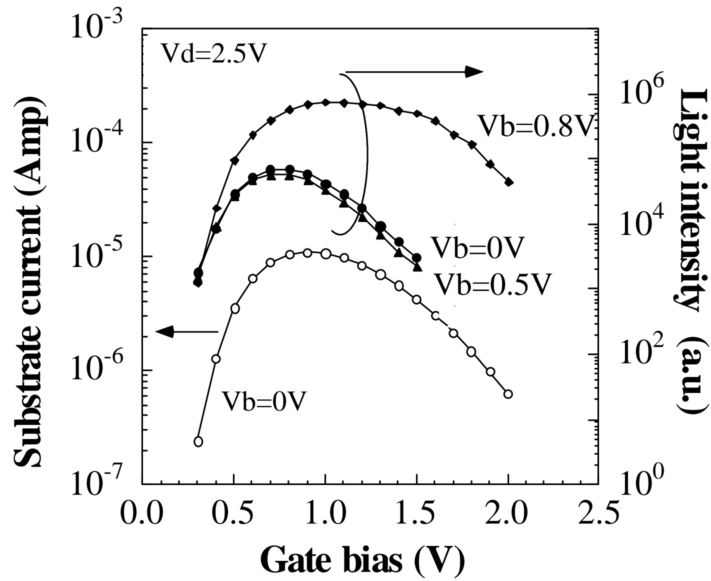


Fig. 2.5 Substrate current and light intensity as a function of gate bias with different substrate biases. V_{ds}=3.5V. The band pass filter is 800Å.

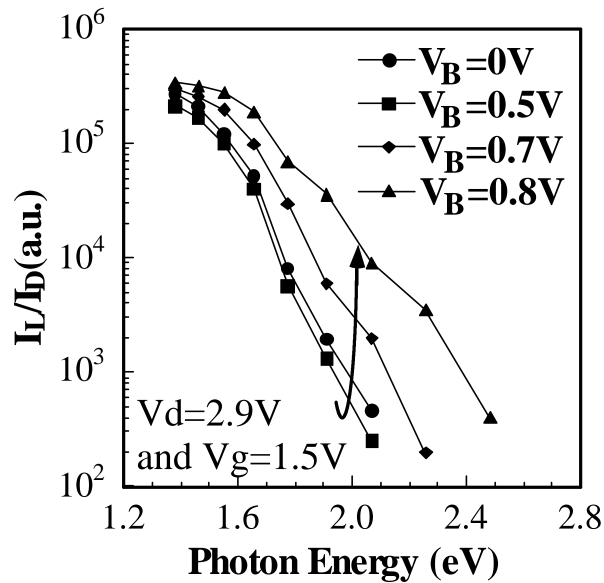


Fig. 2.6 Hot electron light emission in a nMOSFET with different substrate biases. I_L is the light intensity.

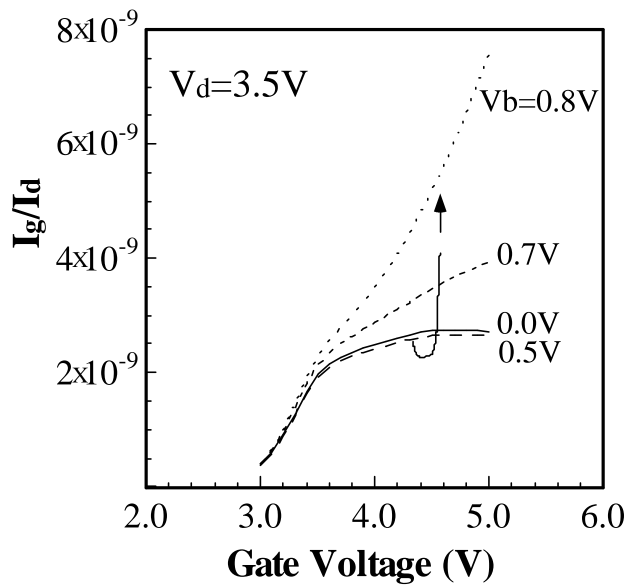


Fig. 2.7 Normalized gate current versus gate voltage with different substrate biases. V_{ds}=3.5V.

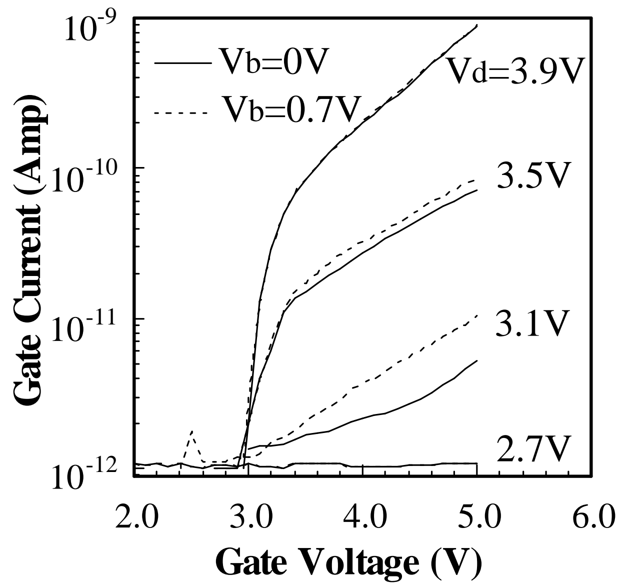


Fig. 2.8 Gate current versus gate voltage at different drain biases.

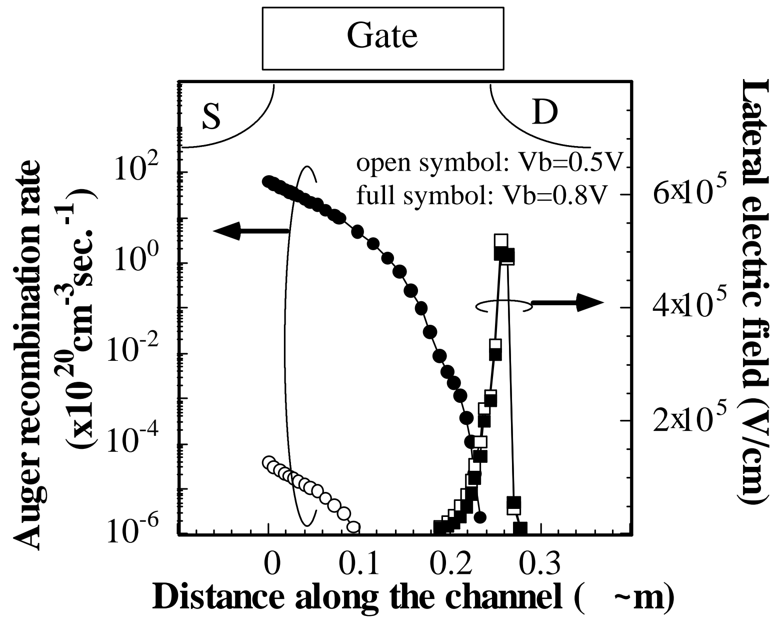


Fig. 2.9 Simulated Auger recombination rate and lateral electric field along the channel. V_{ds}=2.9V and V_{gs}=1.5V.

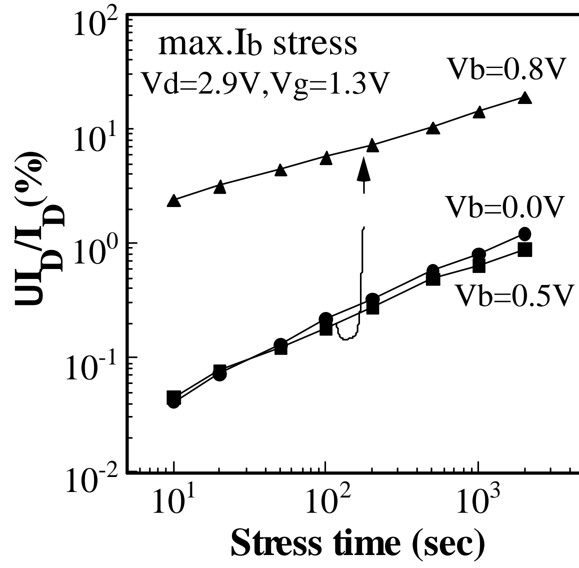


Fig. 3.1 Linear drain current degradation as a function of stress time. Drain current is measured at V_{gs}=2.0V and V_{ds}=0.1V. Stress drain bias is 2.9V and gate bias is 1.5V.

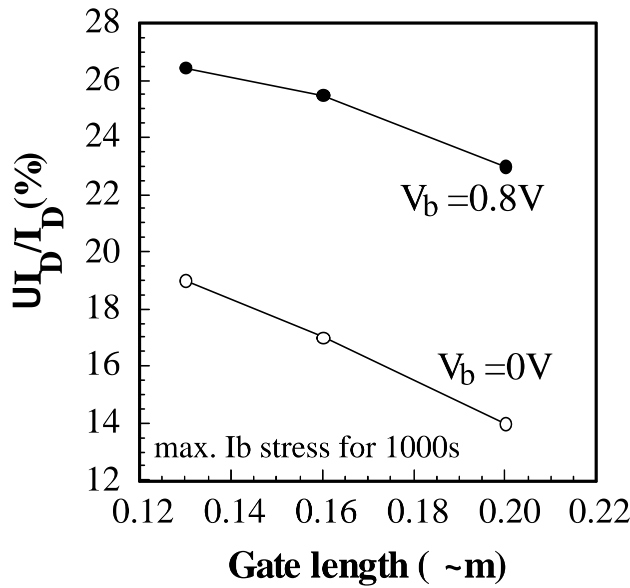


Fig. 3.2 Gate length dependence of Auger enhanced degradation. Stress V_{ds}=2.9V. The stress time is 1000 sec.

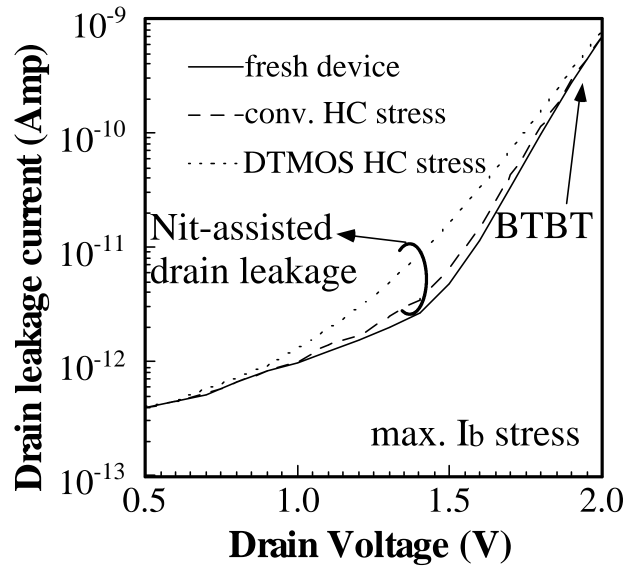


Fig. 3.3 Drain leakage current degradation by the conventional hot carrier stress and by the DTMOS hot carrier stress. Stress drain bias is 2.9V. The stress time is 1000 sec.

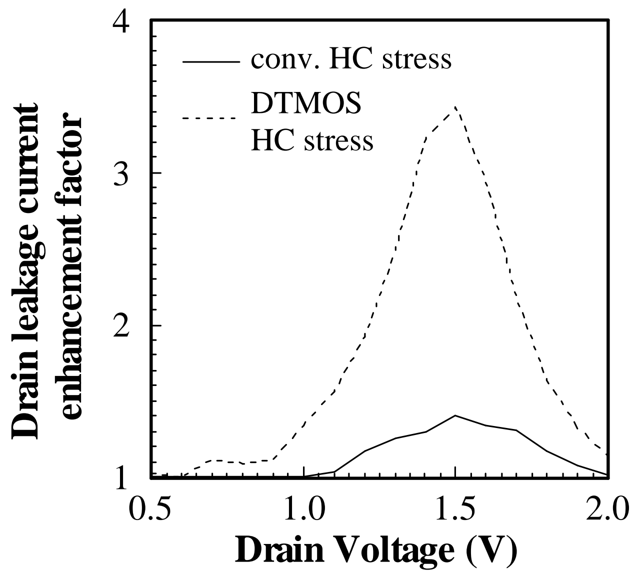


Fig. 3.4 Drain leakage current enhancement factor by the conventional hot carrier stress and by the DTMOS hot carrier stress. Stress drain bias is 2.9V. The stress time is 1000 sec.

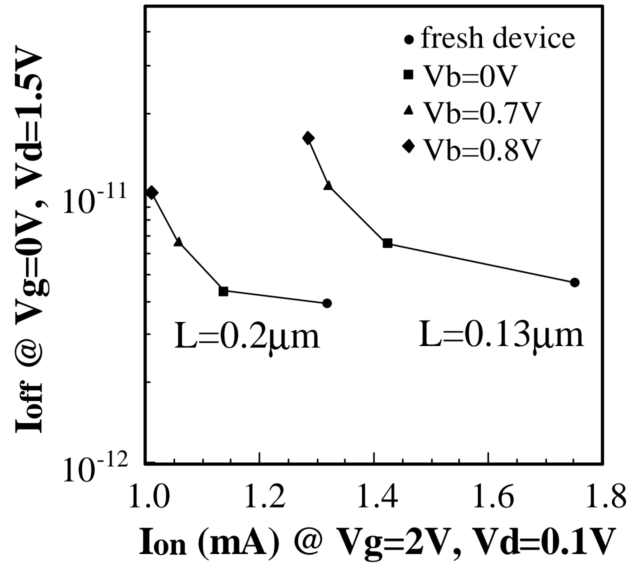


Fig. 3.5 I_{on}/I_{off} characteristics before and after different stress substrate biases. The on-state current is measured at V_{gs}=2.0V and V_{ds}=0.1V. Off-state current is measured at V_{gs}=0V and V_{ds}=1.5V. Stress drain bias is 2.9V and gate bias is 1.5V. The stress time is 1000 sec.

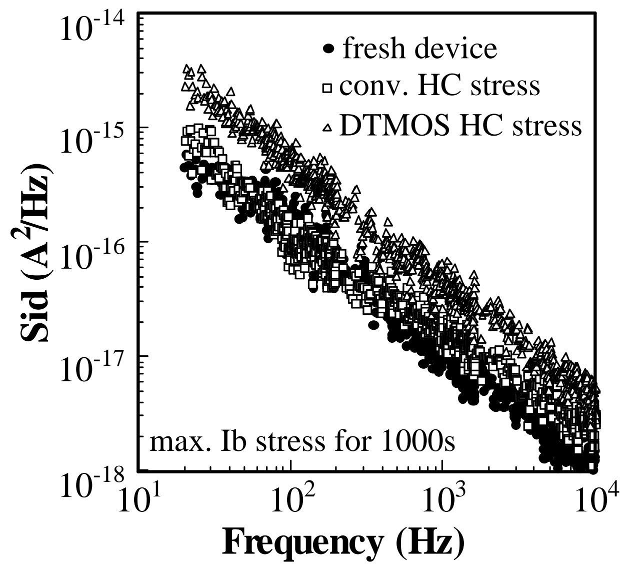


Fig. 3.6 Flicker noise degradation by the conventional hot carrier stress and by the DTMOS hot carrier stress. V_{ds}=2.9V and V_{gs}=1.5V. The stress time is 1000 sec.

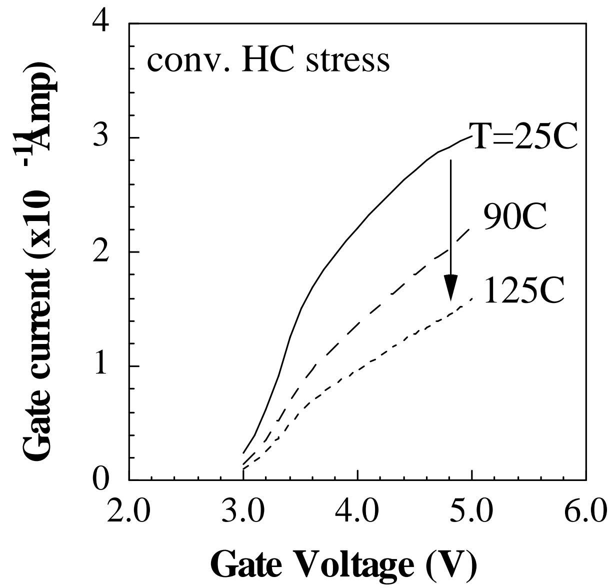


Fig. 3.7a Temperature dependence of hot electron gate current in the conventional hot carrier stress. V_{ds}=3.5V. Negative temperature dependence is observed.

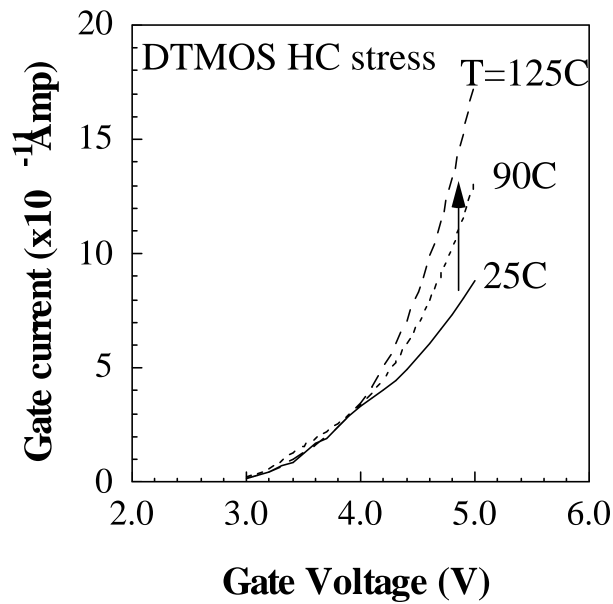


Fig. 3.7b Temperature dependence of hot electron gate current in the DTMOS hot carrier stress. V_{ds}=3.5V. The gate current exhibits positive temperature dependence.

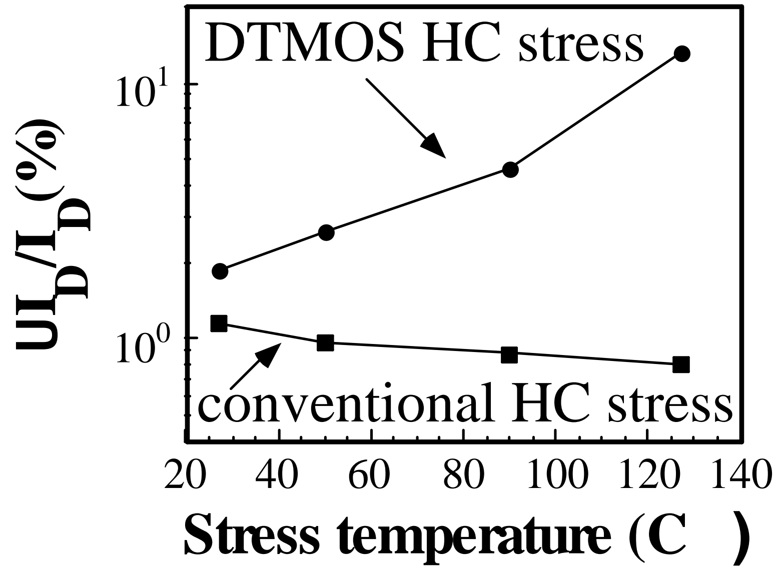


Fig. 3.8 Temperature dependence of linear drain current degradation. V_{ds}=2.9V and V_{gs}=1.5V. The stress time is 2000 sec.

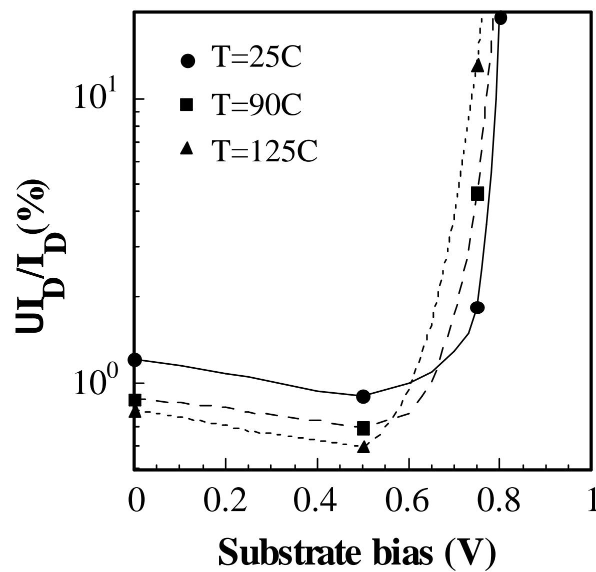


Fig. 3.9 Substrate bias dependence of linear drain current degradation at different stress temperatures. V_{ds}=2.9V and V_{gs}=1.5V. The stress time is 2000 sec.

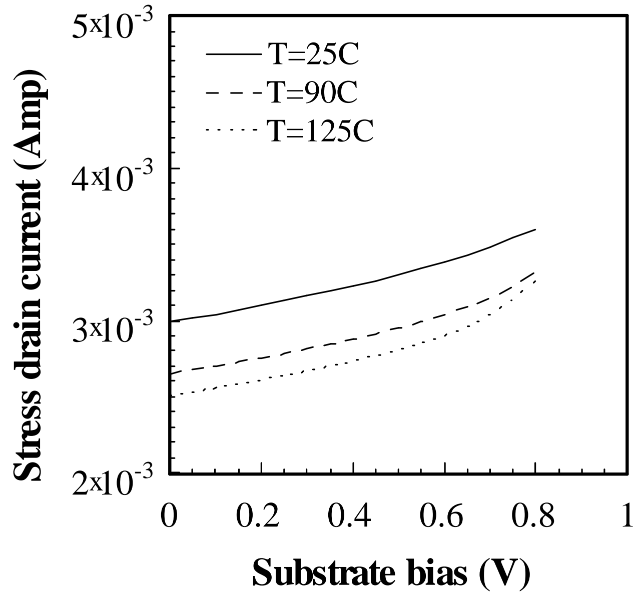


Fig. 3.10 Substrate bias dependence of stress drain current at different stress temperatures. V_{ds}=2.9V and V_{gs}=1.5V.

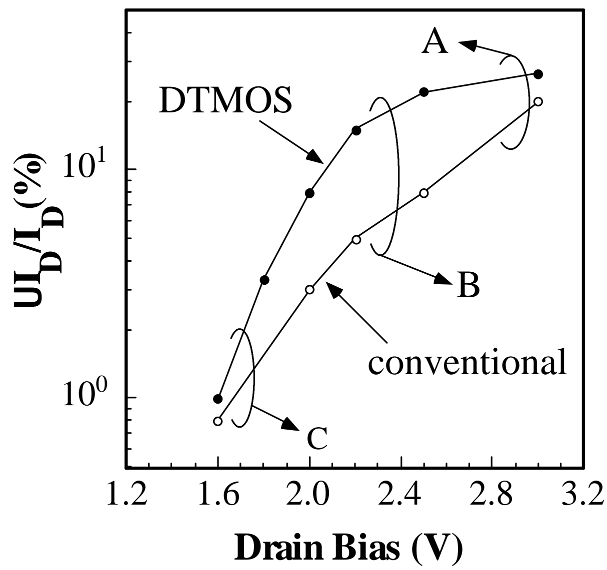


Fig. 3.11 Linear drain current degradation as a function of stress drain bias. The stress time is 2000 sec. Region A, B and C indicate the different hot carrier degradation mechanisms.

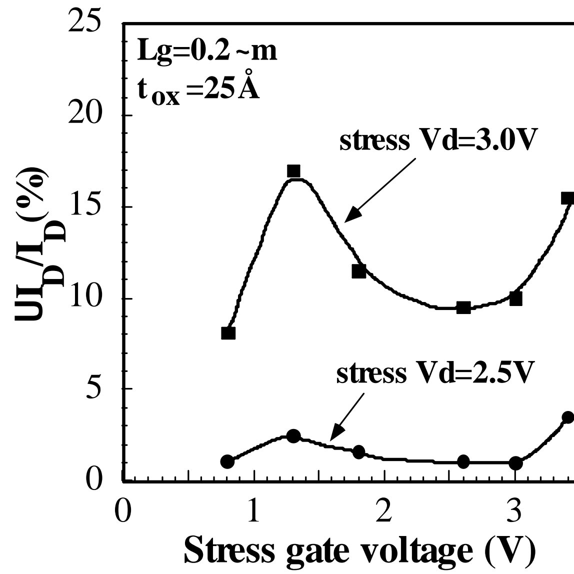


Fig. 4.1a I_d degradation versus stress gate bias in L_g=0.2μm nMOSFET's. Stress V_{ds} is 3.0V and 2.5V. Stress time is 500 sec. I_d degradation is measured at V_{ds}=0.1V and V_{gs}=1.5V.

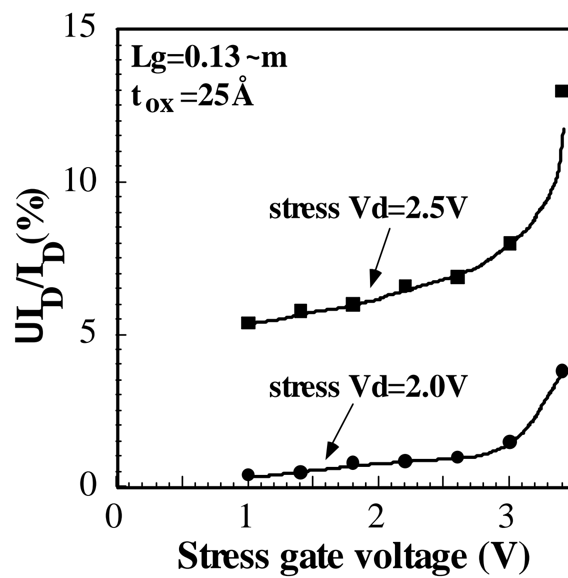


Fig. 4.1b I_d degradation versus stress gate bias in L_g=0.13μm nMOSFET's. Stress V_{ds} is 2.5V and 2.0V. Stress time is 500 sec. I_d degradation is measured at V_{ds}=0.1V and V_{gs}=1.5V.

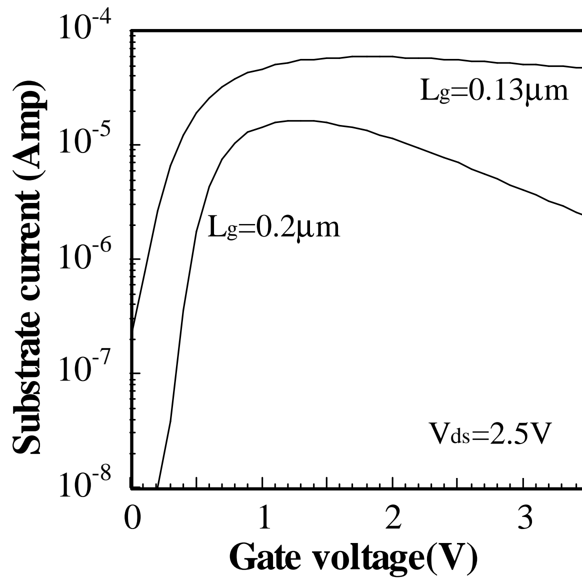


Fig. 4.2 Substrate current versus gate voltage, V_{ds}=2.5V.

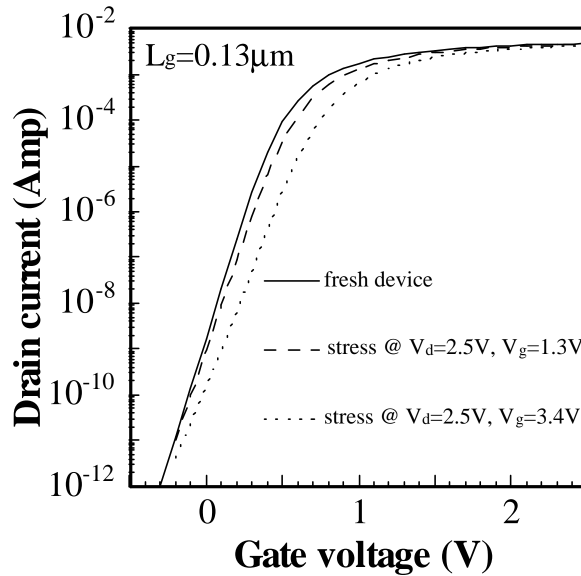


Fig. 4.3 Measured subthreshold characteristics in a fresh device, after V_{ds}=2.5V and V_{gs}=1.3V stress and after V_{ds}=2.5V and V_{gs}=3.4V stress. Stress time is 500 sec. The swing degradation indicates that the cause of degradation is interface trap creation.

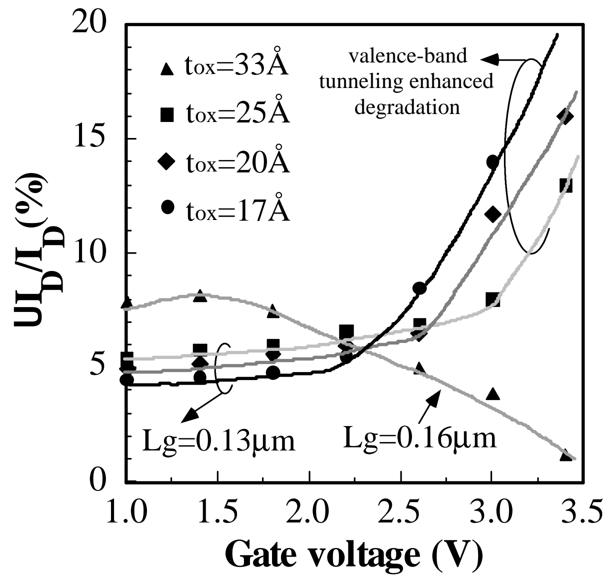


Fig. 4.4a I_d degradation versus stress gate bias in nMOSFET's with t_{ox}=17Å, 20Å, 25Å and 33Å. Stress V_{ds} is 3.0V for the t_{ox}=33Å device and 2.5V for other devices.

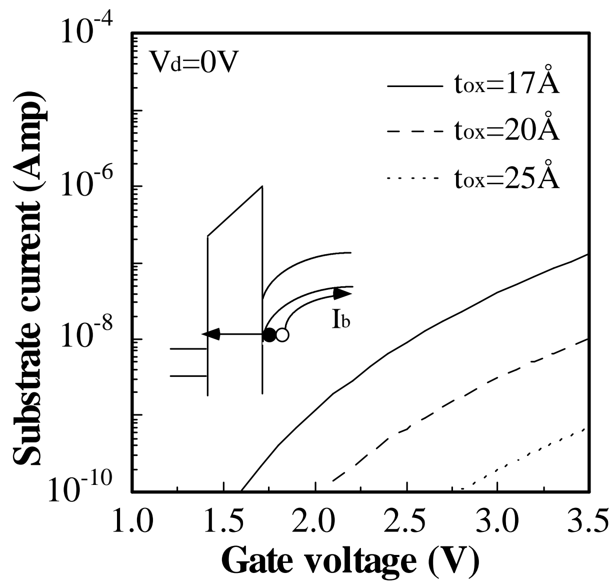


Fig. 4.4b Substrate current versus gate bias with V_{ds}=0V. This substrate current results from valance-band electron tunneling.

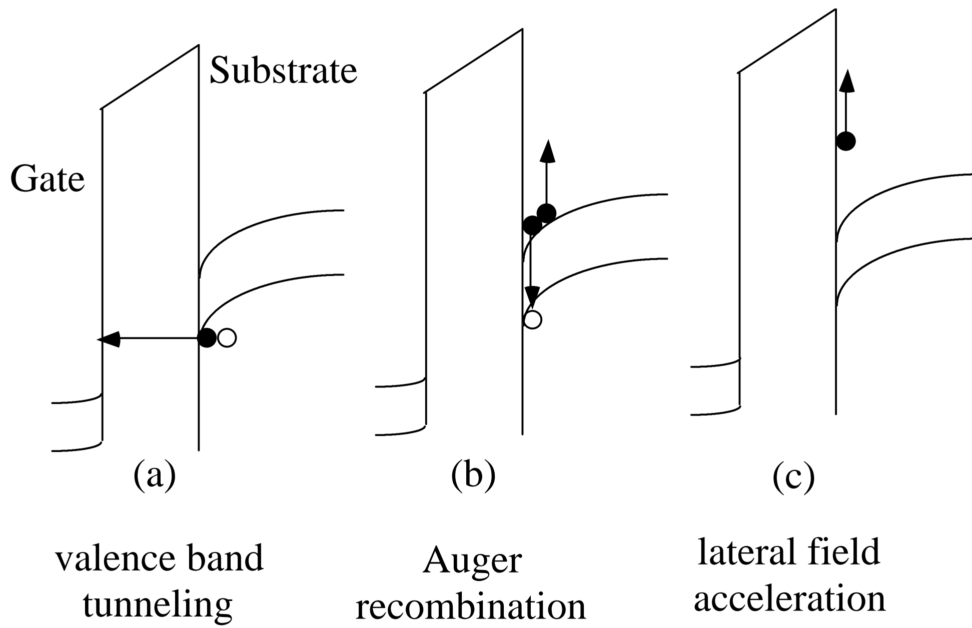


Fig. 4.5 Illustration of valance-band tunneling enhanced hot electron process.

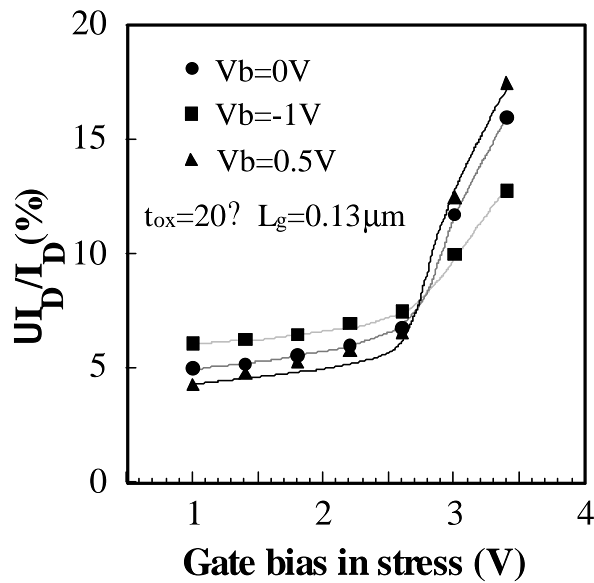


Fig. 4.6a Drain current degradation with different substrate biases in stress, V_{bs}=0.5V, 0V and -1V. t_{ox}=20Å and stress V_{ds}=2.5V.

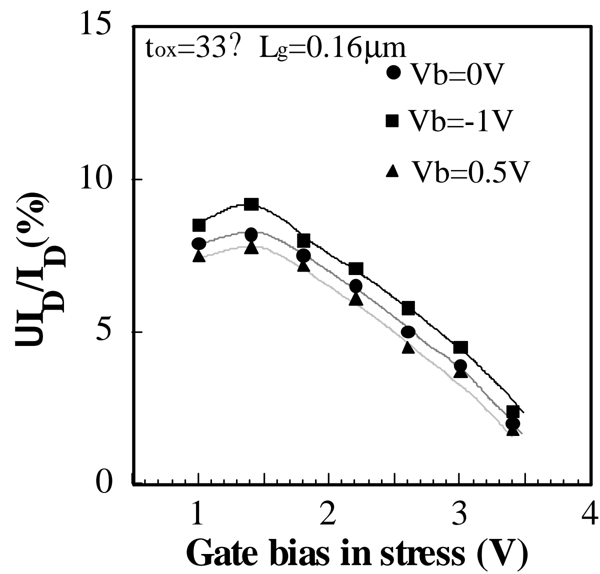


Fig. 4.6b Drain current degradation with different substrate biases in stress, V_{bs}=0.5V, 0V and -1V. t_{ox}=33Å and stress V_{ds}=3.0V.

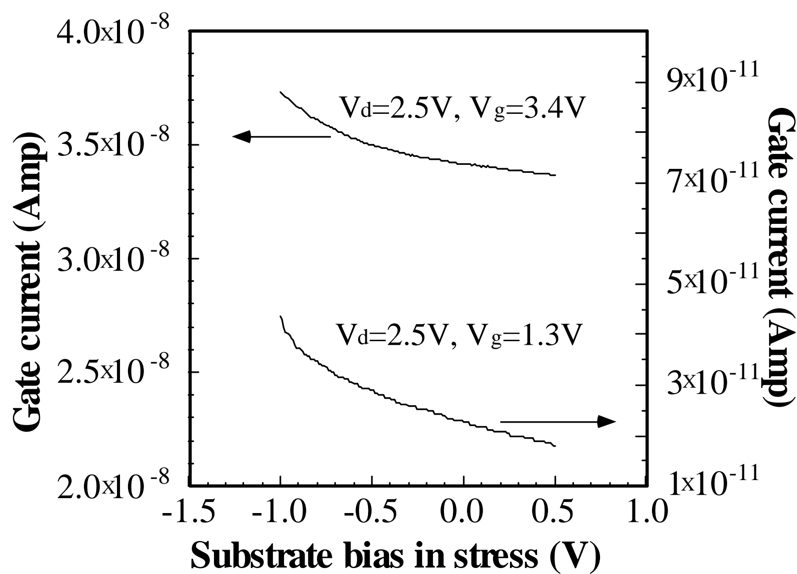


Fig. 4.7 Dependence of gate current on substrate bias in stress. L_g=0.13µm and t_{ox}=25Å.

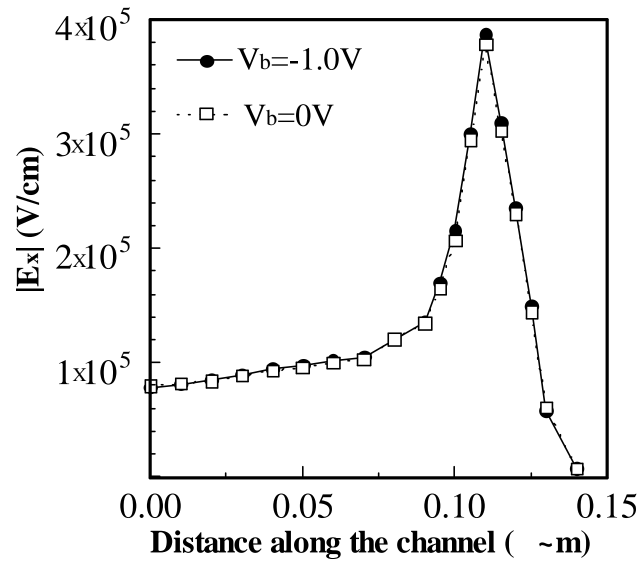


Fig. 4.8a Simulated lateral field distributions along the channel. V_{ds}=2.5V, V_{gs}=3.4V, V_{bs}=0V and -1V. The source junction is at x=0.0µm.

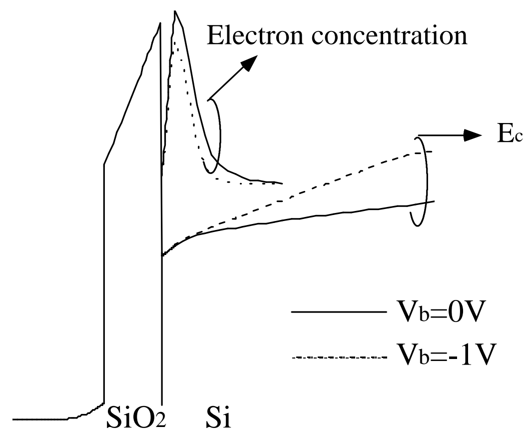


Fig. 4.8b Simulated conduction band-edge diagram and electron concentration distribution in the vertical direction from coupled 1D Poisson equation and Schrodinger equation. The centroid of the electron distribution is closer to the Si surface at V_{bs}=-1V.

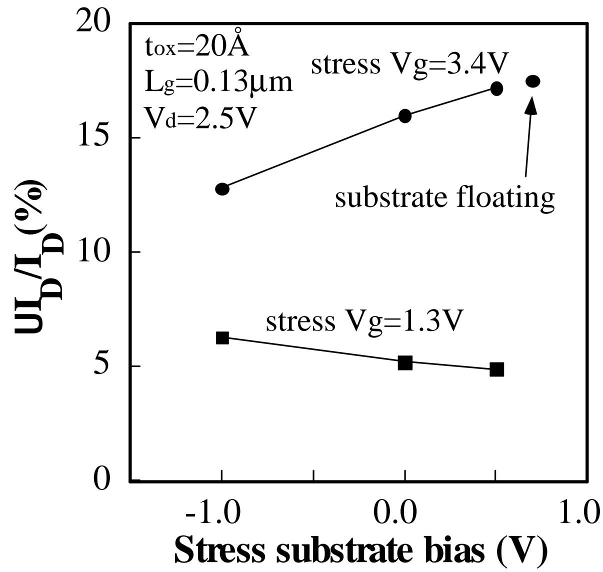


Fig. 4.9 Substrate bias dependence of the drain current degradation at two different stress V_{gs}, 1.3V and 3.4V. The degradation in a stress condition of V_{ds}=2.5V, V_{gs}=3.4V and substrate floating is indicated.

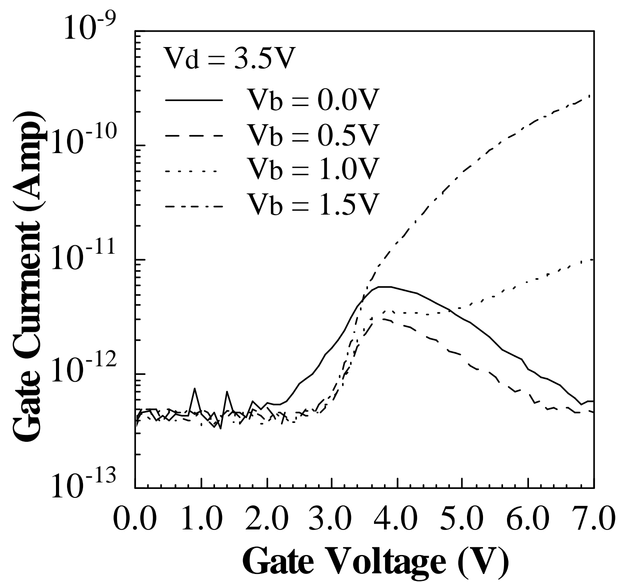


Fig. 5.1 The dependence of hot electron gate current on substate bias. The threshold voltage of the device is about 1.5V.

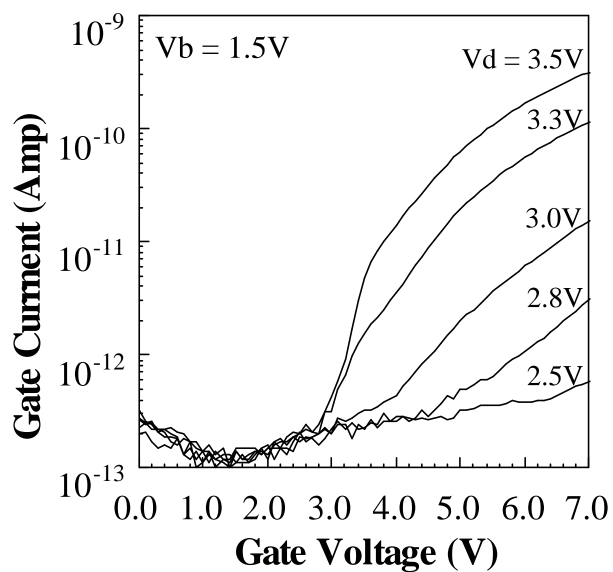


Fig. 5.2 The dependence of hot electron gate current on drain bias. The threshold voltage of the device is about 1.5V.

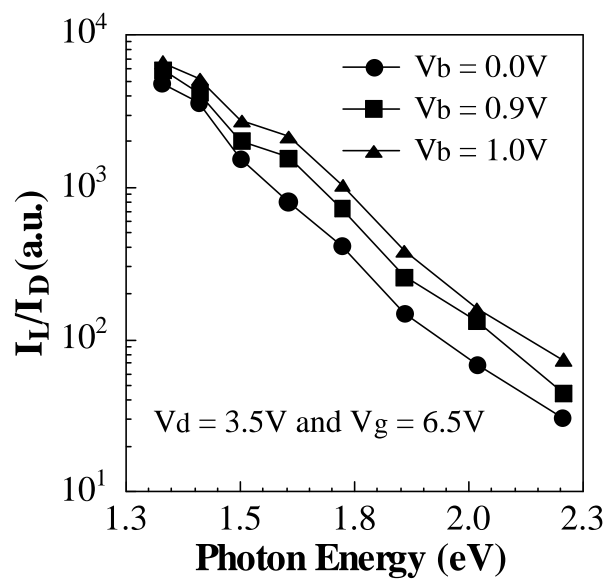


Fig. 5.3 Hot electron light emission spectrum in a nMOSFET with different substrate biases. I_L is the light intensity.

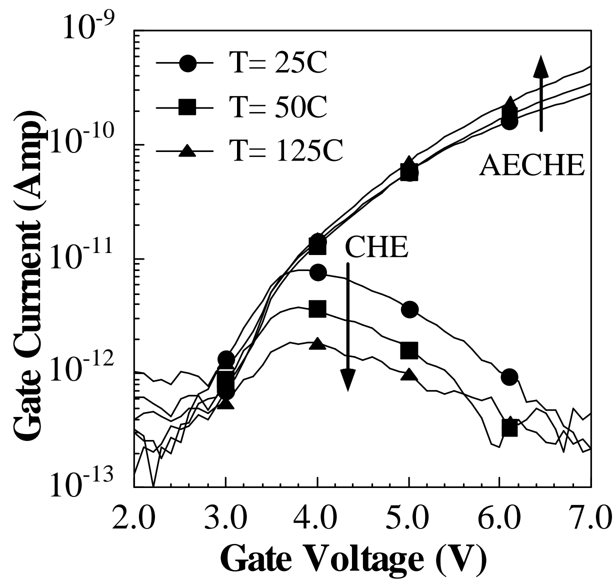


Fig. 5.4 Temperature dependence of hot electron gate current at V_{bs}=0V (CHE) and 1.5V (AECHE). The drain bias is 3.5V.

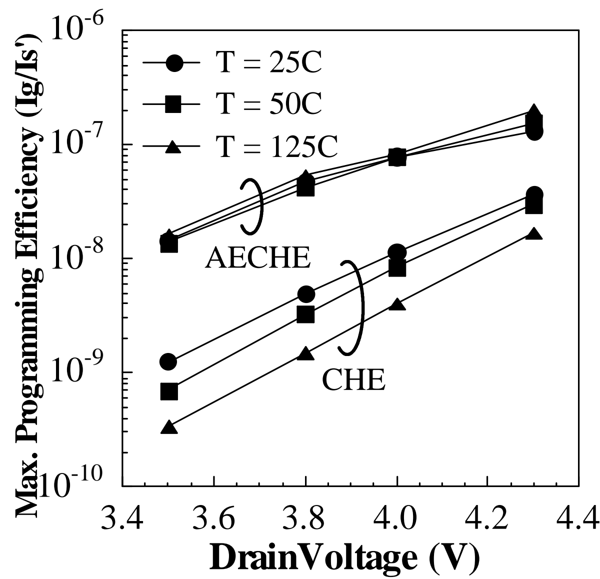


Fig. 5.5 Max. programming efficiency in a range of 0V=V_{gs}=7V versus drain bias. I_s' is defined as I_d+I_b(V_{bs}/V_{ds}).

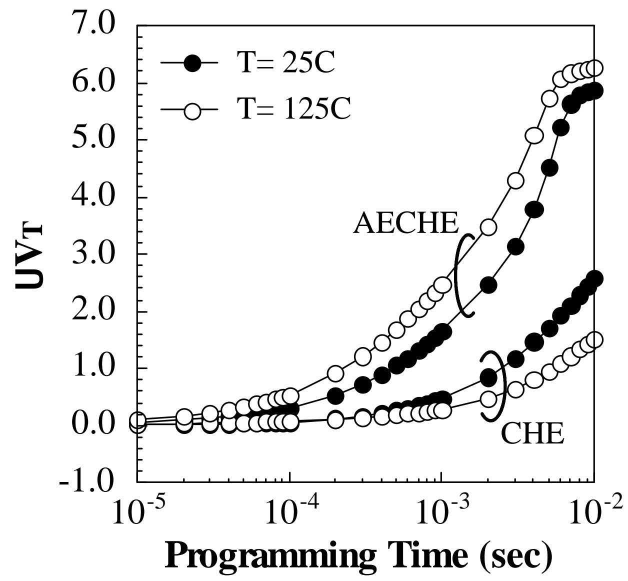


Fig. 5.6 Programming characteristics of the CHE and the AECHE at T=25C and 125C. V_{ds}=3.5V.

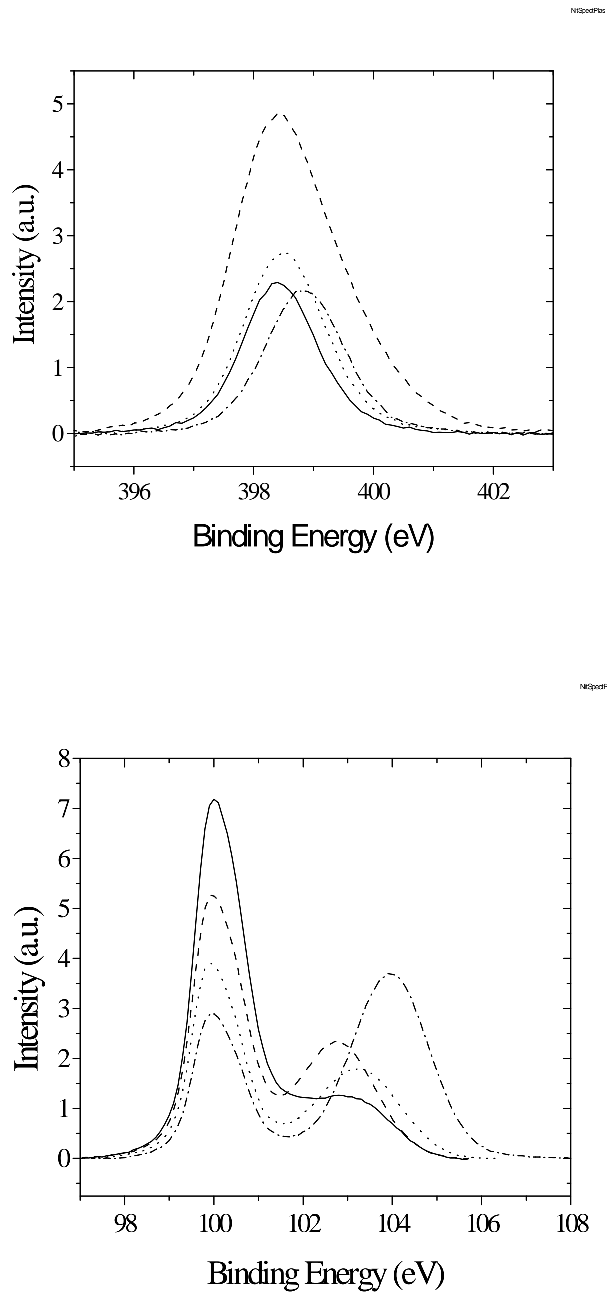
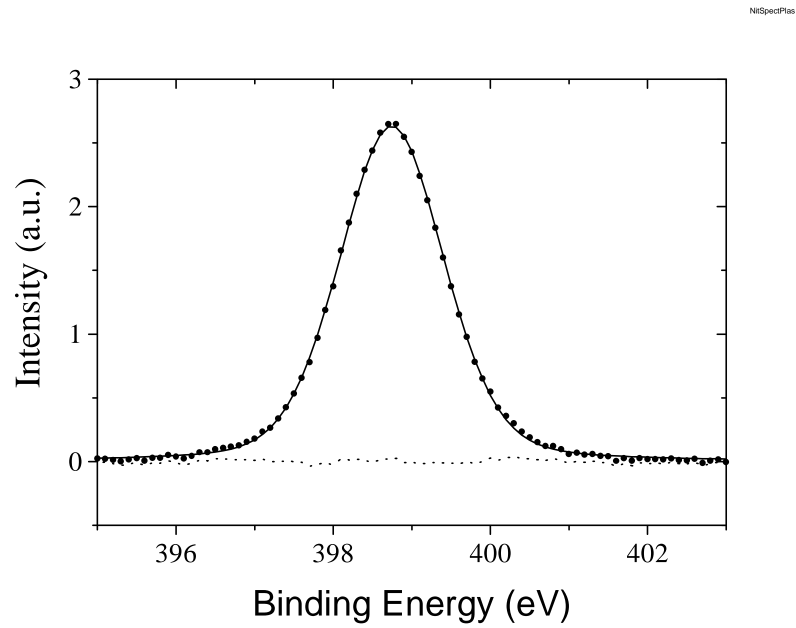


Fig. 7.1 (a) N-1s spectra and (b) Si-2p spectra of plasma nitrided films at various stages of processing: (——) after oxidation of Si(100) in NO at 780 ºC, (----) after exposure to N_2 plasma, (·····) after 30 s anneal in N_2 at 950 ºC, (·-·-·) after 60 s anneal in N_2O at 950 ºC.



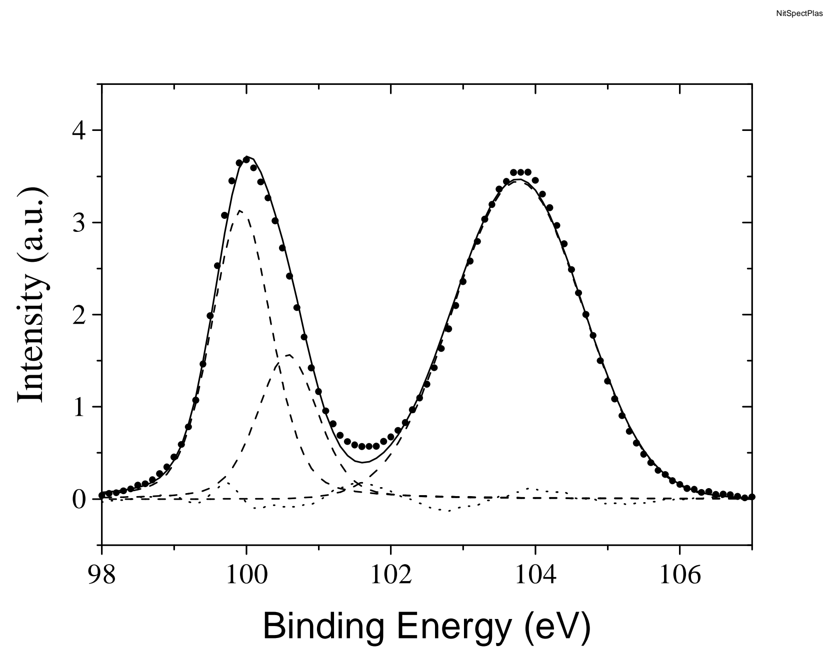


Fig. 7.2 (a) N1s spectrum and (b) Si2p spectrum with background removed for plasma-nitrided film after 15 s anneal in N_2O at 950ºC: (●●●) measured, (----) fit peaks, (——) sum of fit peaks, (·····) residual errors.

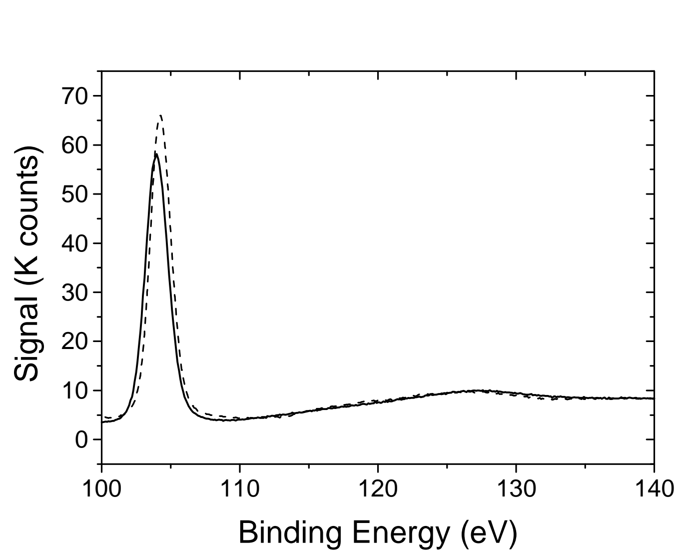


Fig. 7.3 XPS spectra of thick silicon dioxide (----) and silicon nitride films (——) showing the Si 2p features and associated peaks caused by inelastic scattering.

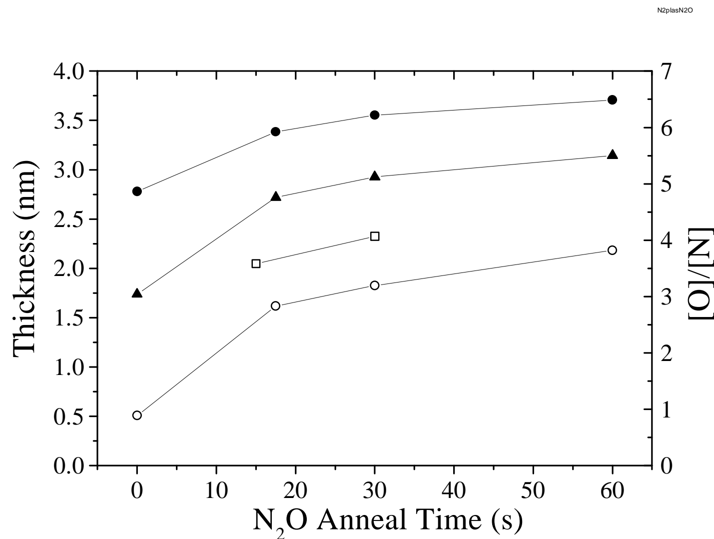


Fig. 7.4 Thickness and oxygen/nitrogen concentrations ratio as a function of annealing time in N_2O at 950 ºC for silicon oxynitride films deposited by LPCVD on Si(100): (●●●) thickness from XPS, (▲▲▲) equivalent oxide thickness determined from XPS measurements and calculated dielectric constant, (○○○) [O]/[N] from XPS measurements, (□) XPS thickness for Si (100) oxidized in N_2O at 950 ºC.

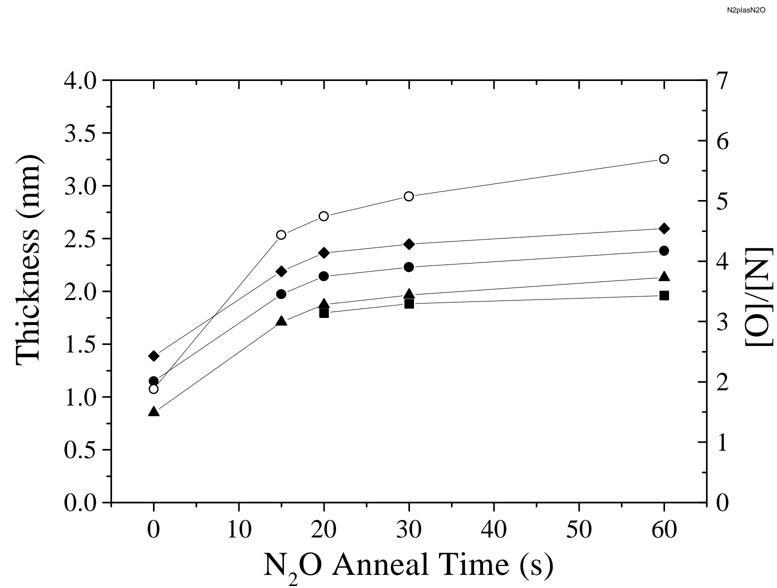


Fig. 7.5 Thickness and oxygen/nitrogen concentrations ratio as a function of annealing time in N_2O at 950 ºC for silicon oxynitride films formed by oxidation of Si(100) in NO followed by plasma nitridation: (●●●) thickness from XPS, (◆◆◆) thickness from XPS uncorrected for nitrogen (■■■) equivalent oxide thickness determined by electrical measurements, (▲▲▲) equivalent oxide thickness determined from XPS measurements, (○○○) [O]/[N] from XPS measurements.

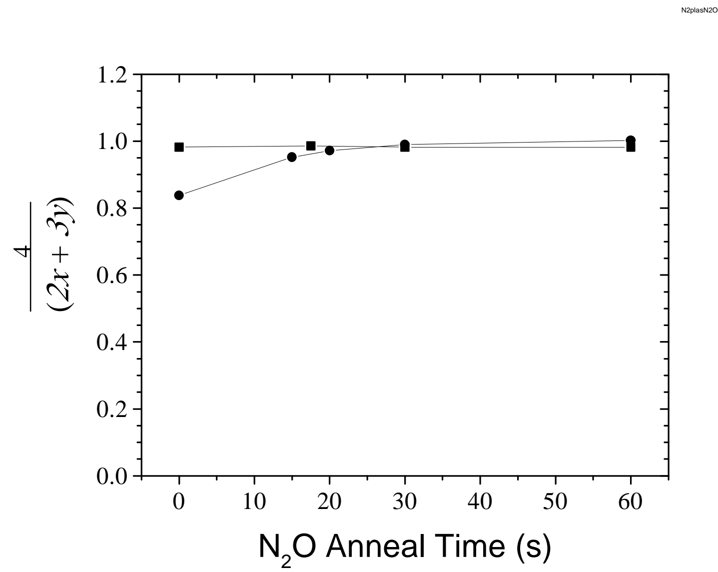


Fig. 7.6 The number of silicon bonds (magnitude of $4/(2x+3y)$) calculated using the XPS measurements for the plasma-nitrided (●●●) and LPCVD (■■■) films as a function of annealing time in N_2O at 950 ºC.

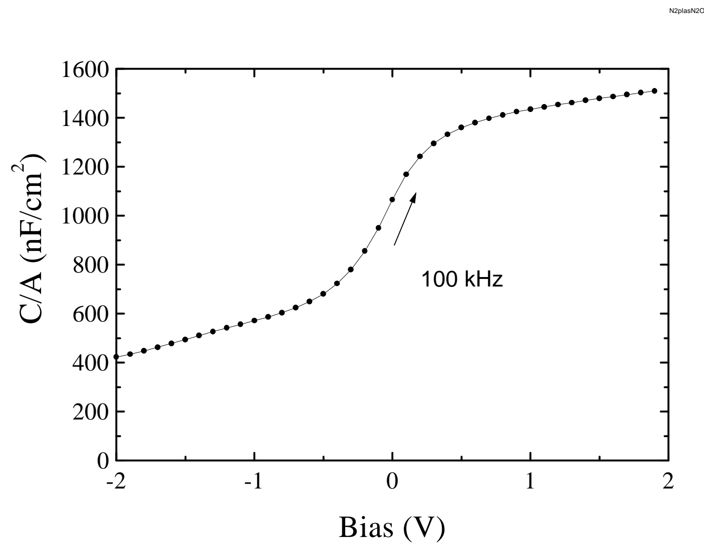


Fig. 7.7 Capacitance per unit area at 100 kHz vs voltage for plasma nitride film annealed for 30 s in N_2O at 950 ºC: (●●●) measured, (——) fit from NCSU CV program [52].

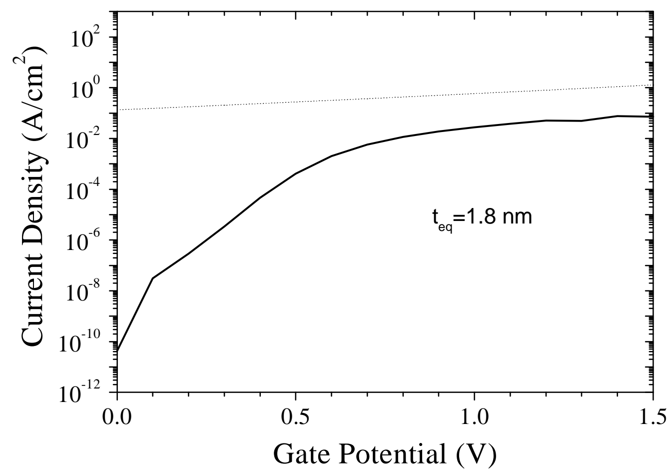


Fig. 7.8 Current density vs voltage for plasma nitride film annealed for 30 s in N_2O at 950 ºC: (——) measured, (·····) calculated from expression of Brar *et al.* [58].

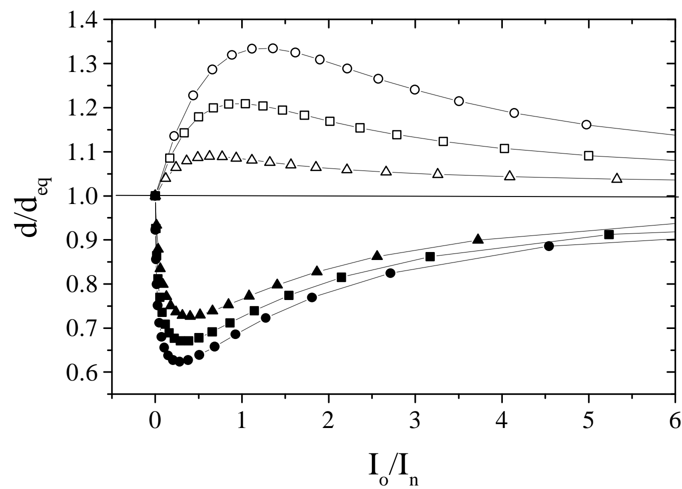


Fig. 7.9 Calculated XPS thickness, *d*, divided by equivalent oxide thickness, d_{eq}, for films consisting of a layer of silicon dioxide on top of a layer of silicon nitride (open symbols) or a layer of silicon nitride on silicon dioxide (solid symbols): (●●●) d_{eq} = 2.0 nm, (■■■) d_{eq} = 1.5 nm, (▲▲▲) d_{eq} = 1.0 nm.