Reliability Mechanisms of LTPS-TFT With HfO_2 Gate Dielectric: PBTI, NBTI, and Hot-Carrier Stress

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***Abstract*—In this paper, a comprehensive study of the reliability mechanisms of high-performance low-temperature polycrystalline-Si thin-film transistor (LTPS-TFT) with HfO_2 gate dielectric is reported for the first time. Various bias- and temperature-stress conditions, which correspond to positive-bias stress (PBS), positive-bias temperature instability (PBTI), negative-bias stress (NBS), negative-bias temperature instability (NBTI), and hot-carrier stress, are used to differentiate the distribution and mechanism of trap density states. The generation of deep-trap states of the effective interfacial layer (IL), tail-trap states of poly-Si grain boundaries, and electron trapping of the HfO_2 gate dielectric is observed for the PBS and PBTI of the HfO_2 LTPS-TFT. In addition, both the deep- and tail-trap states of the effective IL are generated under NBS and NBTI of the HfO_2 LTPS-TFT.**

***Index Terms*—HfO_2 gate dielectric, hot-carrier stress (HCS), low-temperature polycrystalline-Si thin-film transistor (LTPS-TFT), negative-bias temperature instability (NBTI), positive-bias temperature instability (PBTI), reliability.**

I. Introduction

LOW-TEMPERATURE polycrystalline-silicon thin-film transistors (LTPS-TFTs) have been devoted to achieve high-performance characteristics for the application of active-matrix liquid crystal displays (AMLCDs) and system-on-panel (SOP) on glass substrate [1]–[5]. In order to obtain high current-driving capability of LTPS-TFTs, the scaling down of the gate dielectric is an effective way to increase the gate capacitance density, resulting in the improvement of the driving current of LTPS-TFTs, because a large gate capacitance density can attract more carriers with a smaller gate voltage to fill up the traps to lower the potential barrier height in the poly-Si channel film [6] and make the LTPS-TFTs turn on within several voltages to improve the subthreshold swing S.S. and reduce the operation voltage. However, a higher gate leakage current would be introduced when the thickness of gate oxide becomes thinner to increase the gate capacitance density. Many high-κ gate dielectrics have been used to reduce the gate leakage current and increase the transconductance [7]–[12]. Among these dielectric materials, HfO_2 is the most promising candidate of future high-κ gate-dielectric material due to its high permittivity and thermal stability with poly-Si [10]–[12].

In recent years, LTPS-TFTs with high-κ gate dielectric have been developed to be suitable for the application of SOP [8]–[10]. The main limitation of LTPS-TFTs for the application of SOP is their reliability issue which is associated with the trap states in the grain boundaries of poly-Si channel film, interface of gate-oxide/poly-Si channel film, and gate-oxide film. Numerous degradation analyses, such as the carrier injection into the gate oxide, degradation of the channel interface, and the increase of trap states in the grain boundaries of the poly-Si channel film, have been proposed to explain the observed device-degradation behavior [13]–[20]. However, a comprehensive investigation of the reliability mechanism for LTPS-TFTs with HfO_2 gate dielectric has not been reported yet.

In this paper, various gate- and drain-bias-stress conditions are applied to study the instability of LTPS-TFTs with HfO_2 gate dielectric. In addition, two measurements and bias-stress temperatures of 25 °C and 125 °C are also employed to distinguish the degradation impacts of the effective interfacial layer (IL) and the grain boundaries of poly-Si channel film. These bias- and temperature-stress conditions could correspond to the positive-bias stress (PBS), positive-bias temperature instability (PBTI), negative-bias stress (NBS), negative-bias temperature instability (NBTI), and hot-carrier stress (HCS). Finally, a completed reliability mechanisms of LTPS-TFT with HfO_2 gate dielectric are proposed for the first time.

II. Experimental Procedure

The fabrication of devices started by depositing a 50-nm undoped amorphous Si (α-Si) layer at 550 °C in a low-pressure chemical-vapor-deposition system on Si wafers capped with a 500-nm-thick thermal oxide layer. Then, the α-Si layer was recrystallized by solid-phase crystallization process in furnace at 600 °C for 24 h in a N_2 ambient. A 500-nm-thick plasma-enhanced chemical-vapor-deposition oxide was deposited at 300 °C for device isolation. The oxide was then patterned and etched to define the active region of the device. The source and drain regions in the active device region were implanted with phosphorus (15 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24-h annealing in a N_2 ambient. Then, a 75-nm HfO_2 was deposited in vacuum ambient without any gas flow by electron-beam evaporation system at room temperature. An O_2

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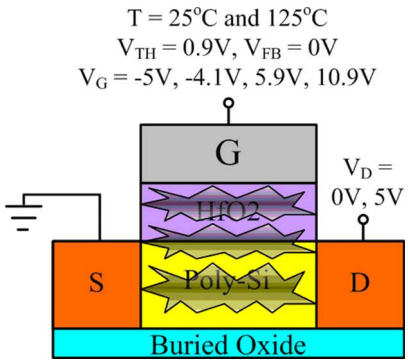

Fig. 1. Cross-section structure of Al/HfO_2/poly-Si n-channel LTPS-TFT with different V_G and V_D stress biases for 1000 s. The locations of stress damage are also indicated.

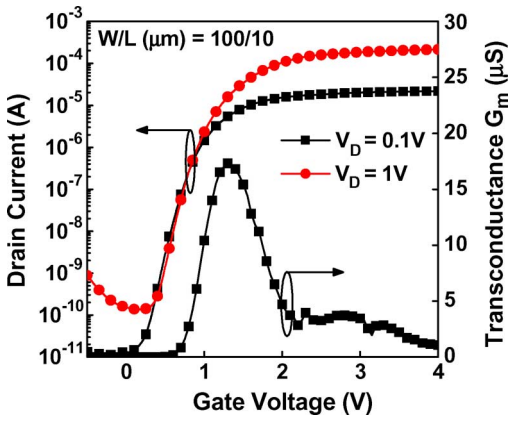

Fig. 2. I_D–V_G and transconductance G_m characteristics of the HfO_2 LTPS-TFT with $W/L = 100/10$ μm.

treatment in the furnace was applied to improve the gate-oxide quality at 400 °C for 30 min. A 75-nm HfO_2 with effective oxide thickness of 14.7 nm was measured to indicate a high permittivity of about 20 for HfO_2. In addition, a ~3-nm IL was also observed from the transmission electron microscopy micrograph of HfO_2 gate-dielectric LTPS-TFT, which is not shown here. After the patterning of contact holes, aluminum was deposited by thermal-evaporation system and patterned as the probe pads to complete the TFT devices.

The devices with gate length and width of 10 and 100 μm, respectively, were measured. The $V_{\rm TH}$ is defined as the V_G at which the I_D reaches 100 nA $\times$ W/L and $V_D = 0.1$ V. Different gate- and drain-bias stresses are performed at 25 °C and 125 °C, as shown in Fig. 1. The stress of $V_G = -5, -4.1, 5.9$, and 10.9 V represent $V_G - V_{\rm FB} = -5$ V, $V_G - V_{\rm TH} = -5$, 5, and 10 V, respectively. The flatband voltage $V_{\rm FB}$ is defined as the gate voltage that yields the minimum drain–current from the transfer characteristic [21]. The field-effect mobility $\mu_{\rm FE}$ is extracted from the maximum transconductance G_m.

III. Results and Discussion

Fig. 2 shows the transfer characteristics of the HfO_2 LTPS-TFT without any passivation treatment. High-performance HfO_2 LTPS-TFT with low threshold voltage $V_{\rm TH} \sim 0.9$ V, excellent subthreshold swing S.S. of ~0.147 V/dec, high field-effective mobility $\mu_{\rm EF} \sim 74.5\ {\rm cm}^2/{\rm V}\cdot{\rm s}$, and high $I_{\rm on}/I_{\rm min}$ current ratio $\sim 2.19 \times 10^6$ is demonstrated to be suitable for the applications of AMLCD and SOP. Some important parameters are listed in Table I. Compared with the conventional LTPS-TFT with thick SiO_2 gate dielectric, as shown in Table I, obviously, the LTPS-TFT with high-κ gate dielectric can lower the threshold voltage $V_{\rm TH}$, reduce the subthreshold swing S.S., improve the field-effect mobility $\mu_{\rm FE}$, and increase the $I_{\rm on}/I_{\rm min}$ current ratio without any hydrogen-related plasma treatment. The highly improved performance of LTPS-TFT with high-κ gate dielectric can be attributed to the employment of high-κ gate dielectric which can provide much higher gate capacitance density with thicker dielectric thickness and smaller gate leakage current.

TABLE I
Device-Parameter Comparison of the HfO_2 Gate-Dielectric TFTs. Other Gate-Dielectric TFTs Are Also Listed for Comparison

Parameters	HfO_2	$AlLaO_3$ [8]	Al_2O_3 [9]	LPCVD Oxide [2]	PECVD Oxide [3]
V_{TH} (V)	0.9	1.2	3	5.6	8.14
EOT (nm)	14.7	8.7	19.5	80	60
S.S. (V/dec.)	0.147	0.31	0.44	1.4	1.97
μ_{EF} (cm^2/V-s)	74.5	40	47	20	12.44
I_{on}/I_{min} (10^6)	2.19	1.5	0.3	0.35	0.297

In order to study the reliability mechanisms of HfO_2 LTPS-TFT, we divided the HfO_2 LTPS-TFT into three parts to discuss, as shown in Fig 1. They are the following: gate-dielectric film, effective IL of HfO_2/poly-Si, and poly-Si channel film. Because the defects in the HfO_2/poly-Si interface are correlated with the defects in the poly-Si grain boundaries of the conduction channel near the HfO_2/poly-Si interface, we define the effective IL as the combination of the HfO_2/poly-Si interface and the grain boundaries of poly-Si near the surface conduction channel which is about several nanometers below the HfO_2/poly-Si interface. Then, the distribution and mechanisms of the defect and trap-state generation will be discussed as follows according to the electrical properties of the HfO_2 LTPS-TFT such as threshold voltage $V_{\rm TH}$, transconductance G_m, gate leakage current, subthreshold swing S.S., and drain leakage current $I_{\rm min}$.

Based on the proposed degradation mechanisms, the generation of the fixed oxide charge in the gate-dielectric film would affect the threshold voltage $V_{\rm TH}$ and gate leakage current due to the variance in the potential of gate dielectric [22]. The subthreshold swing S.S. would depend on the defects in the effective IL. The deep-trap states existing in the grain boundaries of the effective IL have been demonstrated to degrade mainly the subthreshold swing S.S. and much less the transconductance G_m [21], [23], [24]. Moreover, the tail-trap states existing in the grain boundaries of the effective IL would mainly contribute to the degradation of the transconductance G_m and much less to the subthreshold swing S.S. [21], [23], [24]. In addition, the grain-boundary traps in the channel film would

TABLE II
DEGRADATION OF EXPERIMENTAL ELECTRICAL CHARACTERISTICS AND CORRESPONDING POSSIBLE DEGRADATION MECHANISMS

Defect location	Impacts of electrical characteristics	Cause
Gate dielectric film	1. Threshold voltage V_{TH} (V) 2. Flat-band voltage V_{FB} (V) 3. Gate leakage current (A)	Fixed oxide charge
Effective interfacial layer of HfO_2/poly-Si	1. Subthreshold Swing (S.S.) 2. Threshold voltage V_{TH} (V) 3. Transconductance G_m (S)	1. deep trap states 2. deep trap states 3. tail trap states
Poly-Si channel film	1. Transconductance G_m (S) 2. Drain leakage current I_{min} (A)	1. tail trap states 2.deep & tail states

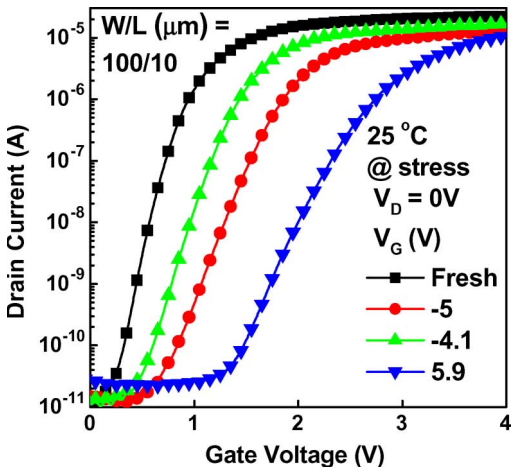

Fig. 3. I_D–V_G characteristics of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 0$ V for 1000 s at 25 °C.

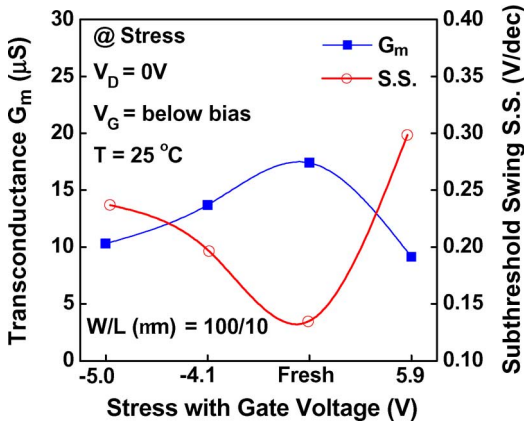

Fig. 4. Transconductance G_m and subthreshold swing S.S. of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 0$ V for 1000 s at 25 °C.

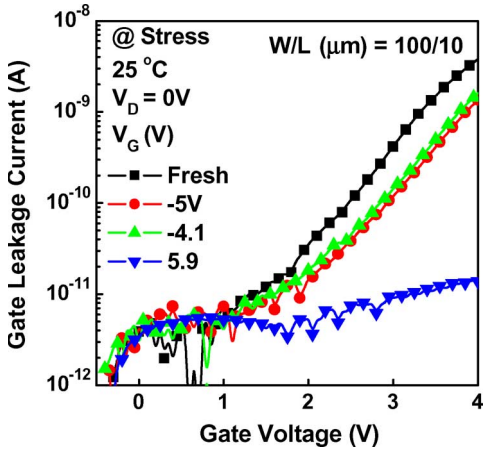

Fig. 5. Gate leakage current of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 0$ V for 1000 s at 25 °C.

also result in the drain leakage current $I_{\min}$ [23], [25]. Therefore, it is obvious that the electrical properties after stress could be used to clarify the generation and distribution of defects and trap states of the LTPS-TFTs. These proposed reliability mechanisms are summarized in Table II.

Fig. 3 shows the I_D–V_G characteristic of HfO_2 LTPS-TFT before and after NBS and PBS with $V_G = -5$, -4.1, and 5.9 V and $V_D = V_S = 0$ V for 1000 s at $T = 25$ °C. The threshold-voltage shift $\Delta V_{\rm TH}$ of PBS is more significant than the $\Delta V_{\rm TH}$ of NBS. Both the subthreshold-swing S.S. degradation and the fixed-oxide-charge generation, which is due to carrier injection, could result in the threshold-voltage shift $\Delta V_{\rm TH}$. Fig. 4 shows the subthreshold swing S.S. and the transconductance G_m of the HfO_2 LTPS-TFT before and after NBS and PBS, which indicates that more subthreshold-swing S.S. degradation of PBS is observed than that of NBS, resulting in more threshold-voltage shift $\Delta V_{\rm TH}$ of PBS than NBS. In addition to the different subthreshold-swing S.S. degradation of NBS and PBS, the flatband voltage shifts $\Delta V_{\rm FB}$ of NBS and PBS also show different behaviors. The NBS shows a slight increase of flatband shift $\Delta V_{\rm FB}$, and PBS shows a significant increase of flatband shift $\Delta V_{\rm FB}$. It indicates that more negative fixed charges are produced by PBS than NBS, which means that more electrons are injected into the HfO_2 from the channel film during PBS than the electron injection from gate during NBS. Electron trapping in HfO_2 would raise the electron potential of HfO_2 to reduce the tunneling of electrons, resulting in the decrease of gate leakage current. Fig. 5 shows the gate leakage current of the HfO_2 LTPS-TFT before and after NBS and PBS. A more significant gate-leakage-current reduction after PBS is observed than the one after NBS, which consists in the results of flatband shift $\Delta V_{\rm FB}$ that is due to the electron trapping in HfO_2. Therefore, the threshold-voltage shifts $\Delta V_{\rm TH}$ of PBS and NBS are mainly attributed to both the subthreshold-swing S.S. degradation and electron trapping in the HfO_2, and both the subthreshold-swing S.S. degradation and electron trapping of PBS are more serious than NBS, resulting in more threshold-voltage shift $\Delta V_{\rm TH}$ of PBS than NBS. Therefore, we can deduce that both PBS and NBS would produce the deep-trap states in the effective IL because of the subthreshold-swing S.S. degradation. In addition, the PBS degrades the device much more than the NBS does. In addition to the threshold-voltage shift $\Delta V_{\rm TH}$ and the subthreshold-swing S.S. degradation, Fig. 4 shows a similar transconductance degradation ΔG_m of PBS and NBS. Although the transconductance degradation ΔG_m of PBS and NBS is similar, the mechanisms of transconductance degradation ΔG_m of PBS and NBS are completely different,

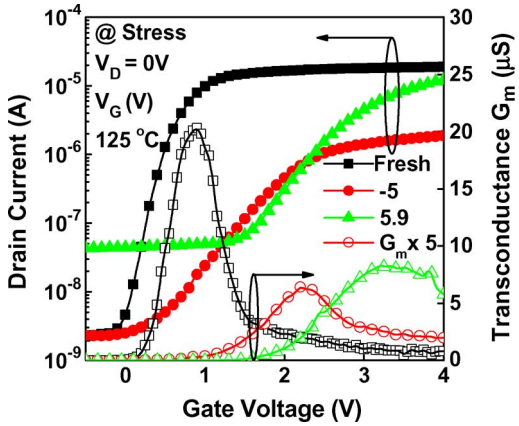

Fig. 6. I_D–V_G and transconductance G_m characteristics of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 0$ V for 1000 s at 125 °C.

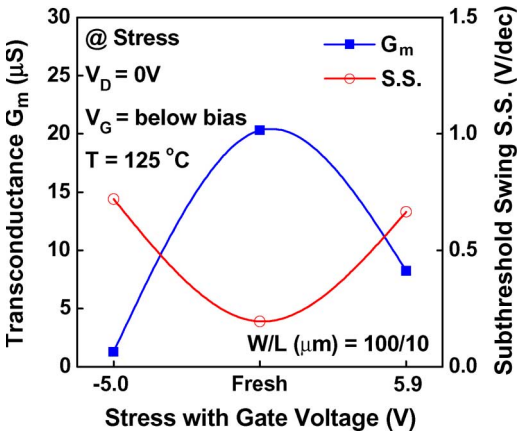

Fig. 7. Transconductance G_m and subthreshold-swing S.S. characteristics of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 0$ V for 1000 s at 125 °C.

and they will be distinguished in terms of NBTI and PBTI and discussed as follows.

Fig. 6 shows the I_D–V_G characteristic of HfO_2 LTPS-TFT before and after NBTI and PBTI with $V_G = -5$ and 5.9 V and $V_D = V_S = 0$ V for 1000 s at $T = 125$ °C. Similar subthreshold-swing S.S. degradation and threshold-voltage shift $\Delta V_{\rm TH}$ are observed for PBTI and NBTI. However, much more serious transconductance degradation G_m of NBTI is observed than that of PBTI, as shown in Figs. 6 and 7. In addition, the drain leakage current $I_{\rm min}$ also shows the remarkably different behavior that PBTI has a significant drain-leakage-current $I_{\rm min}$ degradation and NBTI shows a nearly invariant drain leakage current $I_{\rm min}$, as shown in Fig. 6, which indicates that the mechanism of NBTI is quite different from that of PBTI. The drain leakage current $I_{\rm min}$ can be attributed to two sources: One is coming from the gate leakage current, and the other is coming from the junction leakage current of drain side [25]. In this case, the gate leakage current, as shown in Fig. 8, has been shown to be too low to contribute to the drain leakage current $I_{\rm min}$ of devices. Therefore, we can conclude that the drain-leakage-current $I_{\rm min}$ degradation is coming from the junction leakage of the drain side, which is close to the surface. In PBTI device, the highest drain-leakage-current $I_{\rm min}$ increase

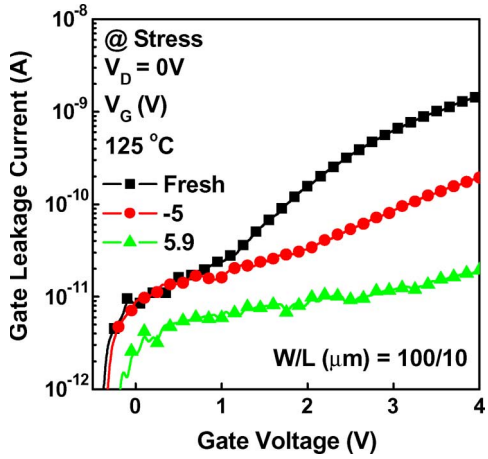

Fig. 8. Gate leakage current of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 0$ V for 1000 s at 125 °C.

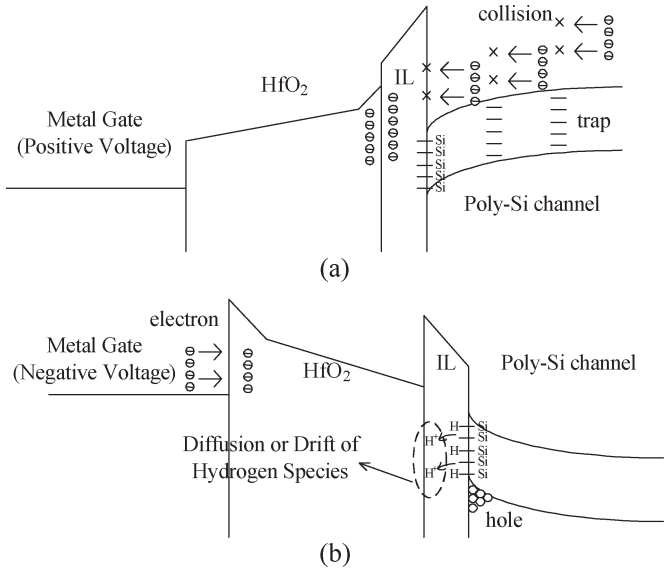

Fig. 9. Energy-band diagram of the HfO_2 LTPS-TFT under (a) PBTI and (b) NBTI stresses.

indicates the most serious grain damage in the channel film, resulting in significant increase of the drain leakage current $I_{\rm min}$. Therefore, we can deduce that the PBTI would attract electrons from the channel film to inject into the HfO_2 gate dielectric. During PBS, electrons would be accelerated by a positive gate voltage, and they move toward the interface of HfO_2/poly-Si, as shown in Fig. 9(a). The accelerated electrons would collide with the weak bond of the grain boundaries and damage the poly-Si channel film and the effective IL to generate the trap states to increase the drain leakage current $I_{\rm min}$ and subthreshold swing S.S. and reduce the transconductance G_m.

In addition to the PBTI, the NBTI would merely damage the effective IL to generate the trap states, increasing the subthreshold swing S.S. and reducing the transconductance G_m. Although the PBTI would degrade the grain boundaries of the channel film much more than the NBTI, the NBTI shows the most serious degradation of transconductance G_m. Therefore, the damage of NBTI would be in the effective IL, which is less dependent on the drain leakage current $I_{\rm min}$. Hydrogen

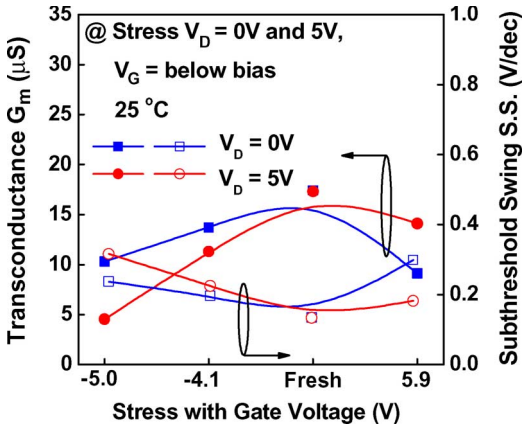

Fig. 10. Transconductance G_m and subthreshold-swing S.S. characteristics of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 0$ V and $V_D = 5$ V for 1000 s at 25 °C.

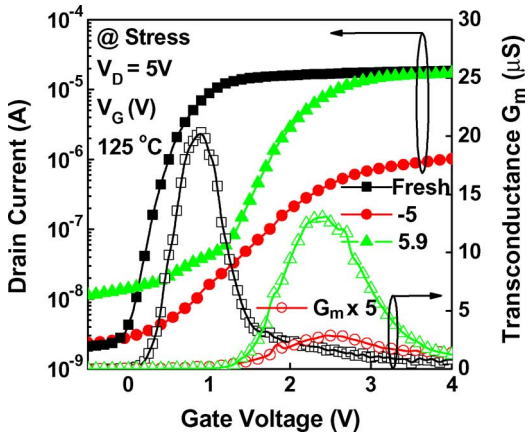

Fig. 11. I_D–V_G and transconductance G_m characteristics of the HfO_2 LTPS-TFT before and after different gate-bias stresses with fixed $V_D = 5$ V for 1000 s at 125 °C.

diffusion-controlled model, which is the electrochemical reactions between the holes and the hydrogen species, has been proposed to be the degradation mechanism of the LTPS-TFTs after NBTI [15], [20]. When an NBS is performed, holes will accumulate at the oxide/Si interface, and they react with the hydrogen species which are weakly bound to Si atoms, as shown in Fig. 9(b). The dissociation of hydrogen will then generate the interface trap states, and this is more important for high-κ gate-dielectric devices due to their high density of trap states. A significant subthreshold-swing S.S. degradation and transconductance G_m reduction indicate that both deep-trap and tail-trap states are generated after the NBTI stress.

The degradation model of LTPS-TFT under the NBTI stress can be described by the following [20]:

$$[\equiv \mathrm{Si}-\mathrm{H}]\ (\text{interface}) + [\equiv \mathrm{Si}-\mathrm{O}-\mathrm{Si} \equiv]\ (\text{interfacial oxide}) \rightarrow [\mathrm{Si}\bullet]\ (\text{interface}) + [\equiv \mathrm{Si}^{+}] + [\equiv \mathrm{Si}-\mathrm{OH}]\ (\text{interfacial oxide}) + e^{-}.$$

The hydrogen atoms are weakly bonded to the Si atoms at the interface of the polysilicon channel film. Under the NBTI stress, hydrogen atoms react with the holes from the inversion layer and dissociate from the Si atoms. The release of hydrogen atoms results in the generation of interface defects to form the deep-trap and tail-trap states and degrade the subthreshold swing S.S. and transconductance G_m, respectively.

Furthermore, a 5-V drain bias is applied during NBS and PBS to investigate the impacts of the drain-bias stress. Fig. 10 shows that more serious transconductance G_m and subthreshold-swing S.S. degradation of NBS with $V_D = 5$ V than $V_D = 0$ V are observed. Contrary to the NBS with drain-bias stress, the PBS with $V_D = 5$ V shows a slight improvement of the transconductance G_m and subthreshold-swing S.S. degradation compared with PBS with $V_D = 0$ V. In addition, the NBTI and PBTI with $V_D = 5$ V at $T = 125$ °C are also studied, as shown in Fig. 11. The same trend of the transconductance G_m and subthreshold-swing S.S. degradation is also observed compared with NBS and PBS with drain-bias application. However, for the PBTI case, the drain leakage current is decreased with $V_D = 5$ V compared with $V_D = 0$ V, as shown

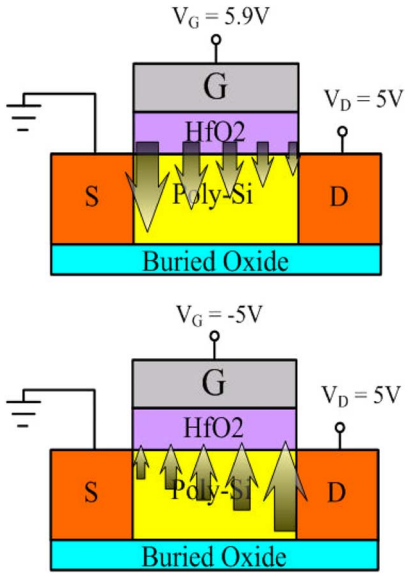

Fig. 12. Cross-section structure of Al/HfO_2/poly-Si n-channel LTPS-TFT with drain-bias stress for 1000 s. The magnitudes of vertical electric field are also indicated.

in Fig. 6. It is because that the application of a drain bias would make the vertical electric field near the drain side becomes lower and improve the drain leakage current $I_{\min}$ slightly. When a larger drain bias was applied during PBTI, the vertical electric field of the channel film would be decreased further. As shown in Fig. 12, applying a drain bias would decrease the vertical field near the drain side and result in less junction damage. Therefore, the large drain bias would make the device to have less drain-leakage-current $I_{\min}$ degradation, and a hump in transfer characteristic of the device is observed, as shown in Fig. 13. For the NBTI case, applying a drain bias would increase the vertical field near the drain side, as shown in Fig. 12, and result in more serious transconductance G_m and subthreshold-swing S.S. degradation. This appearance of asymmetry damage of the source/drain-junction region is also observed in the previous paper [15], [16]. In addition, the transconductance G_m of the HfO_2 LTPS-TFT would be decreased as the drain-bias increases after $V_D = 10$ V to indicate that the impact-ionization

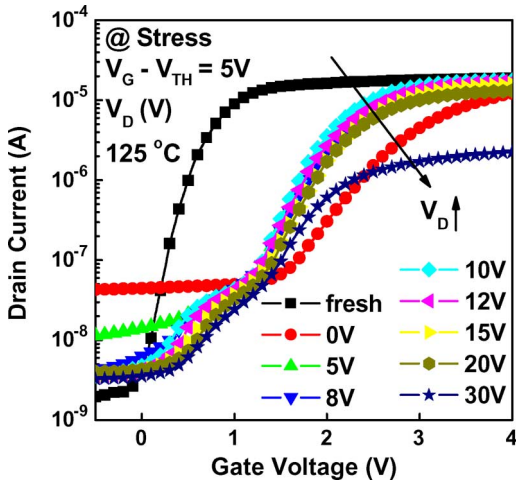

Fig. 13. I_D–V_G characteristics of the HfO_2 LTPS-TFT before and after different drain-bias stresses with fixed $V_G - V_{\rm TH} = 5$ V for 1000 s at 125 °C.

effect of HCS [16] is appearing, as shown in Fig. 13. Therefore, the stress of vertical electric field is more important than the stress of lateral electrical field for the HfO_2 LTPS-TFT before the occurrence of HCS, and the impact ionization of the HfO_2 LTPS-TFT dominates the degradation when the large drain-bias stress is applied.

The electron trapping in the gate dielectric and the trap-state generation of channel film and interface regions are observed for both HfO_2 and conventional thick SiO_2 LTPS-TFTs after PBS stresses [3], [19]. In addition, the significant subthreshold-swing S.S. degradation of HfO_2 and SiO_2 LTPS-TFTs after NBS stresses is observed [3], [14], [15]. However, the location of trap generation in interface or channel film is difficult to determine after PBS and NBS stresses. The mechanism of NBTI of the LTPS-TFT proposed by Chen *et al.* would be adopted to explain the behavior of NBS [20]. Therefore, the reliability mechanisms of positive-gate-bias stress and NBS can be systematically analyzed by studying the electrical characteristics of LTPS-TFT after NBS, PBS, NBTI, and PBTI stresses.

Comparing the stresses of HfO_2 LTPS-TFT with the conventional thick SiO_2 LTPS-TFT, the effective electric field of stress $E_{\rm eff}$ in the channel film $(E_{\rm eff} = V_G/t_{\rm dielectric} \times \varepsilon_{\rm dielectric}/\varepsilon_{\rm silicon})$ is quite different. The $t_{\rm dielectric}$, $\varepsilon_{\rm dielectric}$, and $\varepsilon_{\rm silicon}$ are defined as the gate-dielectric thickness, gate-dielectric permittivity, and silicon permittivity, respectively. The stress field of HfO_2 LTPS-TFT would be higher than that of the conventional thick SiO_2 LTPS-TFT. Large gate-bias stress at high temperature can accelerate the degradation to distinguish between positive-gate-bias stress and NBS. The remarkable $I_{\rm min}$ degradation behavior after PBTI is not observed in previous papers [3], [14], [15], [19] due to higher vertical stress field of HfO_2 LTPS-TFT. In addition, the hole trapping in gate dielectric after PBS and PBTI is not found in this paper. It could be due to the characteristic of high-κ gate dielectric in which electron trapping is easier than hole trapping. Moreover, the stress of vertical electric field is the dominant factor for the HCS of HfO_2 LTPS-TFT, which is completely different with previous report [19]. It would be due to the characteristic of high-κ gate dielectric that the ability of charge trapping is more significant than SiO_2.

So far, we have analyzed the reliability mechanisms of LTPS-TFT with HfO_2 gate dielectric. The employment of high-κ gate dielectric gives an effective way to keep the performance of LTPS-TFT at low operation voltage. In addition, many defect passivation methods have been proposed to improve the reliability of LTPS-TFT [26], [27]. High-performance and reliable LTPS-TFT with high-κ gate dielectric will be one of the most possible solutions to realize the target of system-on-panel.

IV. Conclusion

A comprehensive investigation of the reliability mechanisms of high-performance LTPS-TFT with HfO_2 gate dielectric is reported for the first time. Various stress conditions, including PBS, PBTI, NBS, NBTI, and HCS, are performed to differentiate the degradation mechanisms. For PBS and PBTI, it is found that serious subthreshold-swing S.S. degradation is due to the deep-trap states of the effective IL; the transconductance G_m decrease with the drain-leakage-current $I_{\rm min}$ increase is due to the tail-trap states of poly-Si grain boundaries, and the gate-leakage-current reduction is due to electron trapping of the HfO_2 gate dielectric. For NBS and NBTI, significant subthreshold swing S.S. and transconductance G_m degradation without the drain-leakage-current $I_{\rm min}$ increase are observed to show that the effective IL is the main damage region and that both deep- and tail-trap states are generated after NBS and NBTI. Remarkable drain-leakage-current $I_{\rm min}$ increase of PBTI and almost invariant drain-leakage-current $I_{\rm min}$ degradation of NBTI show that the PBTI and NBTI are attributing to different mechanisms. The carrier collision and injection model is employed to explain the mechanisms of PBS and PBTI, and the hydrogen-diffusion model is employed to explain the mechanisms of NBS and NBTI. In addition, the drain-bias application during stress is also studied, and the results show that the impact ionization will dominate the degradation mechanism if a large drain-bias stress is used.

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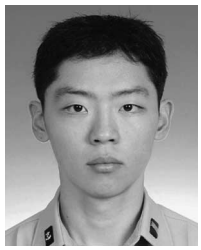

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