A Parabolic Potential Barrier-Oriented Compact Model for the k_BT Layer's Width in Nano-MOSFETs

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***Abstract*—On the basis of a parabolic potential profile around the source-channel junction barrier of nanoscale MOSFETs, a new compact model is physically derived, which links the width of thermal energy k_BT layer (a critical zone in the context of the backscattering theory) to the geometrical and bias parameters of the devices. The proposed model is supported by experimental data and by a critical analysis of various simulation works presented in the literature. The only fitting parameter remains constant in a wide range of channel length (10–65 nm), gate voltage (0.4–1.2 V), drain voltage (0.2–1.2 V), and temperature (100 K–500 K). The confusing temperature-dependent issues in the open literature are straightforwardly clarified.**

***Index Terms*—Backscattering, MOSFET, nanometer.**

I. Introduction

While applied to electrically saturated nanoscale MOSFETs, the channel backscattering theory [1], [2] establishes a link between the thermal energy k_BT layer, which occupies a small fraction of the conductive channel near the source, and the drive capability of the device. Thus, the ability to quantitatively determine the width of this critical zone is essential. To address the issue transparently, an analytically compact treatment is desirable. One such model can be quoted in the literature [3]

$$l \approx L\left(\frac{k_BT}{qV_D}\right)^{\alpha} \tag{1}$$

where l is the width of the k_BT layer, and L is the metallurgical channel length. However, so far, there has been some confusion as to the magnitude of the temperature power exponent α. First of all, fitting of the room-temperature I–V characteristics of a simulation double-gate MOSFET has produced the apparent $\alpha \approx 0.57$ [3]. Comparable $\alpha \approx 0.5$ has also been obtained on experimental bulk n-MOSFETs in a temperature range of 233 K–298 K [4], [5]. In contrast, for the bulk case covering the same temperature range, a higher $\alpha \approx 0.75$ has been experimentally determined [6]. Even $\alpha \approx 1$ has already been adopted in a temperature-dependent backscattering-coefficient extraction method [7]. This is also the case for the recent double-gate device simulation [8], which has shown that l is approximately proportional to the temperature from 100 K to 500 K. Obviously, these widespread values of the apparent α must be clarified. On the other hand, a study on experimental bulk n-MOSFETs has revealed that l significantly decreases with increasing gate voltage [4], [6]; however, it is difficult for (1) to elucidate due to the lack of the gate voltage. This hurdle may be overcome by accurate modeling of the potential profile in the channel [9]; however, a simple approach without loss of accuracy is favored.

In this brief, the experimentally determined parabolic potential profile in the previous work [4], [5] will be utilized to approximate the source-channel junction barrier of nanoscale MOSFETs in saturation. Then, a new compact model will be physically derived for l with the channel length, gate overdrive, drain voltage, and temperature as input parameters. The validity and applicability of the resulting model will also be examined, followed by a significant clarification on the aforementioned α differences.

II. Parabolic Barrier Picture

A parabolic potential profile near the source is schematically shown in Fig. 1. Its extension to the remaining channel can be described by

$$V(x) = V_D(x/\widetilde{L})^2. \tag{2}$$

The origin $x = 0$ indicates the peak of the barrier. $\widetilde{L}$ is the apparent channel length corresponding to a certain position where the parabolic potential drop from the top of the barrier is equal to V_D. Here, the barrier height with respect to the source side is neglected due to the large drain voltages used. By substituting $x = l$ into (2) for a local potential drop of k_BT/q to constitute the thermal energy layer [1], [2], the following expression can be obtained:

$$l = \widetilde{L}\left(\frac{k_BT}{qV_D}\right)^{0.5}. \tag{3}$$

$\widetilde{L}$ is expected to be a function of the channel length, gate and drain voltage, and temperature. In other words, there exists a set

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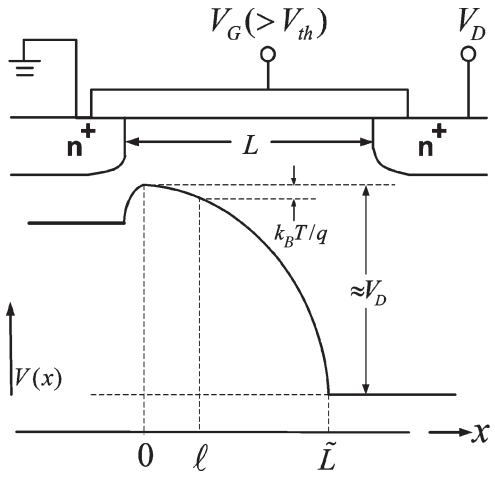

Fig. 1. Schematic demonstration of the parabolic source-channel potential barrier picture corresponding to nano-MOSFET in saturation. The parabolic potential profile is extended to the drain side to highlight the apparent channel length designated by $\widetilde{L}$. Also shown is the width l of the k_BT layer.

of the specific gate and drain voltage denoted by $V_{\rm Go}$ and $V_{\rm Do}$, respectively, at a given temperature T_o, which can ensure that $\widetilde{L} = L$. The corresponding thermal energy layer has a width denoted by l_o, which can be calculated from (3) with $\widetilde{L} \to L$, $T \to T_o$, and $V_D \to V_{\rm Do}$. Then, if the temperature individually changes from T_o to T, a power-law relation can hold: $\widetilde{L} = L(T/T_o)^{0.5}$. This formalism can be obtained by assuming that the potential profile does not change with temperature; that is, the local electric field across the thermal energy layer ($\approx k_BT_o/ql_o$, according to the backscattering theory [1], [2]) at T_o is approximately equal to that ($\approx k_BT/ql$) at T. As for gate-voltage factor, a similar relation can be physically derived but expressed in terms of the gate overdrive (the gate voltage V_G minus the threshold voltage $V_{\rm th}$). This is achieved by twice differentiating (2) with respect to x, leading to $d^2V(x)/dx^2 = 2V_D/\widetilde{L}^2$, which, according to Poisson's equation (see [3] for details), can be linearly related to the underlying inversion-layer carrier density or, equivalently, the gate overdrive. As a result, one achieves $\widetilde{L} = L((V_{\rm Go} - V_{\rm th})/(V_G - V_{\rm th}))^{0.5}$. Here, the term $V_{\rm Go} - V_{\rm th}$ represents the specific gate overdrive for $\widetilde{L}$ approaching L. Finally, if the drain voltage increases to $V_D(> V_{\rm Do})$, the local electric field [$= 2V_Dx/\widetilde{L}^2$ as from (2)] must be larger than that ($= 2V_{\rm Do}x/L^2$) at $V_{\rm Do}$. As a result, one obtains $\widetilde{L} = L(V_D/V_{\rm Do})^{\nu}$ with the power exponent ν of no more than 0.5. This formula remains valid for $V_D < V_{\rm Do}$. Indeed, ν of around 0.25 has been experimentally determined elsewhere [4] and will be cited here.

Through the combination of the aforementioned power-law relationships, a unique expression can be created for $\widetilde{L}$

$$\widetilde{L} = \eta L \frac{V_D^{0.25}}{(V_G - V_{\rm th})^{0.5}} \left(\frac{k_BT}{q}\right)^{0.5}. \tag{4}$$

Here, $\eta = (k_BT_o/q)^{-0.5}(V_{\rm Go} - V_{\rm th})^{0.5}V_{\rm Do}^{-0.25}$. In this brief, η is fixed and is also the only fitting parameter. It is expected that η is a constant, regardless of the channel length, gate and drain voltage, and temperature; otherwise, the applicability of the resulting model may be limited.

III. Confirmative Evidence and Clarification

The experimental l was created from 55-nm bulk n-MOSFETs by means of a parameter extraction process detailed elsewhere [4]–[6]. The results are shown in Fig. 2 versus gate voltage for two drain voltages of 0.5 and 1.0 V and three temperatures of 233 K, 263 K, and 298 K. With known l, T, and V_D, the corresponding $\widetilde{L}$ can be obtained directly from (3), as shown in Fig. 2(c) and (d) versus the gate voltage. The near-equilibrium threshold voltages denoted by $V_{\rm tho}$ are 0.360, 0.345, and 0.328 V for 233 K, 263 K, and 298 K, respectively, and the drain-induced barrier lowering (DIBL) magnitudes are 120, 123, and 130 mV/V, respectively. Throughout this brief, the threshold voltage $V_{\rm th}$ at higher drain voltages is equal to $V_{\rm tho} - {\rm DIBL} \times V_D$ [4]–[7]. Also shown in Fig. 2 are the calculated results from (3) and (4) using a specific η whose value will be explained slightly later. On the other hand, the rich literature [8], [10] dedicated to double-gate device simulations is quoted. First, in [8], the extracted l at $V_D = V_G = 1$ V is available in a wide range of the channel length from 14 to 37 nm and the temperature from 100 K to 500 K. The underlying threshold voltage $V_{\rm tho}$ and DIBL are reasonably 0.3 V and 110 mV/V, respectively [10]. Second, the citation [10] can further provide the relevant data at 300 K: l from 2.0 to 7.0 nm, L from 14 to 65 nm, $V_D(= V_G)$ from 1.0 to 1.2 V, and DIBL from 11 to 230 mV/V. In addition, we have also extracted l directly from the published channel potential profiles on the simulation double-gate devices [2], [3], [9], [11], [12]. The corresponding key parameters are the following: 1) $L = 10$ nm, $V_{\rm tho} \approx 0.33$ V, DIBL ≈ 140 mV/V, $V_D = 0.6$ V, $V_G = 0.6$ V, and $T = 300$ K [2]; 2) $L = 20$ nm, $V_{\rm tho} \approx 0.33$ V, DIBL ≈ 25 mV/V, $V_D = 0.2$ V, $V_G = 0.55$ V, and $T = 300$ K [3]; 3) $L = 25$ nm, $V_{\rm tho} \approx 0.3$ V, DIBL $\approx$ 100 mV/V, $V_D = 0.8$ V, $V_G = 0.5$, 0.8, and 1.0 V, and $T =$ 300 K [9]; 4) $L = 15$ nm, $V_{\rm tho} \approx 0.2$ V, DIBL ≈ 120 mV/V, $V_D = 0.7$ V, $V_G = 0.7$ V, and $T = 300$ K [11]; and 5) $L =$ 15 nm, $V_{\rm tho} \approx 0.3$ V, DIBL ≈ 77 mV/V, $V_D = 0.7$ V, $V_G =$ 0.7 V, and $T = 300$ K [12]. At this point, a scatter plot can be created, as shown in Fig. 3, in terms of the experimental and simulated l versus the quantity of the functional expression $LV_D^{0.25}(V_G - V_{\rm th})^{-0.5}(k_BT/q)^{0.5}(k_BT/qV_D)^{0.5}$. Strikingly, all data are seen to fall on or around a straight line. The slope of the line furnishes η with a value of 4.1 $\rm V^{-0.25}$. As expected, η remains constant, regardless of the channel length, gate and drain voltage, and temperature.

Some remarks can now be made to clarify the confusing α values in the open literature [3]–[8]. First, it is noticed that in the case of bulk n-MOSFET, two different values of α were produced: one of 0.5 [4], [5] and one of 0.75 [6]. This difference can be attributed to the different subband treatments during the parameter extraction process. A Schrödinger–Poisson equation solving was utilized in [4] and [5], whereas in [6], this was done by a triangular potential approximation [13]. Therefore, the different subband levels can lead to different average thermal injection velocities, which in turn give rise to different l values. Second, based on (4), the temperature range of 233 K–298 K in case of a 55-nm bulk device [4], [5] is not large enough to affect the calculated $\widetilde{L}$. In other words, $\widetilde{L}$ is considerably

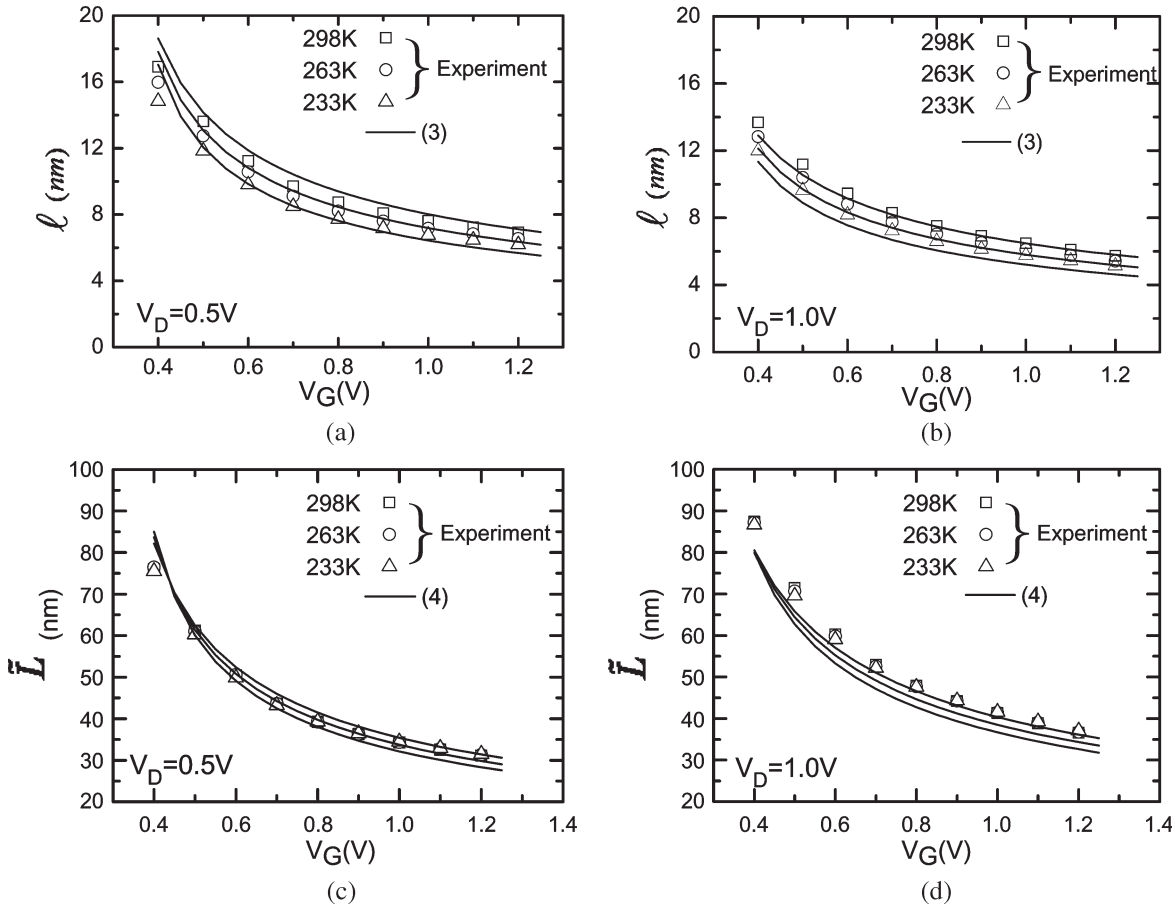

Fig. 2. Measured and calculated l versus gate voltage at two drain voltages of (a) 0.5 V and (b) 1.0 V for three temperatures and the corresponding $\widetilde{L}$ versus gate voltage for the drain voltages of (c) 0.5 V and (d) 1.0 V. The test device is a 55-nm bulk n-MOSFET. The calculation lines are from (3) and (4) with $\eta = 4.1\ \mathrm{V}^{-0.25}$.

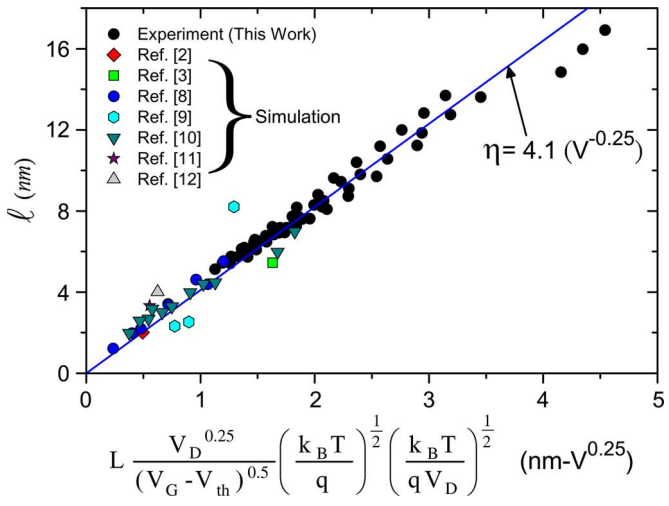

Fig. 3. Scatter plot of the experimental and simulated l versus the quantity of the functional expression $L(V_D^{0.25})(V_G - V_{\mathrm{th}})^{-0.5}(k_BT/q)^{0.5}(k_BT/qV_D)^{0.5}$. Also shown is a straight line which fits the data points. The slope of the line yields η of 4.1 $\mathrm{V}^{-0.25}$.

insensitive to such a narrow temperature range. Consequently, the resulting apparent temperature power exponent was limited to 0.5, as reported in the previous work [4], [5]. Indeed, with the known η as input, fairly good reproduction can be achieved, as shown in Fig. 2, without adjusting any parameters. The same interpretations also apply to the $\alpha \approx 0.57$ case [3]. Only the room temperature of operation was involved, and therefore, the temperature effect of $\widetilde{L}$ can no longer be examined. In other words, only in a wide temperature range (as done in the comprehensive study of [8] and [10]) can the linear relationship of $l \propto T$, as shown in Fig. 3, be observed. Finally, from the aspect of temperature dependences or the excellent coincidence with a significant number of data, as shown in Fig. 3, the existing backscattering-coefficient extraction method [7] is valid.

IV. Conclusion

Based on a parabolic potential profile that is used to approximate the source-channel junction barrier of nanoscale MOSFETs, a new compact model of the k_BT layer's width has been physically derived along with the channel length, gate overdrive, drain voltage, and temperature as input. The validity of the parabolic potential barrier picture and the applicability of the resulting compact model have been justified by experimental data and by a critical analysis of various simulation works presented in the literature. In particular, the confusing temperature-dependent issues in the open literature have been satisfactorily clarified.

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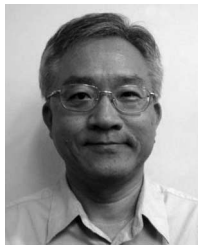

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