行政院國家科學委員會補助專題研究計畫成果報告

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計畫主持人：曾 俊 元
共同主持人：
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□赴國外出差或研習心得報告一份
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□出席國際學術會議心得報告及發表之論文各一份
□國際合作研究計畫國外研究報告書一份

執行單位：國立交通大學電子工程學系

中　華　民　國　90 年 12 月 31 日

八十九年度 【 SBT鐵電薄膜製備與特性的分析（IV） 】經費核定清單

執行機關：國立交通大學電子工程學系　　主 持 人：曾俊元　　教授

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研究成果歸屬：國立交通大學

"SBT 鐵電薄膜製備與特性分析"
成果報告

國科會計畫編號
NSC89-2112-M009-067

主持人：曾俊元
國立交通大學電子工程學系

一、 中文摘要(關鍵字：鉭鈮酸鍶鉍、金屬-鐵電膜-絕緣層-半導體、鐵電記憶體、高介電)

目前使用鐵電電容的 1T1C 結構鐵電隨機存取記憶體是一種破壞性的讀取。實際上我們較希望得到非破壞性讀取的鐵電場效電晶體元件。然而在這方向的進展上仍存在許多挑戰，主要是鐵電薄膜和矽基板間的間介面特性差，且資料保存時間也不長。爲了克服這些問題，通常在鐵電薄膜和矽基板之間加上阻擋層。本研究使用磁控濺鍍法在二氧化矽阻擋層上成長鉭鈮酸鍶鉍鐵電薄膜。探討在不同基板溫度和氧偏壓下的鐵電特性，最後進行這金屬-鉭鈮酸鍶鉍薄膜-二氧化矽-矽基板結構的可靠度檢視。

二、 英文摘要(Keyword：SBTN、MFIS、FRAM、high-k)

At the present time, the 1T1C structure ferroelectric random access memeory (FRAMs) using ferroelectric capacitor is a destructive readout. In principle, it is much more desirable to build a nondestructive readout memory device based on the ferroelectric memory field-effect transistor (FEMFET). However, there are many challenges which have held back the progress in that direction, a major one being the difficulty of making an electrically switchable ferroelectric thin film on Si with good interface properties and long retention time. To overcome these problems, buffer layers are usually inserted between the ferroelectric layer and silicon substrate. In our study, rf sputtering was employed to grow SBTN ferroelectric thin films on SiO_2/Si substrate at various deposition temperatures and oxygen to argon mixing ratios (OMR). The ferroelectric properties and reliability of the Pt/SBTN/SiO_2/Si structure were also examined.

三、 結果與討論

The SBTN thin films were prepared on 270Å oxide insulator. The crystallinity of the films was probed by X-ray diffraction using Cu-Kα radiation source.The surface morphology and film thickness were examined by scanning electron microscopy (SEM) using Hitachi model S4700. The leakage current vs. applied electric field (J-E) measurements were carried out using a semiconductor parameter analyzer (Hewlett-Packard HP4156). Computer controlled HP4284 system was used to obtain high frequency C-V. The capacitance-voltage (C-V) characteristics were measured on the MFIS structure at 1 MHz under different sweeping voltage bias. HP8116A (Programmable Pulse/Function Generator) combined with HP4284 were used to measure fatigue property.

The thickness of the ferroelectric film affects the characteristics of the film. Since the electric fields in each layer is sensitive to the thickness of ferroelectric SBTN and insulator layers, optimizing the thickness of the layers is

extremely important to obtain the required memory window at reasonable operating voltages. Therefore the three different thickness of SBTN films 200, 300, and 400 nm were deposited on the SiO_2 buffer layer. The crystallinity of those films was examined by x-ray diffraction. As shown in Fig.1, the intensity of diffraction of the SBTN film increases with increasing thickness. The (115) peak is closely related to the ferroelectric properties of the film, and we would obtain better ferroelectric properties in thicker film, whick has higher (115) peak.

Fig.2 shows the capacitance versus applied voltage curves (C-V curve) of MFIS structure deposited at various thicknesses with fixed SiO_2 27 nm buffer layer. The sweeping voltage changed from −10 to +10V and back. Counterclockwise hysteresis loop is clearly observed as traced by arrows for the 400 nm thickness film, indicating that the memory effects were due to ferroelectric domain reversion and not due to charge injection. But the hysteresis loop disappears for the film with thickness below 300 nm, indicating that the applied electric field in the ferroelectric layer is insufficient to induce polarization reversal.

The deposition temperature plays an important role in the physical and electrical properties. Fig.3 depicts the change of the deposition rate of $Sr_{0.8}Bi_{2.5}Ta_{1.2}Nb_0O_9$ (SBTN) thin films deposited at various substrate temperatures. It indicates that the deposition rate decreases slightly with increasing substrate temperature. We check the crystallinity of those films from XRD result. As shown in Fig.4, the 40• •OMR SBTN films on silicon dioxide show increased intensity of diffraction peak from 500 to 575 ℃ substrate temperature. The films is polycrystalline structure in nature. Except for the main (115) peak, the other peaks (200), (117) and (224) can be found and become stronger with the increasing temperature.

The curves of normalized C-V characteristics of an Pt/SBTN/SiO_2/n-Si(100) diode are shown in Fig.5. The film thicknesses of SBTN and SiO_2 are approximately 400 nm and 27 nm, respectively. The C-V curves show counterclockwise hysteresis loops, indicating that the memory effect was due to ferroelectric domain reversal and not due to charge injection. This means that ferroelectric hysteresis controls the Si surface potential and that this can be applied to an MFIS-FET memory device. The maximum memory window for 500 ℃, 40% OMR film is 3.37 V. It is clearly seen from Fig.5 that the decrease in memory window tends to be accompanied with an increase in substrate temperature. As mutual atomic diffusion between the SBTN thin film and the Si substrate occurs easily at a high substrate temperature, the SiO_2 film shows larger leakage compared with that for a lower substrate temperature. This leads to an enhanced charge injection, and counterclockwise C-V hysteresis is reduced. We also notice that the memory window shifts along voltage axis and does not center at zero voltage. It may be possibly caused by some fixed charge in insulating layer.

Fig.6 shows the leakage current density variation as a function of the electric field for the 40% OMR SBTN film deposited at various substrate temperatures with a delay time of 3 seconds. It indicates that the leakage current densities of these films are all below $1.2*10^{-8}$ A/cm^2 under electric field of 200 kV/cm. With

the increase in the substrate temperature, the (115) peak increases gradually. Therefore, the film deposited at high substrate temperatures has larger grain size and electric dipole. The roughness causes the nonuniform electric field distribution in SBTN and SiO_2 films. Hence, the leakage current density increased with the increasing deposition temperature.

The oxygen to argon mixing ratio (OMR) used in sputtering deposition process is an important factor to affect the properties of SBTN films. Therefore, we study how the OMR affect the ferroelectric properties of the films. Fig.7 shows the deposition rate of 500° C SBTN films deposited with various OMR. The lower content of argon in the sputtering gas decreases the deposition rate of the film due to the decrease of the sputtering probability.

Fig.8 shows the curves of normalized capacitance versus applied voltage of the Pt/SBTN/SiO_2/n-Si(100) diode in which the SBTN film deposited at 500° C with various OMR. It is clear that the memory window tends to decrease as the OMR is lowered. The interdiffusion between the Si substrate and the SBTN thin film deposited with low OMR easily occurs, which leads to an enhanced leakage current density(Fig.9) and reduced counterclockwise C-V hysteresis.

Besides at the high measuring frequency of 1 MHz, a slight increase is observed in the inversion capacitance. Generally, an increase in inversion capacitance is explained to be due to the generated minority carriers in accordance with the variation of the measuring signal. However, the phenomenon should be happened at the low frequency and not arised at the high frequency. This phenomenon may be explained by the following mechanism. Carriers are trapped and detrapped at the trap levels distributed near the SBTN/SiO_2 interface. The trapped charges cancel the memory effect induced by the ferroelectric polarization and the movement of the charges between the trap levels located at SBTN/Si interface raises the inversion capacitance measured at 1 MHz.

Fig.10 shows the C-V curves for the 500° C, 40 % OMR films deposited on SiO_2/Si substrate under different switching cycles. It is indicated that accumulation capacitance is reduced from its initial value after the switching duration. The reduced accumulation capacitance may be attributed to the decreased dielectric constant of the SBTN film by the fatigue. Besides, the memory window decreases with the increasing switching cycles. Fig.11 shows fatigue characteristics of the memory window in a MFOS structure. The fatigue test is performed using a bipolar triangle wave of 8 V at 10 kHz below 10^6 cycles and 1 MHz over 10^6 cycles. We can find that it has degradation of memory window at fatigue cycle over 10^6. The memory window is decreased from 2.27 V to 1.59 V after fatigue pulses of 10^{11} cycles. This phenomenon may be attributed to the increased leakage between F-I-S interfaces which resulted from interfacial reaction.

Memory retention characteristics were measured from the C-V curve in the Pt/SBTN/SiO_2/Si/Al capacitor, where write 'on' and 'off' pulse voltages are +10 V and −10 V. Fig.12 shows that the change of capacitance with time. After applied a pulse voltage of +10V or −10V, small signal capacitance was measured by using a signal (1 MHz and 25 mV) under a holding voltage at 0 V dc bias. The data storage

and measurement were executed at room temperature. The memory capacitance decreased linearly along the logarithm of the retention time. The capacitance difference between two states decreased by 40 % after retention time of 7000 sec. The retention time is directly related to the leakage characteristics in the MFOS structure. To decrease the leakage current density it is necessary to decrease grain size in the SBTN film, suppress mutual diffusion between F-O-S interface and reduce the electric field in the SBTN and SiO_2 films. The decrease in leakage current of the film can increase the retention time.

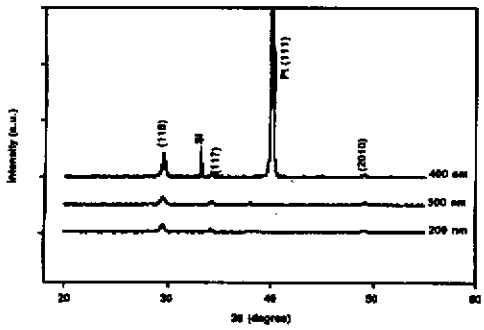

Fig.1 XRD patterns of 25 % OMR SBTN thin films with various thickness deposited on SiO_2/Si

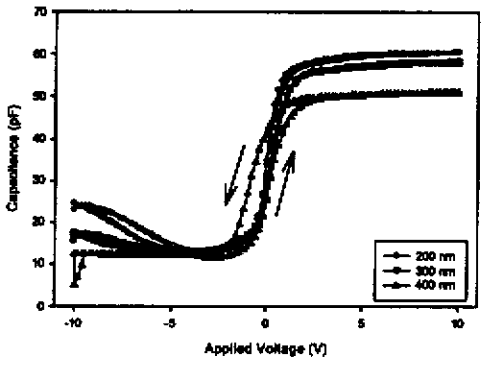

Fig.2 C-V curve of various thickness SBTN films with a sweeping voltage from +10 to -10 V and back

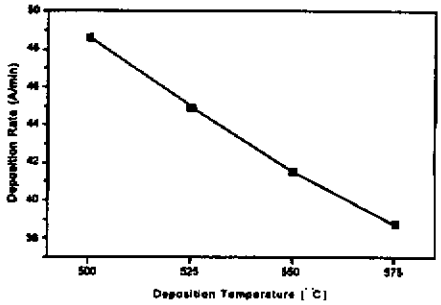

Fig.3 The deposition rate of 40 % OMR SBTN films deposited at various substrate temperatures

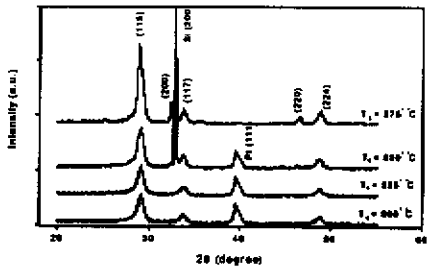

Fig.4 XRD patterns of 40 % OMR SBTN films deposited on SiO_2/Si substrates at various deposition temperatures

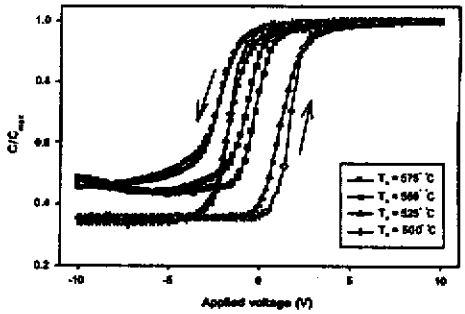

Fig.5 Normailized C-V curve of SBTN films deposited on SiO_2/Si substrates at various substrate temperatures

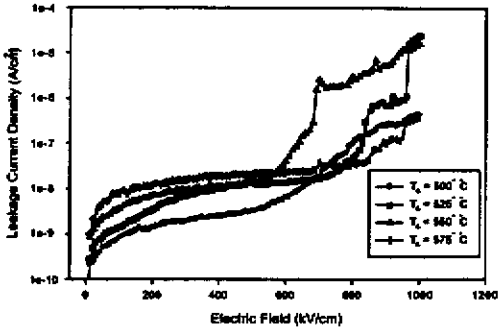

Fig.6 J-E curve of the SBTN films deposited on SiO_2/Si substrates at various substate temperatures

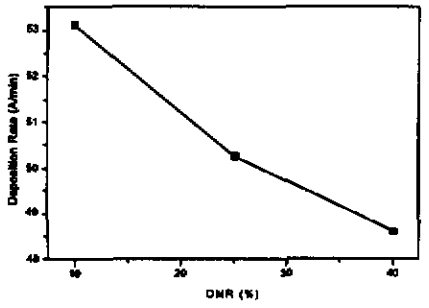

Fig.7 The deposition rate of 500° C SBTN films with various OMR .

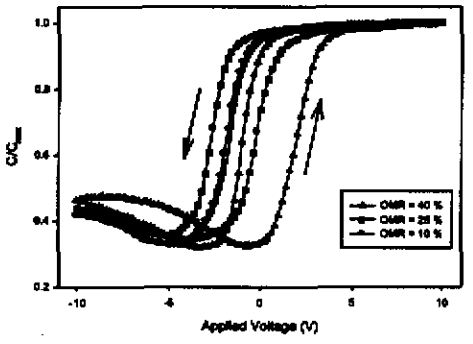

Fig.8 Normailized C-V curve for SBTN films deposited on SiO_2/Si substrates at various OMR. A sweeping voltage from +10 V to -10 V and back

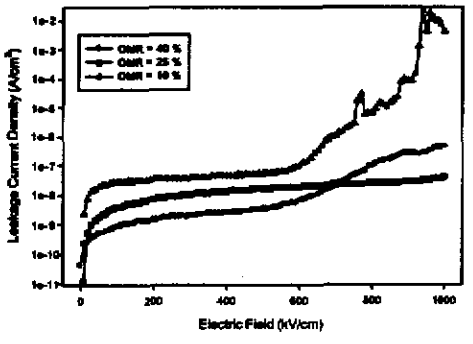

Fig.9 J-E curve for the SBTN films deposited on SiO_2/Si substrates at OMR indicated

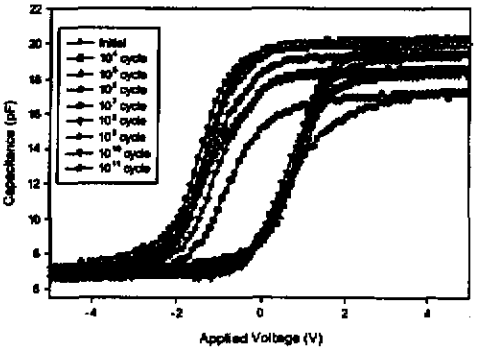

Fig.10 C-V curve of SBTN films deposited on SiO_2/Si substrates at various switching cycles

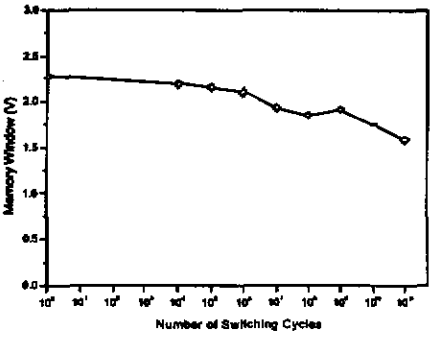

Fig.11 Fatigue characteristics of the memory window with SBTN films deposited at 500° C, 40 % OMR

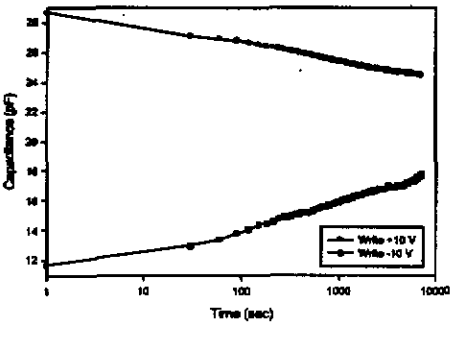

Fig.12 Retention characteristics of Pt/SBTN/SiO_2/Si capacitor with 525 ° C, 40 % OMR SBTN films