RF CMOS 雜訊分析與可靠性研究
RF CMOS Noise Analysis and Reliability

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一、中文摘要

由於無線通訊的發展，RF CMOS 已成為一極具前瞻性之研究領域。在本計劃中，吾人提出一新的雜訊模擬方法，進一步預測元件高頻雜訊的特性。吾人模擬結果顯示，在短通道的元件中，閘極電流雜訊主要是由熱雜訊所主導，而熱載子效應微導致此熱雜訊的主要原因。

Abstract

The main concern for this work will focus on the simulation of noise within MOS devices. We report a new noise simulation method by the use of 2D device simulator (TMA Medici) which accurately predicts the RF noise performance of MOS transistors. Our study reveals that the drain current noise is dominated by the thermal noise in short channel devices. To explain the phenomenon of raised γ for short channel devises, probably only hot carrier effect can account for it.

二、計劃緣由與目的

Due to grate flourish of wireless communications, radio-frequency integrated circuits are becoming more in demand. The majority of RF IC's are typically implemented in GaAs or silicon bipolar technologies because of their relatively high cutoff frequency. Comparably, with the progress in process technology the continuing scaling down of the minimum channel length has given rise to the increasing cutoff frequency. As a consequence, the CMOS devices start to emerge in the components of RF IC's [1]. In this study, we focus on the deviation of noise for RF CMOS. Rather than constructing an analytical noise model, the simulation task is performed directly through numerical calculation which is implemented into the framework of 2D device simulator (TMA Medici). The simulation approach makes use of a two-step technique of classical methods for noise analysis [2][3]. First, a set of microscopic noise sources is identified in terms of carrier velocity and number fluctuations, called diffusion and generation recombination noise sources, respectively. Second, the effect of microscopic fluctuations on voltage at the device terminals is evaluated. This latter task is performed through linear perturbation of the transport model and solution through a Green's function technique.

三、結果與討論

A. Uniformed-Doped Resistor

As a first example of application of noise analysis implemented into TMA Medici, 2D simulation of uniformly doped semiconductor samples is presented. The simulation sample is 1μm thick and 100μm long, the doping level is $10^{14}cm^{-3}$ for n-type. FIGURE 1. shows the frequency dependence of the noise voltage spectrum S_V for an electric field of 10 V/cm. As expected, the noise voltage spectrum shows the characteristic of white noise at low frequency, while it shows a low-pass behavior at high frequency. The low-pass behavior is related to the parasitic capacitance of the resistor.

According to the Nyquist theorem, the exact form of the noise voltage spectrum is $S_V=4KTRe[Z(f)]$. In order to perform the simulation in TMA Medici, there must be two ohmic contacts attaching between both sides of the resistor. Consequently, as for the two ohmic contacts, there are one resistor and one capacitor in parallel. Hence the small signal impedance is given as

$$Z(f) = \frac{R}{1 + j2ffRC} \qquad (4)$$

Implying that

$$Re(Z(f)) = \frac{R}{1+(2ffRC)^2} \qquad (5)$$

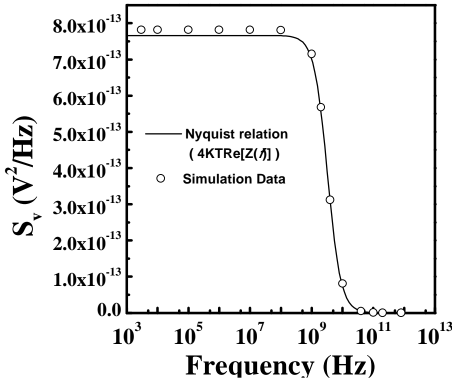

FIGURE 1. Frequency dependence of voltage noise power spectrum density for a 100μm long uniformly doped semiconductor simulation sample. The open circle is simulation data, whereas the solid line is calculated according to the Nyquist relation.

Consequently, the noise voltage spectrum for the resistor is

$$S_V = 4KT \cdot \frac{R}{1+(2\pi fRC)^2} \tag{6}$$

Return to the simulation case, $R=4.62\times10^{7}\ \Omega\text{-}\mu m$ and $C=1.05\times10^{-18} F/\mu m$.

B. Schottky-Barrier Diode

The schottky-barrier diode is formed by a metal making contact with a uniformly-doped n-type semiconductor and the device is 0.1 μm wide and 2 μm deep. The noise behavior of a Schottky-barrier diode shows the shot noise, and the theoretical expression of power spectrum for shot noise is $2qI$, where I is the DC diode current. FIGURE 2. shows the *I-V* characteristic of the simulation sample. Beyond the cut-in voltage, diode current increasing linearly with the applied voltage has been observed. This is due to the depletion region in the semiconductor shrinks and the neutral region contributes a finite resistance r_s.It will be indicated that the noise simulation is influenced by the r_s quite well.

The noise simulation result is illustrated in FIGURE 3. Apparently, the simulation result nearly matches with the predicted data 2qI within the diode turn-on range. Yet the simulation result is two or three times smaller than the predicted data and the deviation towards larger as the applied voltage increased.

As for our simulation case, the noise model should be revised, i.e. incorporating the thermal noise due to r_s in addition to the intrinsic component of shot noise. The modified noise model is involving two noise sources connected in series. The equivalent total noise current spectrum should be two noise current spectrum in parallel. It depicts that there is one shot noise source connected with a thermal noise source in series. Accordingly, the equivalent total current noise power of the two components should be

$$S_{total} = (S_{shot} \parallel S_{thermal}) = \frac{1}{\frac{1}{2qI}+\frac{r_s}{4KT}} = \frac{2qI}{1+\frac{2qI\cdot r_s}{4KT}} \tag{7}$$

Since the simulation outcome is S_{total}, and once the applied voltage is beyond the built-in voltage, the deviation between S_{total} and $2qI$ will become larger. This influence is in quite agreement with the trend of our simulation result.

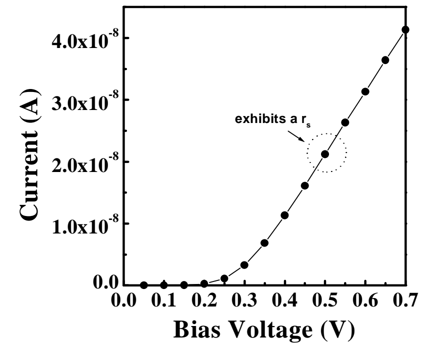

FIGURE 2. I-V characteristic curve for the simulation sample of Schottky-barrier diode.

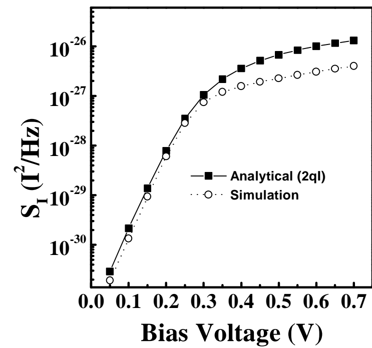

FIGURE 3. Comparison of noise current spectrum for a Schottky-barrier diode between the analytical result and simulation data.

C. n-channel MOSFET

The approach to simulate drain current noise for MOS transistors is following from the procedure mentioned above. Both long channel device and short channel device will be covered. The feature for noise analysis is depicted in FIGURE 4.

The drain current noise is typically represented by

$$\overline{i_d^{\,2}} = 4KTXg_{d0}\Delta f \qquad (8)$$

Here, X is a bias-dependent parameter, g_{d0} is zero drain voltage conductance of the channel and Uf is the noise bandwidth.

FIGURE 5. shows the drain current noise and the extract γ parameter for a 1.5 ~*m* NMOS. The simulation result of g_{d0} is equal to *1.23Î10*$^{-4}$ *S/~m.* Also, one can see as shown in FIGURE 5. that γ is about equal to 1 for linear region and 2/3 for saturation region which are in well agreement with the expected value for the long channel device.

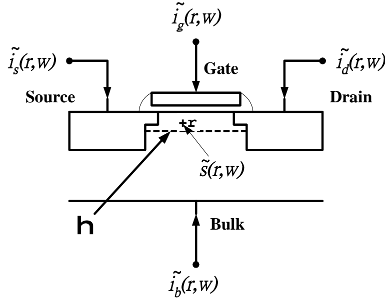

FIGURE 4. The features of noise source within the device and output current noise at terminals are depicted. Domain where the noise analysis is performed is outlined by Ω.

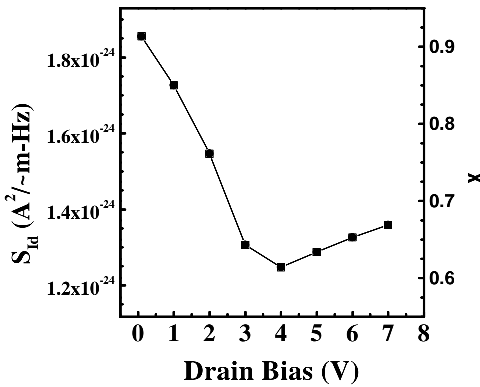

FIGURE 5. Drain bias dependence of drain current noise power spectrum and extracted parameter γ for 1.5μm NMOS. Gate bias is fixed at 5V, and substrate is grounded.

Next, a short channel device of 0.24 ~*m* NMOS transistor is simulated. We will perform the simulation by the use of both Drift-Diffusion model and Hydrodynamic model. The major difference between the two is without or with coupling temperature effect. FIGURE 6. shows the extracted γ parameter for various V_{ds} at V_{gs}*=2V.* It should be noted that the extracted X parameter increases as V_{gs} increases for Hydrodynamic model.

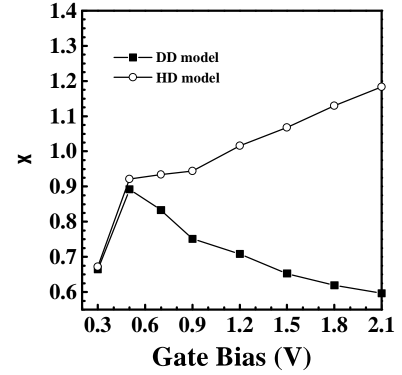

FIGURE 6. Gate bias evolution of extracted noise parameter γ comparing Hydrodynamic and Drift-Diffusion model results. V_{ds} is fixed at 2V.

Since it is found that excess drain current noise occurs in short channel devices The majority tends to explain this due to hot carrier effects [4], while some others claim that shot noise accounts for the excess drain current noise [5]. As a consequence, the Hydrodynamic model is incorporated in the simulation to couple the temperature effect. Our simulation results reveal that the standard Drift-Diffusion model cannot account for the excess drain current noise, whereas the Hydrodynamic model can. So we believe that hot carrier effects account for the excess drain current noise.

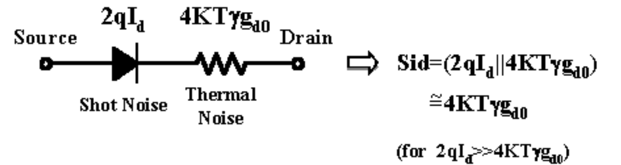

FIGURE 7. The feature of two noise source, i.e. shot noise and thermal noise, connected in series.

It cannot be denied that both shot noise and thermal noise do coexist in the channel for MOS transistors. To distinguish which one truly dominates for short channel devices, we use the model in FIGURE 7. to prove that thermal noise do dominate the drain current noise. From FIGURE 7., the two noise are in series, so the drain current noise power spectrum is

$$S_{id} = 2qI \,||\, 4KTXg_{d0} \qquad (9)$$

Whatever it is for long channel or short channel device, the term *2qI* is always much larger than

$4KTXg_{d0}$, it yields that the drain current noise is dominated by the thermal noise. To explain the phenomenon of the raised X for short channel devices, probably only hot carrier effects can account for it.

So far the drain current noise within the MOS transistors have been successfully derived from our simulation. However, only the insight of the microscopic noise behaviors is investigated, a perspective viewpoint of noise performance for a device is not revealed yet. As for the noise performance of a device, the figure of merit leads to the four noise parameters. Consequently, a noise equivalent circuit model will be demonstrated in order to derive the for noise parameters. A small-signal lumped circuit model of a MOSFET including the noise source with each noise component is illustrated in FIGURE 8 [5]. From the noisy two port equivalent circuit, one can derive the four noise parameters as follows

$$G_n = (\frac{f}{f_t})^2 X g_{d0} \quad (10)$$

$$R_{opt} \cong (\frac{f_t}{f})\sqrt{\frac{R_g + r_s}{X g_{d0}}} \quad (11)$$

$$X_{opt} = \frac{1}{wC_g} \quad (12)$$

$$F_{\min} \cong 1 + 2\frac{f}{f_t}\sqrt{X g_{d0}(R_g + r_s)} \quad (13)$$

$$f_t = \frac{1}{2fC_g} \quad (14)$$

The four noise parameters can be derived from applying equation (10-13) with the simulation results described before. f_t can be extracted from the simulation results of y-parameters, while R_g cannot be derived from simulation. Base on our measurement experience, we take R_g=20h. The simulation results of the four noise parameters for a 5 ~m /0.24 ~m nMOS with V_d=2V, V_g=0.9V are as FIGURE 9.

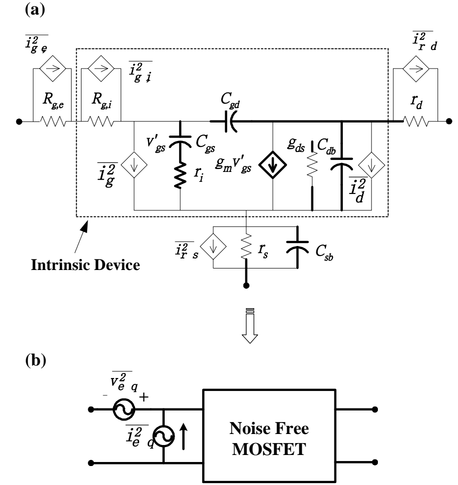

FIGURE 8. (a) Noise equivalent circuit model of a MOSFET. (b) Noiseless network with equivalent input noise sources.

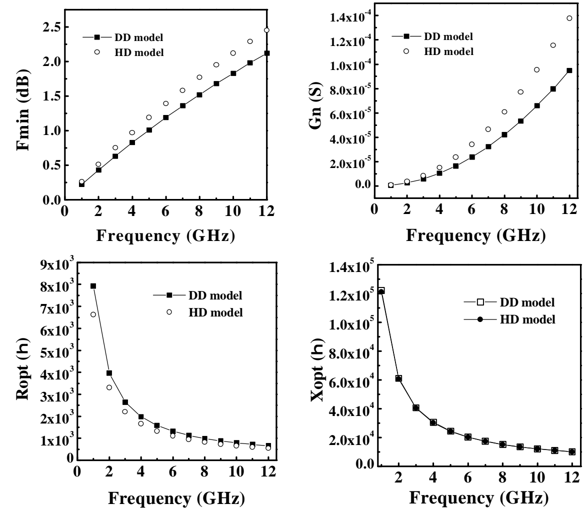

FIGURE 9. Frequency dependence of minimum noise figure (Fmin), noise conductance (Gn), optimum noise resistance (Ropt), and optimum noise reactance (Xopt) comparing Drift-Diffusion and Hydrodynamic model results. The bias condition is 0.9V for gate and 2.0V for drain.

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