高介電氧化鋁閘極於下世代深次微米技術的應用

High-K Al_2O_3 gate dielectrics on next generation VLSI technology

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主持人：荊鳳德
學生：陳晞白
交通大學電子工程系

一、中文摘要

藉由直接氧化沈積在矽晶片上的鋁膜，可以成長出氧化鋁薄膜。K 值為 8.5 的 21Å 及 36 Å 氧化鋁具有等效氧化層厚度約 9.6Å 及 16.5Å。21 Å氧化鋁在 1V 的偏壓下漏電流密度為 0.4 A/㎠，介面缺陷密度約在 2~3×10^{11} $eV^{-1}/㎠$，而 3,600 秒 2.5V 的偏壓下，仍有很好的可靠度，以上證明了氧化鋁薄膜具有好的介電特性。

關鍵詞：閘極介電質、氧化鋁、介電性質

Abstract

We have investigated the gate dielectric integrity of Al_2O_3 formed by a simple process using direct oxidizing the deposit Al on Si. The 21Å and 36 Å Al_2O_3 gate dielectric have a K value of 8.5 that is equivalent to an oxide thickness of 9.6Åand 16.5Å Good dielectric integrity is evidenced by the very low leakage current density of 0.4 A/cm^2 at 1V for 21 Å Al_2O_3, low interface-trap density of 2~3×10^{11} eV^{-1}/cm^2, and good reliability measured by the small SILC after 2.5V stress for 3,600s.

Keywords: gate dielectric, Al_2O_3, dielectric integrity

二、緣由與目的

By continuously scaling down the CMOS technology, ultra-thin gate dielectrics with equivalent oxide thickness below 10-15Åwill soon be needed for sub-0.1μm devices. Although recently Si_3N_4 gate dielectric has been studied extensively for replacing thermal SiO_2 [1]-[2], the marginal improvement is due to the relatively lower K and slightly higher leakage current. Thus, Si_3N_4 might be used only for one or two generations of device scaling. Therefore, the search for alternative gate dielectric with higher dielectric constant than Si_3N_4 is urgently required for future VLSI generation [1]-[4]. In addition to high K value, this alternative gate dielectric must also have low leakage current, good interface property, good thermal stability, small stress-induced leakage current (SILC), good reliability, and process compatibility to existing VLSI technology. Recently, we have developed the Al_2O_3 material [5]-[6] as another candidate for high K gate dielectric that has a K value of ~ 9 higher than Si_3N_4. Further, the Al_2O_3 gate dielectric can satisfy almost all the above requirement except that the relatively high interface-trap density and slightly large dielectric thickness [8]. In this paper, we have further improved the dielectric integrity of Al_2O_3. We have achieved a low leakage current density of 10^{-6} A/cm^2 at 1V with an equivalent oxide thickness of 18Åand 0.4 A/cm^2 at 1V for 21 Åwith an equivalent oxide thickness of 9.6Å Al_2O_3. The interface-trap density is about 2~3 × 10^{11} eV^{-1}/cm^2. Good reliability is evidenced by the small SILC after 2.5V stress for 3,600s.

三、實驗步驟

Standard p-type Si wafers with resistivity of ~10 Ω–cm were used in this study. After device isolation, amorphous Al layer is deposited by ultra-high vacuum molecular beam epitaxy (MBE) system. A HF-vapor passivation [7]-[8] is used to reduce the desorption temperature of native oxide in MBE before Al deposition. The deposited Al is first oxidized at a temperature of 500°C for 1 hour by oxygen followed by a 900°C furnace annealing for 30 min in nitrogen ambient. In comparison with chemical-vapor deposited (CVD) or sputtering deposited Al_2O_3, the direct oxidation process is simpler and may have better gate dielectric property because it is well known that thermal SiO_2 has better integrity than CVD SiO_2. MOS devices were formed after a 3000Å poly-Si deposition and subsequent patterning.

四、結果與討論

In order to get accurate K and EOT, the oxide thickness is carefully examined by both ellipsometer and TEM in Fig. 1. The very uniform oxide and smooth interface are due to native oxide free surface and high thermal stability as contact with Si. Fig. 2 shows the J-V characteristics of 21Å and 36Å Al_2O_3 capacitor. Good Flower-Nordheim (F-N) tunneling behavior is observed that suggests relatively low defect concentration. A breakdown electric voltage of ~4V for 36Å Al_2O_3 is measured that is high enough for sub-μm devices application. A low leakage current density of 10^{-6} A/cm^2 is measured at 1V; to our best knowledge, this is the lowest reported value for high K gate dielectric with an equivalent oxide thickness of 16.5Å Fig. 3 shows the cumulative values for 21Å Al_2O_3, and leakage current of 0.4 A/cm^2 are obtained. The related dielectric constant is measured by C-V characteristics in Fig. 4, and a value of 8.5 is obtained.

In order to apply Al_2O_3 gate dielectric to current CMOS technology, good interface-trap density is unavailable because it is directly related to low frequency noise of MOS transistor [9]. We have therefore measured the interface-trap density for the 36Å Al_2O_3 that is obtained from the quasi-static and high frequency C-V curves. Fig. 5 shows the measured interface-trap density. A minimum interface-trap density of 2~3× 10^{10} eV^{-1}/cm^2 is obtained that is close to conventional thermal SiO_2. It is also important to notice that further reduction of interface-trap density is possible using forming gas annealing. However, the weak hydrogen-Si bond at interface may degrade the device reliability [10]. The lower interface-trap density for 36Å Al_2O_3 than our previous work may be due to the thinner thickness for oxygen penetration and additional SiO_2 formed beneath Al_2O_3. This is evidenced by the slightly lower K value as compared to our previous report.

Gate dielectric reliability is another important factor for practical VLSI application. We have measured Al_2O_3 reliability under a constant voltage stress of 2.5V for 3,600s. Fig. 6 plots the SILC to show the difference between fresh and stressed devices, and Fig. 7 is the current variation during stress. No soft breakdown can be found even after a charge injection of 2.5 C/cm^2. Excellent reliability is evidenced from the tiny current change during stress and very small SILC after stress as shown in Fig. 8. The excellent SILC resistance may be important for certain device application such as flash memory. Therefore, the Al_2O_3 gate dielectric is suitable for continuous operation at VLSI generations of 2.5V and beyond.

五、計畫成果自評

We have studied the gate dielectric integrity of Al_2O_3 formed by direct oxidizing the deposit Al on Si. The 38Å Al_2O_3 gate dielectric have a K value of 8.5 that is equivalent to an oxide thickness of 18Å

Good dielectric integrity is evidenced by the very low leakage current density of 10^{-6} A/cm^2 at 1V, low interface-trap density of $2\sim3\times10^{11}$ eV^{-1}/cm^2, and good reliability measured by the small SILC after 2.5V stress for 3,600s. In addition to high K value, these dielectric properties are very close to conventional thermal SiO_2.

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Figure Captions:

Fig. 1. Cross-section TEM of 21Å Al_2O_3. Very smooth interface is due to the high thermal stability and native oxide free surface.

Fig. 2. J-V characteristics for 21Åand 36ÅAl_2O_3 capacitors.

Fig. 3. Cumulative distribution of leakage current and for 21Å Al_2O_3 gate dielectrics.

Fig. 4. Hysteresis curves for 21ÅAl_2O_3 gate dielectrics.

Fig. 5. Interface state density of Al_2O_3 on Si. Min D_{it} of $3x10^{10}$ eV^{-1}/cm^2 is obtained for both dielectrics and close to SiO_2/Si.

Fig. 6. Stress induced leakage current and current variation for Al_2O_3 under -2.5V for 1hr.

Fig. 7. Time evolution of I_g under -2.5V for 1hr with Q_{inj} of $1.5x10^5$ C/cm^2 for Al_2O_3.

Fig. 8. The leakage current difference for 21ÅAl_2O_3.

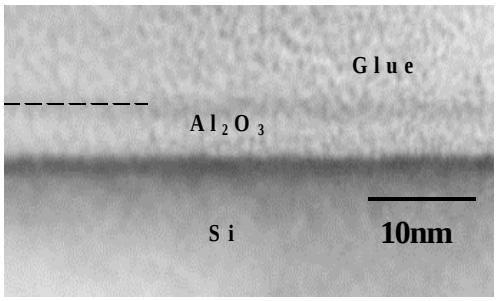

Fig. 1

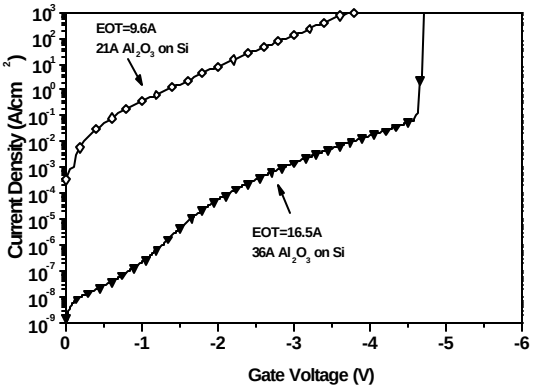

Fig. 2

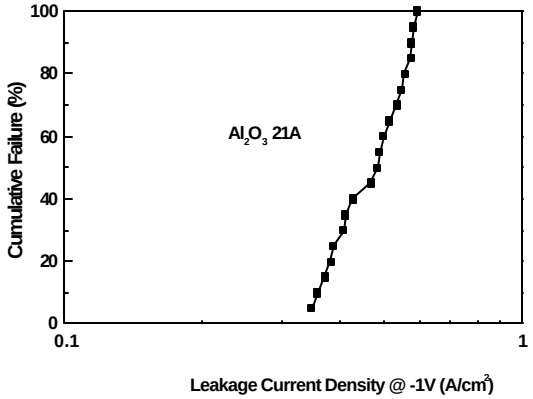

Fig. 3

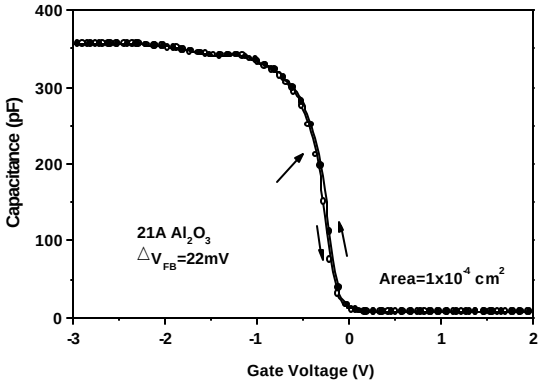

Fig. 4

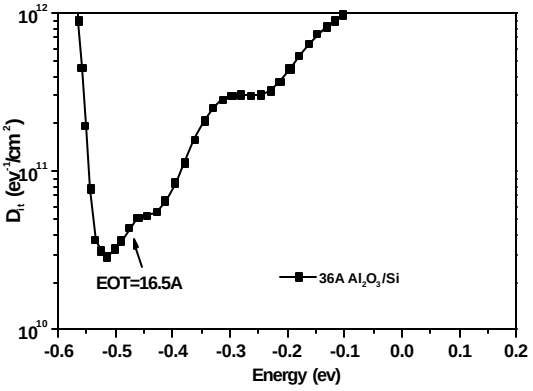

Fig. 5

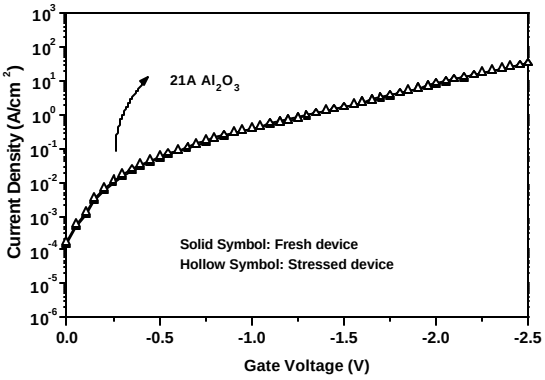

Fig. 6

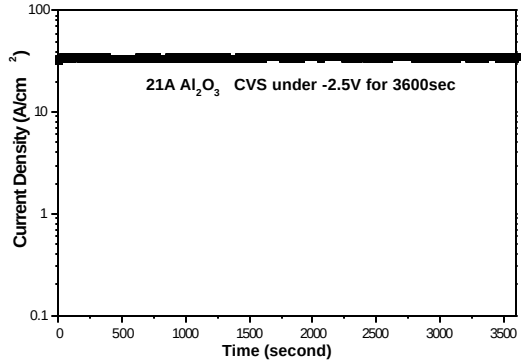

Fig. 7

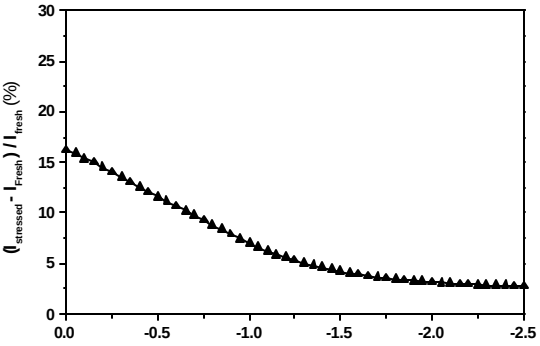

Fig. 8